

## Introduction

This document provides the design specification for the AXI Ethernet core. This core can implement a tri-mode (10/100/1000 Mbps) Ethernet MAC or a 10/100 Mbps Ethernet MAC. It supports most popular PHY interfaces including 1000BASE-X and SGMII. The core optionally supports Ethernet AVB (Audio Video Bridging) functions. This core provides a control interface to internal registers via a 32-bit AXI4-Lite Interface subset. This AXI4-Lite slave interface supports single beat read and write data transfers (no burst transfers).

The transmit and receive data interface is via the AXI4-Stream interface.

This core is based on the Xilinx hard silicon Ethernet MAC in the Virtex<sup>®</sup>-6 devices and provides a soft Ethernet MAC option for supported devices.

This core has been designed incorporating the applicable features described in IEEE Std. 802.3-2003.

## Features

- Independent 2 K, 4 K, 8 K, 16 K, or 32 K Byte TX and RX
- Filtering of *bad* receive frames
- Support for several PHY interfaces
- Media Independent Interface Management access to PHY
- Full Duplex support
  - Half Duplex is not supported
- Optional support for jumbo frames up to 16 K Bytes
- Optional TX and RX TCP/UDP partial checksum off load
- Support for VLAN frames
- Optional TX and RX VLAN tagging, stripping, and translation

LogiCORE IP Facts Table	
<b>Core Specifics</b>	
Supported Device Family <sup>(1)</sup>	Virtex-6 <sup>(2)</sup> , Spartan-6 <sup>(3)</sup>
Supported User Interfaces	AXI-Stream, AXI4-Lite
<b>Resources Used</b>	
See <a href="#">Table 106</a> and <a href="#">Table 107</a>	
<b>Frequency</b>	
See <a href="#">Table 108</a>	
<b>Provided with Core</b>	
Documentation	Product Specification
Design Files	Verilog, VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Xilinx <a href="#">Answer 37174</a>
Simulation Model	N/A
<b>Tested Design Tools</b>	
Design Entry Tools	12.4 EDK
Simulation	ModelSim PE/SE 6.5c
Synthesis Tools	XST.
<b>Support</b>	
Provided by Xilinx, Inc.	

### Notes:

1. For a listing of supported devices, see the [release notes](#) for this core.
2. For more information on the Virtex-6 devices, see the [DS150 Virtex-6 Family Overview](#).
3. For more information on the Spartan-6 devices, see the [DS160 Spartan-6 Family Overview](#).

## Features (continued)

- Support for Pause frames for flow control
- Optional extended filtering for multicast frames
- Optional TX and RX statistics gathering
- Auto PAD and FCS field insertion or pass through on transmit
- Auto PAD and FCS field stripping or pass through on receive Ethernet Audio Video Bridging (AVB) at 100/1000Mbps
- Ethernet Audio Video Bridging (AVB) at 100/1000 Mbps (Additional license required)

## Known Issues

Please reference the change log for known issues.

## How To Use This Document

Some of the information in this document is identical or very similar for all modes of the AXI Ethernet. The first sections of this document will provide that information. In the cases where slight differences occur for a particular mode, footnotes will call attention to the variance.

Other information in this document is specific to either the type of TEMAC or PHY interface selected. Following the sections containing the common information will be sections specific to Virtex-6 FPGA Hard TEMAC and Soft TEMAC implementations.

Within these sections will be separate sections for each of the supported PHY interfaces.

## Functional Description

An AXI Ethernet provides additional functionality and ease of use to the Hard TEMAC silicon component that is built into some Virtex-6 devices while providing a soft Ethernet MAC option for all of the devices types that are supported. The main AXI Ethernet core uses several “helper” cores as needed for user selected functions.

The soft TEMAC is based on the Xilinx Coregen Tri Mode Ethernet MAC LogiCORE. The soft Ethernet 1000Base-X PCS/PMA or SGMII core is based on the Xilinx Coregen Ethernet 1000Base-X PCS/PMA or SGMII LogiCORE™. The Virtex-6 FPGA TEMAC is based on the Xilinx Coregen Virtex-6 Embedded Tri Mode Ethernet MAC LogiCORE™. The statistics function is based on the Xilinx Coregen Ethernet Statistics LogiCORE™. The Ethernet AVB Endpoint is based on the Xilinx Coregen Ethernet AVB Endpoint LogiCORE™.

A high level block diagram of the AXI Ethernet IP core is shown in [Figure 1](#). When the AXI Ethernet is used with the Virtex-6 FPGA hard TEMAC mode only, the core is free and does not require a license key.

When the AXI Ethernet is used with the soft TEMAC mode or Ethernet AVB endpoint mode, it will operate in an evaluation mode to allow users to determine if they would like to purchase a license for the full version of the core.

During evaluation modes, the core is fully functional, but will only operate for several hours before requiring a reset to continue.

For more information on the Virtex-6 FPGA Hard TEMAC silicon component, see [UG368 Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide](#). For more information on the soft Tri Mode Ethernet MAC LogiCORE, see the [UG138 LogiCORE Tri-Mode Ethernet MAC User Guide](#). For more information on the soft Ethernet 1000Base-X PCS/PMA or SGMII LogiCORE, see [UG155 LogiCORE™ IP Ethernet 1000Base-X PCS/PMA or SGMII User Guide](#).

For more information on the Ethernet statistics LogiCORE, see the [UG170 LogicCORE IP Ethernet Statistics User Guide](#). For more information on the Ethernet AVB Endpoint LogiCORE™, please refer to the *LogicCORE™ IP Ethernet AVB Endpoint User Guide* [UG492](#).

Please note that the links to the documents above are updated over time and may not match the version that is used in AXI Ethernet. Please refer to the [Reference Documents](#) section at the end of document to determine the version of cores used at the time this core was released.

AXI Ethernet provides an AXI4-Lite bus interface for a simple connection to the MicroBlaze processor core to allow access to the registers.

The AXI4-Stream 32-bit buses are provided for moving transmit and receive Ethernet data to and from AXI Ethernet. These buses are designed to be used with a soft DMA IP core or any other custom logic in any supported device. The AXI4-Stream buses are designed to provide support for TCP/UDP partial checksum off load in hardware if that function is required. The AXI4-Stream buses will be described later in this document.

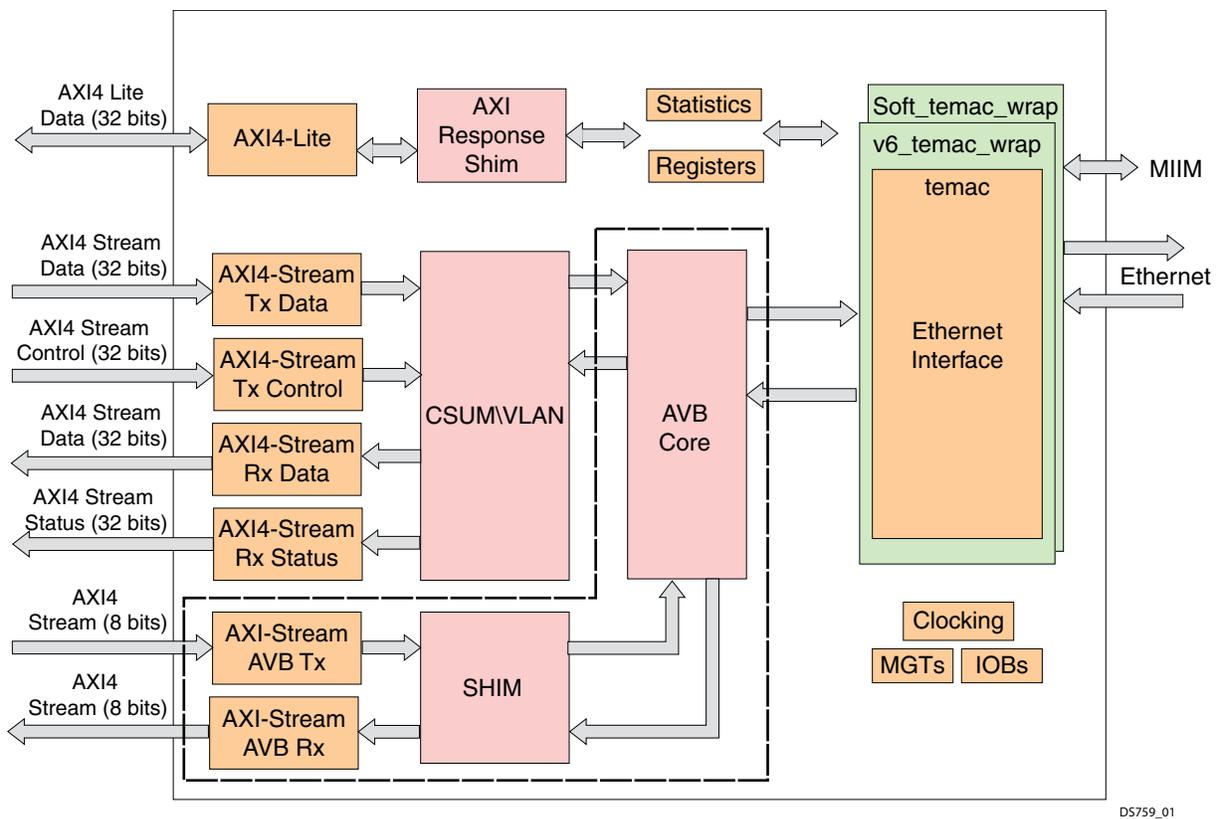


Figure 1: Block Diagram for the AXI Ethernet

Support for many PHY interfaces is included and is selected with parameters at build time. The PHY interface support varies based on the Ethernet MAC type selected. Please refer to [Table 1](#) and [Table 2](#).

Table 1: PHY Support Based on Hard TEMAC and Mode Selected

PHY Interface	Hard TEMAC		
	Full Duplex		
	10Mbps	100Mbps	1000Mbps
MII <sup>(1)</sup>	Yes	Yes	No

Table 1: PHY Support Based on Hard TEMAC and Mode Selected (Cont'd)

Hard TEMAC			
PHY Interface	Full Duplex		
	10Mbps	100Mbps	1000Mbps
GMI <sup>(2)</sup>	Yes	Yes	Yes
RGMI v1.3	Yes	Yes	Yes
RGMI v2.0	Yes	Yes	Yes
SGMII	Yes	Yes	Yes
1000Base-X	No	No	Yes

**Notes:**

1. Virtex-6 devices support MII at 2.5 V only; Spartan<sup>®</sup>-6 devices support MII at 3.3V or lower.
2. Virtex-6 devices support GMII/MII at 2.5 V only; Spartan-6 devices support GMII/MII at 3.3 V or lower.

Table 2: PHY Interface Support Based on Soft TEMAC and Mode Selected

Soft TEMAC			
PHY Interface	Full Duplex		
	10Mbps	100Mbps	1000Mbps
MII <sup>(1)</sup>	Yes	Yes	No
GMII <sup>(2)</sup>	Yes	Yes	Yes
RGMI v2.0	Yes	Yes	Yes
SGMII	Yes	Yes	Yes
1000Base-X	No	No	Yes

**Notes:**

1. Virtex-6 Devices support MII at 2.5 V only; Spartan-6 Devices support MII at 3.3 V or lower.
2. Virtex-6 Devices support GMII/MII at 2.5 V only; Spartan-6 Devices support GMII/MII at 3.3 V or lower.

Table 3: Ethernet Types Supported Based on Device Selected

C_FAMILY	Soft Ethernet	V6 Hard Ethernet
SPARTAN6	Yes	No
VIRTEX6	Yes	Yes

Some of the optional functions provided by AXI Ethernet are not compatible with other optional functions. [Figure 2](#) shows which optional functions are compatible with each other.

	Tx Csum Offload	Tx VLAN Tag	Tx VLAN Strp	Rx Csum Offload	Rx VLAN Tag	Rx VLAN Strp	Rx VLAN Trans	Rx Multicast Fitr	Ethernet AVB	Statistics
Tx Csum Offload	Y	N	N	Y	Y	Y	Y	Y	Y	Y
Tx VLAN Tag	N	Y	Y	Y	Y	Y	Y	Y	N	Y
Tx VLAN Strp	N	Y	Y	Y	Y	Y	Y	Y	N	Y
Tx VLAN Trans	N	Y	Y	Y	Y	Y	Y	Y	N	Y
Rx Csum Offload	Y	Y	Y	Y	N	N	N	Y	Y	Y
Rx VLAN Tag	Y	Y	Y	Y	N	Y	Y	Y	N	Y
Rx VLAN Strp	Y	Y	Y	Y	N	Y	Y	Y	N	Y
Rx VLAN Trans	Y	Y	Y	Y	N	Y	Y	Y	N	Y
Rx Multicast Fitr	Y	Y	Y	Y	Y	Y	Y	Y	N	Y
Ethernet AVB	Y	N	N	Y	N	N	N	N	Y	Y
Statistics	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

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Figure 2: Option Function Compatibility

The AXI Ethernet provides one Ethernet interface.

Access to external PHY registers is provided via a standard MII Management bus. When using the SGMII or 1000 Base-X PHY interfaces, the AXI Ethernet provides some PHY functionality and as a result also includes PHY registers which are also accessible via the MII Management bus. These registers will be described later in this document.

This core includes, as an option, logic which helps calculate TCP/UDP checksums for transmit and verify TCP/UDP checksums for receive. Using this logic can significantly increase the maximum Ethernet bus data rate while reducing utilization of the processor for Ethernet tasks. Including the checksum off load function will increase the amount of FPGA resources used for this core. The checksum information is included with each Ethernet frame passing over the AXI4-Stream interface. The checksum off load functionality can not be used at the same time as the extended VLAN functionality.

The AXI Ethernet provides memory buffering of transmit and receive Ethernet frames, thereby allowing more optimal transfer to and from the core with DMA. The number of frames that can be buffered in each direction is based on the size of each frame and the size of the memory buffer which are selected by parameters at build time. If the AXI Ethernet transmit memory buffer becomes full, it will throttle the transmit AXI4-Stream Data interface until more room is available for Ethernet frames. If the receive memory buffer becomes full, frames will be dropped until more memory buffer room is available. Receive frames that do not meet Ethernet format rules or do not satisfy receive address qualification will always be dropped.

Optional logic can be included to facilitate handling of VLAN type frames. Auto insertion, stripping, or translation of VLAN frames can be performed on transmit or receive with a number of options for choosing which frames will be altered.

Additional logic may be selected to provide additional filtering of receive frames with multicast destination addresses. The AXI Ethernet provides native support for up to four (4) multicast addresses.

Logic may be selected to gather statistics on transmit and receive frames. This logic provides 64-bit counters for many statistics about the frames passing through the TEMAC core.

Ethernet AVB support is available with an additional license and is supported at 100 Mbps or 1000 Mbps implementations.

## I/O Signals

The signals are listed and described in [Table 4](#).

**Table 4: I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
<b>AXI4-Lite Slave Signals</b>				
S_AXI_ACLK	AXI4-Lite	I		Clock
S_AXI_ARESETN <sup>(1)</sup>	AXI4-Lite	I		Reset (active low)
S_AXI_AWADDR(C_S_AXI_ADDR_WIDTH-1:0)	AXI4-Lite	I		Write address
S_AXI_AWVALID	AXI4-Lite	I		Write address valid: Indicates a valid write address and control information is available
S_AXI_AWREADY	AXI4-Lite	O		Write address ready: Slave is ready to accept address and control information
S_AXI_WDATA(C_S_AXI_DATA_WIDTH-1:0)	AXI4-Lite	I		AXI write data bus
S_AXI_WSTRB(C_S_AXI_DATA_WIDTH/8)-1:0	AXI4-Lite	I		Write strobes: Indicates which byte lanes have valid data. S_AXI_WSTRB[n] corresponds to S_AXI_WDATA[(8xn)]+7:(8xn)]
S_AXI_WVALID	AXI4-Lite	I		Write valid: Indicated valid write data and strobes are available. 1 = write data and strobes available 0 = write data and strobes not available
S_AXI_WREADY	AXI4-Lite	O		Write ready: Indicates the slave can accept the write data 1= slave ready 0 = slave not ready
S_AXI_BRESP(1:0)	AXI4-Lite	O		Write response: Indicates the status of the write transaction
S_AXI_BVALID	AXI4-Lite	O		Write response valid: Indicates a valid write response is available 1= write response available 0 = write response not available
S_AXI_BREADY	AXI4-Lite	I		Response ready: Indicates the master can accept the response information 1 = master ready 0 = master not ready
S_AXI_ARADDR(C_S_AXI_ADDR_WIDTH-1:0)	AXI4-Lite	I		Read address
S_AXI_ARVALID	AXI4-Lite	I		Read address valid: When HIGH this signal indicates the read address and control information is valid and will remain valid until S_AXI_ARREADY is HIGH 1 = Address and control information valid 0= Address and control information not valid

**Table 4: I/O Signal Description (Cont'd)**

Signal Name	Interface	Signal Type	Init Status	Description
S_AXI_ARREADY	AXI4-Lite	O		Address ready: Indicates the slave is ready to accept an address and associated control signals
S_AXI_RDATA(C_S_AXI_DATA_WIDTH-1:0)	AXI4-Lite	O		Read data.
S_AXI_RRESP(1:0)	AXI4-Lite	O		Read response: Indicates the status of the read transaction.
S_AXI_RVALID	AXI4-Lite	O		Read data valid: Indicates the read data is available and the read transfer can complete 1 = read data available 0 = read data not available
S_AXI_RREADY	AXI4-Lite	I		Read ready: Indicates the master can accept the read data and response information 1 = master ready 0 = master not ready
<b>AXI4-Stream Transmit Data Signals</b>				
AXI_STR_TXD_ACLK	AXI4-Stream TxD	I		AXI4-Stream Transmit Data Clock
AXI_STR_TXD_ARESETN <sup>(1)</sup>	AXI4-Stream TxD	I		AXI4-Stream Transmit Data Reset
AXI_STR_TXD_TVALID	AXI4-Stream TxD	I		AXI4-Stream Transmit Data Valid
AXI_STR_TXD_TREADY	AXI4-Stream TxD	O		AXI4-Stream Transmit Data Ready
AXI_STR_TXD_TLAST	AXI4-Stream TxD	I		AXI4-Stream Transmit Data Last Word
AXI_STR_TXD_TSTRB(3:0)	AXI4-Stream TxD	I		AXI4-Stream Transmit Data Valid Strobes
AXI_STR_TXD_TDATA(31:0)	AXI4-Stream TxD	I		AXI4-Stream Transmit Data bus
<b>AXI4-Stream Transmit Control Signals</b>				
AXI_STR_TXC_ACLK	AXI4-Stream TxC	I		AXI4-Stream Transmit Control Clock
AXI_STR_TXC_ARESETN <sup>(1)</sup>	AXI4-Stream TxC	I		AXI4-Stream Transmit Control Reset
AXI_STR_TXC_TVALID	AXI4-Stream TxC	I		AXI4-Stream Transmit Control Valid
AXI_STR_TXC_TREADY	AXI4-Stream TxC	O		AXI4-Stream Transmit Control Ready
AXI_STR_TXC_TLAST	AXI4-Stream TxC	I		AXI4-Stream Transmit Control Last Word
AXI_STR_TXC_TSTRB(3:0)	AXI4-Stream TxC	I		AXI4-Stream Transmit Control Valid Strobes
AXI_STR_TXC_TDATA(31:0)	AXI4-Stream TxC	I		AXI4-Stream Transmit Control bus
<b>AXI4-Stream Receive Data Signals</b>				

**Table 4: I/O Signal Description (Cont'd)**

Signal Name	Interface	Signal Type	Init Status	Description
AXI_STR_RXD_ACLK	AXI4-Stream RxD	I		AXI4-Stream Receive Data Clock
AXI_STR_RXD_ARESETN <sup>(1)</sup>	AXI4-Stream RxD	I		AXI4-Stream Receive Data Reset
AXI_STR_RXD_TVALID	AXI4-Stream RxD	O		AXI4-Stream Receive Data Valid
AXI_STR_RXD_TREADY	AXI4-Stream RxD	I		AXI4-Stream Receive Data Ready
AXI_STR_RXD_TLAST	AXI4-Stream RxD	O		AXI4-Stream Receive Data Last Word
AXI_STR_RXD_TSTRB(3:0)	AXI4-Stream RxD	O		AXI4-Stream Receive Data Valid Strobes
AXI_STR_RXD_TDATA(31:0)	AXI4-Stream RxD	O		AXI4-Stream Receive Data bus
<b>AXI4-Stream Receive Control Signals</b>				
AXI_STR_RXS_ACLK	AXI4-Stream RxC	I		AXI4-Stream Receive Control Clock
AXI_STR_RXS_ARESETN <sup>(1)</sup>	AXI4-Stream RxC	I		AXI4-Stream Receive Control Reset
AXI_STR_RXS_TVALID	AXI4-Stream RxC	O		AXI4-Stream Receive Control Valid
AXI_STR_RXS_TREADY	AXI4-Stream RxC	I		AXI4-Stream Receive Control Ready
AXI_STR_RXS_TLAST	AXI4-Stream RxC	O		AXI4-Stream Receive Control Last Word
AXI_STR_RXS_TSTRB(3:0)	AXI4-Stream RxC	O		AXI4-Stream Receive Control Valid Strobes
AXI_STR_RXS_TDATA(31:0)	AXI4-Stream RxC	O		AXI4-Stream Receive Control bus
<b>AXI4-Stream Ethernet AVB Transmit Data Signals</b>				
AXI_STR_AVBTX_ACLK	AXI4-Stream AvTx	I		AXI4-Stream AVB Transmit Data Clock
AXI_STR_AVBTX_ARESETN	AXI4-Stream AvTx	I		AXI4-Stream AVB Transmit Data Reset
AXI_STR_AVBTX_TVALID	AXI4-Stream AvTx	I		AXI4-Stream AVB Transmit Data Valid
AXI_STR_AVBTX_TREADY	AXI4-Stream AvTx	O		AXI4-Stream AVB Transmit Data Ready
AXI_STR_AVBTX_TLAST	AXI4-Stream AvTx	I		AXI4-Stream AVB Transmit Data Last Word
AXI_STR_AVBTX_TDATA(7:0)	AXI4-Stream AvTx	I		AXI4-Stream AVB Transmit Data bus
AXI_STR_AVBTX_TUSER(0:0)	AXI4-Stream AvTx	I		AXI4-Stream AVB Transmit User defined signal
<b>AXI4-Stream Ethernet AVB Receive Data Signals</b>				

Table 4: I/O Signal Description (Cont'd)

Signal Name	Interface	Signal Type	Init Status	Description
AXI_STR_AVBRX_ACLK	AXI4-Stream AvRx	O		AXI4-Stream AVB Receive Data Clock
AXI_STR_AVBRX_ARESETN	AXI4-Stream AvRx	I		AXI4-Stream AVB Receive Data Reset
AXI_STR_AVBRX_TVALID	AXI4-Stream AvRx	O		AXI4-Stream AVB Receive Data Valid
AXI_STR_AVBRX_TLAST	AXI4-Stream AvRx	O		AXI4-Stream AVB Receive Data Last Word
AXI_STR_AVBRX_TDATA(7:0)	AXI4-Stream AvRx	O		AXI4-Stream AVB Receive Data bus
AXI_STR_AVBRX_TUSER(0:0)	AXI4-Stream AvRx	O		Receive channel User information used to indicate good (active LOW) / bad (active HIGH) frame indication during
<b>Other Ethernet AVB Signals</b>				
RTC_CLK	AVB	I		Reference clock used to increment the Real Time Clock.
<b>Ethernet AVB Interrupt Signals</b>				
AV_INTERRUPT_10MS	AVB	O		This interrupt is asserted every 10 ms as a measure by the RTC. This is used as a timer for the PTP software algorithms.
AV_INTERRUPT_PTP_TX	AVB	O		This is asserted following the transmission of any PTP packet from the Tx PTP packet buffers. Following this interrupt, the software is required to record the Tx Frame Time Stamp.
AVI_INTERRUPT_PTP_RX	AVB	O		This is asserted following the transmission of any PTP packet from the Rx PTP packet buffers. Following this interrupt, the software is required to record the Rx Frame Time Stamp.
<b>Reference signals may be used for 1722 logic, etc.</b>				
AV_RTC_NANOSECFIELD_172(31:0)	AVB	O		The synchronized nanosecond field from the RTC.
AV_RTC_SECFIELD(47:0)	AVB	O		The synchronized second field from the RTC
AV_CLK_8K	AVB	O		A 8 KHz clock which is derived from and is synchronized to the RTC. The period of this clock, 125us, marks the isochronous cycle.
AV_RTC_NANOSECFIELD_1722(31:0)	AVB	O		The IEEE1722 specification contains a different format for the RTC which is provided here as an extra port. This is derived from and synchronized with the IEEE802.1 AS RTC.
<b>System Signals</b>				
INTERRUPT	System	O	0	Interrupt indicator for core
<b>Ethernet System Signals</b>				
PHY_RST_N	Ethernet	O	0	TEMAC to PHY reset signal: This active LOW reset is held active for 10 ms after power is applied and during any reset. After the reset goes inactive, the PHY cannot be accessed for an additional 5 ms.

**Table 4: I/O Signal Description (Cont'd)**

Signal Name	Interface	Signal Type	Init Status	Description
REFCLK	Ethernet	I		200 MHz input clock on global clock routing used for signal delay primitives for all GMII and RGMII PHY modes.
GTX_CLK <sup>(2)</sup>	Ethernet	I		The 125 MHz clock used in all MII, GMII, RGMII, and SGMII configurations to control the PHY reset requirements. In addition to this, it is a 125 MHz input clock on global clock routing used to derive the other transmit clocks for all GMII and RGMII PHY modes. For soft TEMAC MII PHY systems, this clock must be driven by some clock (does not need to be 125 MHz). The AXI4-Lite clock may be used in these cases; however, the use of a slower clock will increase the PHY reset (10 ms @ 125MHz) and the time required to wait after reset (5ms @ 125MHz) before accessing the PHY registers. This clock is also used when Ethernet Statistics are enabled with all supported device families.
MGTCLK_P	Ethernet	I		Positive polarity of differential clock used to drive GTX/GTP MGTs. Must be connected to an external, high-quality differential reference clock of frequency of 125 MHz.
MGTCLK_N	Ethernet	I		Negative polarity of differential clock used to drive GTX/GTP MGTs. Must be connected to an external, high-quality differential reference clock of frequency of 125 MHz.
<b>Ethernet MII Signals</b>				
MII_COL <sup>(3)</sup>	Ethernet bus MII	I		Collision: Half Duplex signal that when HIGH, indicates an ethernet data collision has occurred
MII_CRS <sup>(3)</sup>	Ethernet bus MII	I		Carrier sense: Half duplex signal the when asserted by the PHY indicates the transmit or receive medium is non-idle
MII_TXD(3:0)	Ethernet bus MII	O	0	TEMAC to PHY transmit data
MII_TX_EN	Ethernet bus MII	O	0	TEMAC to PHY transmit enable
MII_TX_ER	Ethernet bus MII	O	0	TEMAC to PHY transmit Error enable
MII_RXD(3:0)	Ethernet bus MII	I		PHY to TEMAC receive data
MII_RX_DV	Ethernet bus MII	I		PHY to TEMAC receive data valid indicator
MII_RX_ER	Ethernet bus MII	I		PHY to TEMAC receive error indicator
MII_RX_CLK	Ethernet bus MII	I		PHY to TEMAC receive clock
MII_TX_CLK <sup>(2)</sup>	Ethernet bus MII	I		PHY to TEMAC transmit clock (also used for GMII/MII mode)
<b>Ethernet GMII Signals</b>				

**Table 4: I/O Signal Description (Cont'd)**

Signal Name	Interface	Signal Type	Init Status	Description
GMII_COL <sup>(3)</sup>	Ethernet bus GMII	I		Collision: Half Duplex signal that when HIGH, indicates an ethernet data collision has occurred
GMII_CR <sup>(3)</sup>	Ethernet bus GMII	I		Carrier sense: Half duplex signal the when asserted by the PHY indicates the transmit or receive medium is non-idle
GMII_TXD(7:0)	Ethernet bus GMII	O	0	TEMAC to PHY transmit data
GMII_TX_EN	Ethernet bus GMII	O	0	TEMAC to PHY transmit enable
GMII_TX_ER	Ethernet bus GMII	O	0	TEMAC to PHY transmit Error enable
GMII_TX_CLK	Ethernet bus GMII	O	0	TEMAC to PHY transmit clock
GMII_RXD(7:0)	Ethernet bus GMII	I		PHY to TEMAC receive data
GMII_RX_DV	Ethernet bus GMII	I		PHY to TEMAC receive data valid indicator
GMII_RX_ER	Ethernet bus GMII	I		PHY to TEMAC receive error indicator
GMII_RX_CLK	Ethernet bus GMII	I		PHY to TEMAC receive clock
<b>Ethernet SGMII and 1000Base-X Signals</b>				
TXP	Ethernet bus SGMII and 1000Base-X	O	0	TEMAC to PHY transmit data positive
TXN	Ethernet bus SGMII and 1000Base-X	O	0	TEMAC to PHY transmit data negative
RXP	Ethernet bus SGMII and 1000Base-X	I		PHY to TEMAC receive data positive
RXN	Ethernet bus SGMII and 1000Base-X	I		PHY to TEMAC receive data negative
<b>Ethernet RGMII Signals</b>				
RGMII_TXD(3:0)	Ethernet bus RGMII	O	0	TEMAC to PHY transmit data
RGMII_TX_CTL	Ethernet bus RGMII	O	0	TEMAC to PHY transmit control
RGMII_TXC	Ethernet bus RGMII	O	0	TEMAC to PHY transmit clock
RGMII_RXD(3:0)	Ethernet bus RGMII	I		PHY to TEMAC receive data
RGMII_RX_CTL	Ethernet bus RGMII	I		PHY to TEMAC receive control

Table 4: I/O Signal Description (Cont'd)

Signal Name	Interface	Signal Type	Init Status	Description
RGMII_RXC	Ethernet bus RGMII	I		PHY to TEMAC receive clock
<b>Ethernet MII Management Interface (MIIM) Signals</b>				
MDC	Ethernet bus MIIM	O	0	TEMAC to PHY MII management bus clock
MDIO <sup>(4)</sup>	Ethernet bus MIIM	I/O	1	Tri-stateable bi-directional MII Management data bus.

**Notes:**

1. See [Reset Considerations](#).
2. See [Clock Pin Selection](#).
3. This core does not support Half Duplex operation.
4. The MDIO signal is required to be pulled HIGH via the PHY data sheet. If the MDIO interface is not used with the Soft PCS PMA core (C\_TYPE = 1 and C\_PHY\_TYPE = 4 or 5), the internal MDIO\_I signal must be tied HIGH to allow MDIO communication to the internal MAC.

## Reset Considerations

The Hard and Soft TEMAC components are reset via any of the following AXI4 reset signals: AXI\_STR\_TXD\_ARESETN, AXI\_STR\_TXC\_ARESETN, AXI\_STR\_RXD\_ARESETN, AXI\_STR\_RXS\_ARESETN, or S\_AXI\_ARESETN. This core is designed with only synchronous resets. As a consequence of this design methodology, slower clock domains will come out of reset after fast clock domains. For most systems this is not an issue, but for 10 Mbps operation, the slower tx client Ethernet core clock can be as low as 2.5 MHz. With such a slow clock and AXI4-Lite running at 125 MHz, the circuit on the 2.5 MHz clock will come out of reset up to 800 ns (or 100 AXI4-Lite clock periods) after the AXI4-Lite clock domain comes out of reset. To insure proper core behavior, the TEMAC core should not be accessed for at least 800 ns after AXI4-Lite reset.

## Clock Pin Selection

When targeting a GMII design, it uses a BUFGMUX to switch between the MII\_TX\_CLK and the GTX\_CLK. This allows for the design to support data rates of 10/100Mbps and also 1000Mbps. The FPGA pins for these clocks must be selected such that they are located in the same clock region and they are both on clock dedicated pins. The GMII status, control, and data pins must be chosen to be in the same clock region as the above mentioned clocks. Please refer to either the [UG382 Spartan-6 FPGA Clocking Resources User Guide](#) or the [UG362 Virtex-6 FPGA Clocking Resources User Guide](#) for more information. Please pay special attention to clocking conflicts. Failure to adhere to these rules will result in build errors and data integrity errors.

## Design Parameters

To allow the user to generate an AXI Ethernet that is uniquely tailored the user’s system, certain features can be parameterized in the AXI Ethernet design as shown in [Table 5](#).

## Inferred Parameters

In addition to the parameters listed in [Table 5](#), there are also parameters that are inferred for each AXI interface in the EDK tools. Through the design, these EDK-inferred parameters control the behavior of the AXI Interconnect. For a complete list of the interconnect settings related to the AXI interface, see the [DS768 AXI Interconnect IP Data Sheet](#).

Table 5: AXI Ethernet Design Parameters

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
<b>User Specified AXI Implementation Parameters</b>				
SAXI Base Address <sup>(1)</sup>	C_BASEADDR	Valid AXI Address	0xFFFFFFFF <sup>(2)</sup>	std_logic_vector
SAXI High Address <sup>(3)</sup>	C_HIGHADDR	Valid AXI Address	0x00000000 <sup>(2)</sup>	std_logic_vector
SAXI Protocol	C_S_AXI_PROTOCOL	AXI4LITE	AXI4LITE	string
<b>System Specified Slave AXI Bus Implementation Parameters</b>				
SAXI Data Bus Width <sup>(4)</sup>	C_S_AXI_DATA_WIDTH	32	32	integer
SAXI Address Bus Width <sup>(4)</sup>	C_S_AXI_ADDR_WIDTH	32	32	integer
SAXI ID Width <sup>(4)</sup>	C_S_AXI_ID_WIDTH	4	4	integer
<b>User Specified TEMAC Implementation Parameters</b>				
FPGA Device Family Selected <sup>(4)</sup>	C_FAMILY	virtex6, spartan6	virtex6	string
AXI interface clock frequency in Hertz	C_S_AXI_ACLK_FREQ_HZ	Valid AXI Frequency	100_000_000	integer
Spartan-6 MGT Transceiver to be used	C_TRANS <sup>(5)</sup>	A, B	A	string
Type of TEMAC selected	C_TYPE <sup>(6)(7)</sup>	0 = Soft TEMAC operating at 10/100Mbps 1 = Soft TEMAC operating at 10/100/1000 Mbps 2= Virtex 6 Hard	0	integer
Half Duplex <sup>(8)</sup>	C_HALFDUP	0	0	integer
INCLUDE I/O and BUFs as needed for the PHY interface selected	C_INCLUDE_IO <sup>(6)</sup>	1 = I/O included 0 = I/O not included	1	integer
PHY Interface Type	C_PHY_TYPE <sup>(6)(7)(9)(11)</sup>	0 = MII 1 = GMII/MII 2 = RGMII V1.3 3 = RGMII v2.0 4 = SGMII 5 = 1000Base-X	1	integer

**Table 5: AXI Ethernet Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
PHY Address for TEMAC	C_PHYADDR <sup>(10)</sup>	00001 - 11111	00001	std_logic_vector
Transmit BRAM depth in bytes for TEMAC	C_TXMEM	2048, 4096, 8192, 16384, 32768	4096	integer
Receive BRAM depth in bytes for TEMAC	C_RXMEM	2048, 4096, 8192, 16384, 32768	4096	integer
Transmit TCP/UDP Checksum off load	C_TXCSUM	0 = Tx CSUM unused 1 = Partial Tx CSUM used	0	integer
Receive TCP/UDP Checksum off load	C_RXCSUM	0 = Rx CSUM unused 1 = Partial Rx CSUM used	0	integer
Transmit VLAN tagging	C_TXVLAN_TAG	1 = Tx VLAN tagging used 0 = Tx VLAN tagging unused	0	integer
Receive VLAN tagging	C_RXVLAN_TAG	1 = Rx VLAN tagging used 0 = Rx VLAN tagging unused	0	integer
Transmit VLAN translation	C_TXVLAN_TRAN	1 = Tx VLAN translation used 0 = Tx VLAN translation unused	0	integer
Receive VLAN translation	C_RXVLAN_TRAN	1 = Rx VLAN translation used 0 = Rx VLAN translation unused	0	integer
Transmit VLAN stripping	C_TXVLAN_STRP	1 = Tx VLAN stripping used 0 = Tx VLAN stripping unused	0	integer
Receive VLAN stripping	C_RXVLAN_STRP	1 = Rx VLAN stripping used 0 = Rx VLAN stripping unused	0	integer
Extended Multicast address filtering for RX	C_MCAST_EXTEND	1 = Extended multicast filtering used 0 = Extended multicast filtering unused	0	integer
Statistic gathering	C_STATS	1 = Statistics gathering used 0 = Statistics gathering unused	0	integer
Ethernet Audio Video Bridging (AVB) mode	C_AVB	1 = Ethernet AVB mode used 0 = Ethernet AVB mode unused	0	integer

Table 5: AXI Ethernet Design Parameters

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
Simulation parameter	C_SIMULATION	0 = Hardware build 1= Reduce simulation reset time in some configurations	0	integer

**Notes:**

1. C\_BASEADDR must start on an address boundary that is an integer multiple of 262,144 (256K). For example, valid settings are 0x00000000, 0x00040000, 0x00080000, etc
2. The default value will insure that the actual value is set. For example, if the value is not set, a compiler error will be generated. The address range must be at least 0x00040000.
3. C\_HIGHADDR is required to be at least C\_BASEADDR + 262,143 to provide space for the 32-bit addresses used by the registers and memory. For example: C\_BASEADDR= 0x00000000 and C\_HIGHADDR = 0x0003FFFF
4. These parameters are calculated and automatically assigned by the tools during the system creation process.
5. This parameter is used only for C\_TYPE = 1 and C\_PHY\_TYPE= 4 or 5.
6. The C\_INCLUDE\_IO parameter does not have any effect when the Soft TEMAC 1000Base-X PCS/PMA or SGMII core is selected (C\_TYPE = 1 and C\_PHY\_TYPE = 4 or 5). When the Soft TEMAC 1000Base-X PCS/PMA or SGMII core is selected, the necessary connections are made.
7. When C\_TYPE is set to 0, C\_PHY\_TYPE must also be set to 0
8. This core does not support Half Duplex
9. See Table 1 and Table 2 for the PHY types and data rates supported for full duplex operation of the Hard and Soft TEMAC cores.
10. The value "00000" is a broadcast PHY address and should not be used to avoid contention between the internal TEMAC PHYs and the external PHY(s)
11. See table footnote 4 in Table 4 for MDIO communication for the Soft PCS PMA TEMAC.

## Allowable Parameter Combinations

Please refer to Table 1, Table 2, Table 3, and Figure 2 for parameter combination restrictions.

## Memory and Register Descriptions

The AXI Ethernet contains memory and addressable registers for read and write operations as shown in Table 6. All register are directly accessible. The base address for the directly addressable registers is set in the parameter C\_BASEADDR. All reserved address spaces indicated in Table 6 below will return zeros when read.

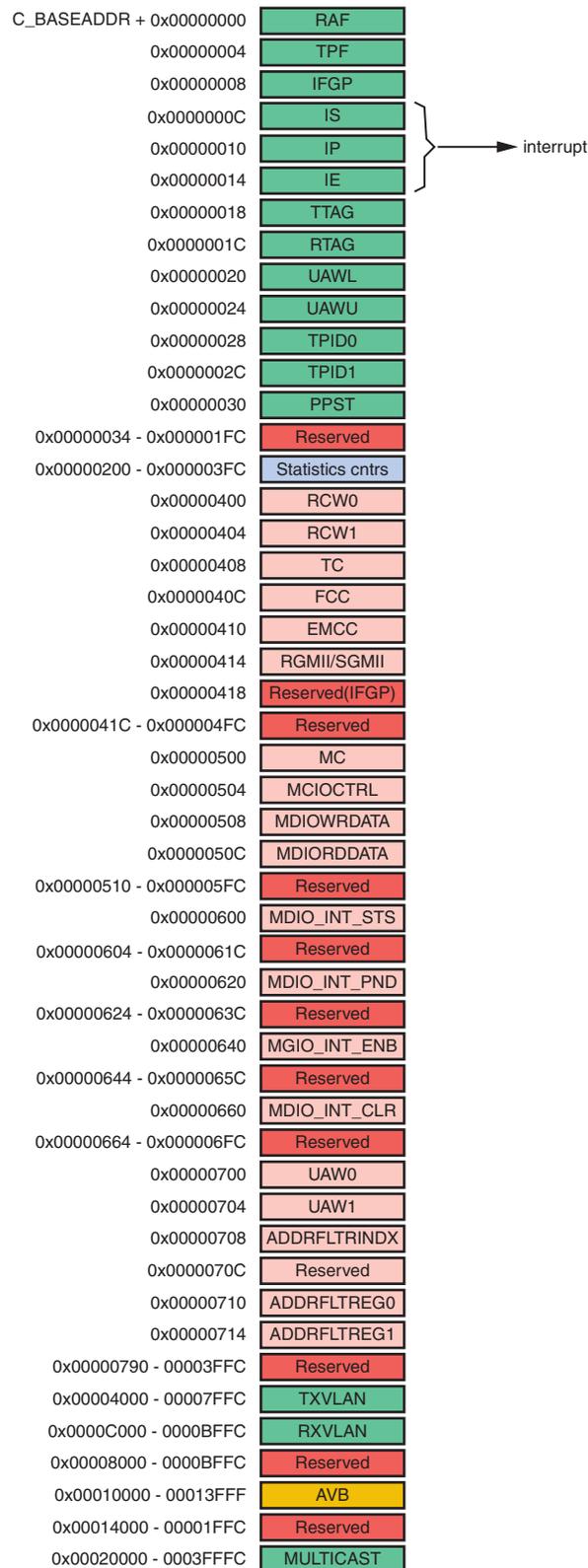
**Table 6: AXI4-Lite Addressable Memory and Soft Registers**

Register Name	AXI4-Lite Address (offset from C_BASEADDR)	Access
Reset and Address Filter Register TEMAC (RAF)	0x00000000	Read/Write
Transmit Pause Frame TEMAC (TPF)	0x00000004	Read/Write
Transmit Inter Frame Gap Adjustment TEMAC (IFGP)	0x00000008	Read/Write
Interrupt Status Register TEMAC (IS)	0x0000000C	Read/Write
Interrupt Pending Register TEMAC (IP)	0x00000010	Read
Interrupt Enable Register TEMAC (IE)	0x00000014	Read/Write
Transmit VLAN Tag TEMAC (TTAG)	0x00000018	Read/Write
Receive VLAN Tag TEMAC (RTAG)	0x0000001C	Read/Write
Unicast Address Word Lower TEMAC (UAWL)	0x00000020	Read/Write
Unicast Address Word Upper TEMAC (UAWU)	0x00000024	Read/Write
VLAN TPID TEMAC Word 0 (TPID0)	0x00000028	Read/Write
VLAN TPID TEMAC Word 1 (TPID1)	0x0000002C	Read/Write
PCS PMA Soft TEMAC Status Register (PPST)	0x00000030	Read
Reserved	0x00000034-0x000001FC	Reserved
Statistics Counters	0x00000200 - 0x000003FC	Read
TEMAC Receive Configuration Word 0 Register (RCW)	0x00000400	Read/Write
TEMAC Receive Configuration Word 1 Register (RCW)	0x00000404	Read/Write
TEMAC Transmitter Configuration Register (TC)	0x00000408	Read/Write
TEMAC Flow Control Configuration Register (FCC)	0x0000040C	Read/Write
TEMAC Ethernet MAC Mode Configuration Register (EMMC)	0x00000410	Read except bits 30 and 31 which are Read/Write
RGMII/SGMII Configuration (Hard TEMAC only)	0x00000414	Reserved
Reserved (IFG)	0x00000418	Reserved
Reserved	0x0000041C-0x000004FC	Reserved
MII Management Configuration Register	0x00000500	Read/Write
MII Management Control	0x00000504	Read/Write
MII Management Write Data	0x00000508	Read/Write
MII Management Read Data	0x0000050C	Read
Reserved	0x00000510-0x000005FC	Reserved
MDIO Interrupt Status Register (MIS)	0x00000600	Read/Write
Reserved	0x00000604-0x0000061C	Reserved
MDIO Interrupt Pending Register (MIP)	0x00000620	Read
Reserved	0x00000624-0x0000063C	Reserved
MDIO Interrupt Enable Register (MIE)	0x00000640	Read/Write
Reserved	0x00000644-0x0000065C	Reserved
MDIO Interrupt Clear Register (MIC)	0x00000660	Read/Write

**Table 6: AXI4-Lite Addressable Memory and Soft Registers (Cont'd)**

<b>Register Name</b>	<b>AXI4-Lite Address (offset from C_BASEADDR)</b>	<b>Access</b>
Reserved	0x00000664-0x000006FC	Reserved
TEMAC Unicast Address Word 0 Register (UAW0)	0x00000700	Read/Write
TEMAC Unicast Address Word 1 Register (UAW1)	0x00000704	Read/Write
Filter Mask Index	0x00000708	Read/Write
Reserved	0x0000070C	Reserved
Address Filter (31:0)	0x00000710	Read/Write
Address Filter (47:32)	0x00000714	Read/Write
Reserved	0x00000718 - 0x0000078C	Read/Write
Reserved	0x00000790-0x00000FFC	Reserved
Reserved	0x00001000-0x00003FFC	Reserved
Transmit VLAN Data Table TEMAC	0x00004000 - 0x00007FFC	Read/Write
Receive VLAN Data Table TEMAC	0x00008000 - 0x0000BFFC	Read/Write
Reserved	0x0000C000-0x0000FFFC	Reserved
Ethernet AVB	0x00010000-0x00013FFC	Read/Write
Reserved	0x00014000-0x0001FFFC	Reserved
Multicast Address Table TEMAC	0x00020000 - 0x0003FFFC	Read/Write

## Addressable Memory



DS759\_03

Figure 3: Address Mapping Diagram

### Reset and Address Filter Registers (RAF) - Offset 0x0000\_0000

The Reset and Address Filter (RAF) Register is shown in Figure 4. This register allows the software to block receive multicast and broadcast Ethernet frames. Additional receive address filtering is provided with the registers in Table 38 and Table 39.

The multicast reject bit provides a means of blocking receive multicast Ethernet frames without having to clear out any multicast address values stored in the multicast address table. It also provides a means for allowing more than four multicast addresses to be received (the limit of the multicast address table). To accept more than four multicast addresses, the FMI register would be set to promiscuous mode and the multicast reject bit of this register set to allow multicast frames. Note that software may also need to filter out additional receive frames with other addresses.

The broadcast reject bit provides the only means for rejecting receive broadcast Ethernet frames.

As additional functionality was added to the core, this register became the convenient location for new bits to control those new functions. Care has been taken to minimize the effect of these new bits on existing applications by ensuring that the default values of these bits disable new functionality which will ensure that when applications do not use the new bits, the core will operate the way it did previously.

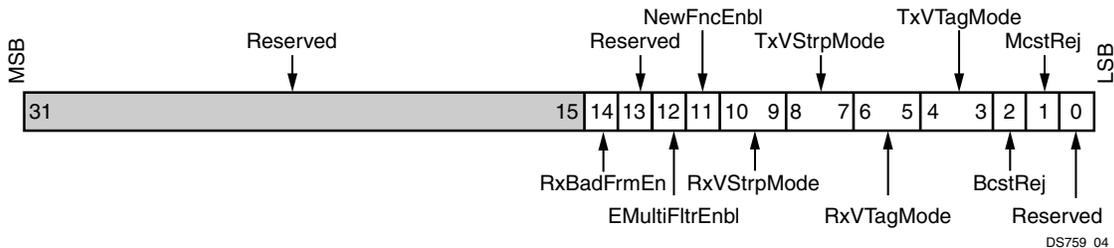


Figure 4: Reset and Address Filter Registers (offset 0x0000\_0000)

Table 7 shows the Reset and Address Filter Register bit definitions.

Table 7: Reset and Address Filter Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 15	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
14	RxBadFrmEn	Read/Write	0	<b>Receive Bad Frame Enable.</b> This bit provides a means for allowing bad receive frames to be accepted and passed to the RX AXI4-Stream interface as if they were good frames. 0 - Normal operation, bad frames will be rejected. 1 - Bad frames will be accepted.
13	Reserved	Read	0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
12	EMultiFiltrEnbl	Read/Write	0	<b>Enhanced Multicast Filter Enable:</b> This bit provides a simple way to disable the new enhanced multicast filtering if present. This is necessary if promiscuous address reception mode is desired or if use of the built-in 4 TEMAC multicast address registers is required when the core includes the enhanced multicast address filtering function enabled at build time by the C_MCAST_EXTEND parameters. Please refer to the Enhanced Multicast Filtering section of this document for more details. 0 - disable enhanced multicast address filtering mode 1 - enable enhanced multicast address filtering mode if present

Table 7: Reset and Address Filter Register Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
11	NewFncEnbl	Read/Write	0	<p><b>New Functions Enable:</b> This bit provides a simple way to disable new functions that have been added in this version. This includes the VLAN tagging, VLAN stripping, VLAN translation, and extended multicast filtering. Enabling the new functions will only affect operation if the functions have been added to the design using the appropriate parameters at build-time.</p> <p>0 - disable new functions 1 - enable new functions if present</p>
10 - 9	RxVStrpMode	Read/Write	00	<p><b>Receive VLAN Strip Mode:</b> These bits select the operation mode for receive VLAN stripping and are only used when C_RXVLAN_STRP = 1. Valid VLAN TPID values must be initialized in the TPID0 and TPID1 registers. For mode 11, the Receive VLAN data table must be initialized. Please refer to the VLAN section of this document for more details.</p> <p>00 - No VLAN tags will be stripped from receive frames 01 - One VLAN tag will be stripped from all receive frames that have VLAN tags 10 - Reserved 11 - One VLAN tag will be stripped from select receive frames that already have VLAN tags</p>
8 - 7	TxVStrpMode	Read/Write	00	<p><b>Transmit VLAN Strip Mode:</b> These bits select the operation mode for transmit VLAN stripping and are only used when C_TXVLAN_STRP = 1. Valid VLAN TPID values must be initialized in the TPID0 and TPID1 registers. For mode 11, the Transmit VLAN data table must be initialized. Please refer to the VLAN section of this document for more details.</p> <p>00 - No VLAN tags will be stripped from transmit frames 01 - One VLAN tag will be stripped from all transmit frames that have VLAN tags 10 - Reserved 11 - One VLAN tag will be stripped from select transmit frames that already have VLAN tags</p>
6 - 5	RxVTagMode	Read/Write	00	<p><b>Receive VLAN Tag Mode:</b> These bits select the operation mode for receive VLAN tagging and are only used when C_RXVLAN_TAG = 1. The VLAN tag that is added is from the RTAG register. Valid VLAN TPID values must be initialized in the TPID0 and TPID1 registers. For mode 11, the Receive VLAN data table must be initialized. Please refer to the VLAN section of this document for more details.</p> <p>00 - No VLAN tags will be added to receive frames 01 - VLAN tags will be added to all receive frames 10 - VLAN tags will be added to all receive frames that already have a VLAN tag 11 - VLAN tags will be added to select receive frames that already have VLAN tags</p>
4 - 3	TxVTagMode	Read/Write	00	<p><b>Transmit VLAN Tag Mode:</b> These bits select the operation mode for transmit VLAN tagging and are only used when C_TXVLAN_TAG = 1. The VLAN tag that is added is from the TTAG register. Valid VLAN TPID values must be initialized in the TPID0 and TPID1 registers. For mode 11, the Transmit VLAN data table must be initialized. Please refer to the VLAN section of this document for more details.</p> <p>00 - No VLAN tags will be added to transmit frames 01 - VLAN tags will be added to all transmit frames 10 - VLAN tags will be added to all transmit frames that already have a VLAN tag 11 - VLAN tags will be added to select transmit frames that already have VLAN tags</p>

Table 7: Reset and Address Filter Register Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
2	BcstRej	Read/Write	0	<b>Reject Receive Broadcast Destination Address:</b> This bit provides a means for accepting or rejecting broadcast Ethernet frames. 0 - accept receive broadcast destination address Ethernet frames 1 - reject all receive broadcast destination address Ethernet frames. This is the only method available for blocking broadcast Ethernet frames
1	McstRej	Read/Write	0	<b>Reject Receive Multicast Destination Address:</b> This bit provides a means for accepting or rejecting multicast Ethernet frames. 0 - accept receive multicast destination address Ethernet frames that meet address filtering specified in FMI register and/or the multicast address table 1 - reject all receive multicast destination address Ethernet frames regardless of FMI register and multicast address table
0	Reserved	Read	0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.

### Transmit Pause Frame Registers (TPF) - Offset 0x0000\_0004

The Transmit Pause Frame TEMAC Register is shown in Figure 5. This register provides a value of pause when enabled by the FCC register (page 41). When enabled, the Ethernet will transmit a pause frame whenever this register is written. Pause values are defined in units of pause quanta which are defined as 512 bit times for the current transmission speed. Therefore, pause times may have values ranging from 0 to 65,535 \* 512 bit times.

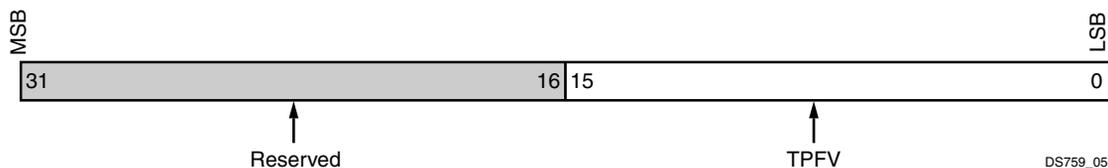


Figure 5: Transmit Pause Frame Registers (offset 0x0000\_0004)

Table 8 shows the Transmit Pause Frame Register bit definitions.

Table 8: Transmit Pause Frame register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
15 - 0	TPFV	Read/Write	0x0	<b>Transmit Pause Frame Value:</b> These bits denote the value of the transmit pause frame pause time in units of 512 bit times. If enabled by the FCC register, writing a value into this register initiates the transmission of a single pause frame with the pause value defined in this field.

### Transmit Inter Frame Gap Adjustment Registers (IFGP) - Offset 0x0000\_0008

The Transmit Inter Frame Gap Adjustment Register is shown in Figure 6. This register provides a duration value of Inter Frame Gap when enabled by the TC register (page 40). When enabled, the TEMAC will use the value of this

register to extend the Inter Frame Gap beyond the minimum of 12 idle cycles which is 96-bit times on the Ethernet Interface.

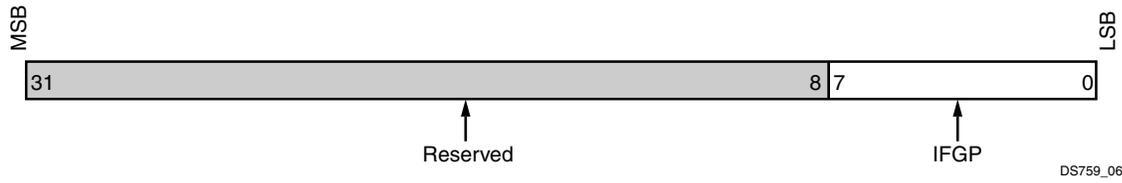


Figure 6: Transmit Inter Frame Gap Adjustment Registers (offset 0x0000\_0008)

Table 9 shows the Transmit Inter Frame Gap Adjustment Register bit definitions.

Table 9: Transmit Inter Frame Gap Adjustment Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 8	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
7 - 0	IFGP0	Read/Write	0x0	<b>Transmit Inter Frame Gap Adjustment Value:</b> This 8-bit value can be used along with the Inter Frame Gap Adjustment Enable bit of the Transmit Configuration Register ( <a href="#">TEMAC Transmit Configuration Registers (offset 0x408), page 40</a> ) to increase the Transmit Inter Frame Gap. This value is the width of the IFG in idle cycles. Each idle cycle is 8 bit times on the Ethernet interface. The minimum IFG time is 12 idle cycles which is 96 bit-times. If this field value is less than 12 or if IFGP adjustment is disabled in the Transmit Configuration register, an IFGP of 12 idle cycles (96-bit times) will be used.

### Interrupt Status Registers (IS) - Offset 0x0000\_000C

The Interrupt Status Register is shown in [Figure 7](#). This register combined with the IE, IP, MIS, and MIE registers define the interrupt interface of the AXI Ethernet. The Interrupt Status register uses one bit to represent each AXI Ethernet internal interruptible condition. One of these interruptible conditions, Hard register Access Complete (HardAcsCmplt), comes from the TEMAC component and is further defined and enabled by the MIS and MIE registers which will be described later in this document.

Once an interruptible condition occurs, it will be captured in this register (represented as the corresponding bit being set to 1) even if the condition goes away. The latched interruptible condition is cleared by writing a 1 to that bit location. Writing a 1 to a bit location that is 0 has no effect. Likewise, writing a 0 to a bit location that is 1 has no effect. Multiple bits may be cleared in a single write.

For any bit set in the Interrupt Status Register, a corresponding bit must be set in the Interrupt Enable Register for the same bit position to be set in the Interrupt pending register. Whenever any bits are set in the Interrupt Pending

Register, the INTERRUPT signal is driven active high out of the AXI Ethernet. Figure 8 shows the structure of the interrupt registers.

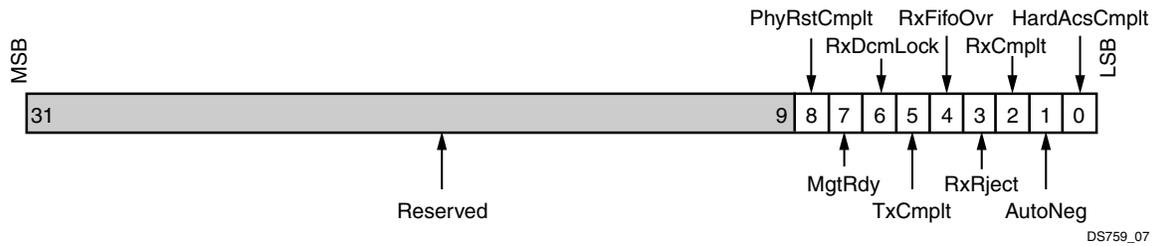


Figure 7: Interrupt Status Registers (offset 0x0000\_000C)

Table 10 shows the Interrupt Status Register bit definitions.

Table 10: Interrupt Status Register Bit Definitions

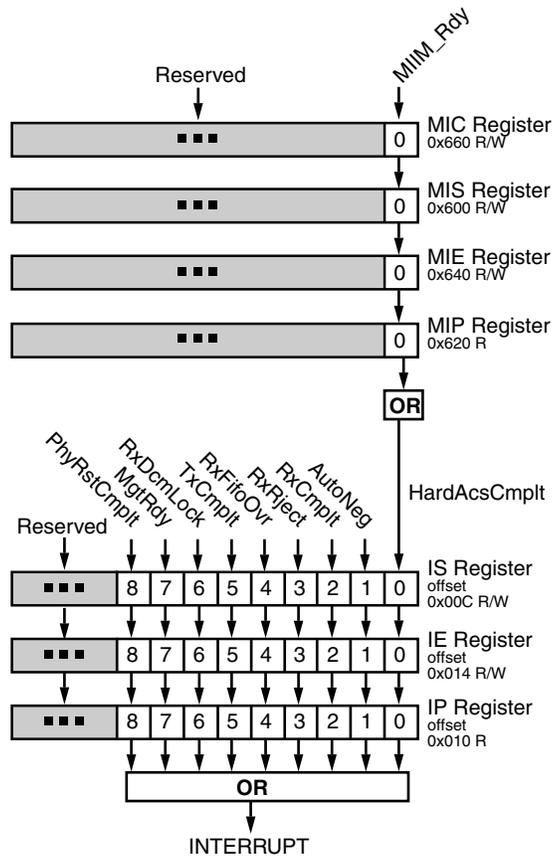
Bit(s)	Name	Core Access	Reset Value	Description
31 - 9	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
8	PhyRstCmpl	Read/Write	0	<b>PHY Reset Complete.</b> When set to “1”, this bit indicates the PHY may be accessed. This signal will not transition to “1” for 5 ms after PHY_RST_N transitions to “1”. 0 - PHY not ready 1 - PHY ready
7	MgtRdy <sup>(1)</sup>	Read/Write	0 / 1	<b>MGT Ready:</b> This bit will indicate if the TEMAC is out of reset and ready for use. In systems that use an MGT, this bit will go to “1” when the MGT is ready to use. Prior to that time, access of TEMAC registers will not complete and the core will not operate. In systems that do not use an MGT, this signal will go to “1” immediately after reset. 0 - MGT / TEMAC not ready 1 - MGT / TEMAC ready
6	RxDcmLock	Read/Write	1	<b>Receive DCM Lock:</b> No longer used, but reserved for future use. This bit will always be one. 0 - Rx DCM not locked 1 - Rx DCM Locked
5	TxCmpl	Read/Write	0	<b>Transmit Complete:</b> This bit indicates that a frame was successfully transmitted. 0 - no frame transmitted 1 - frame transmitted
4	RxMemOvr	Read/Write	0	<b>Receive Memory Overrun:</b> This bit indicates that the receive Memory overflowed while receiving an Ethernet frame. 0 - normal operation, no overflow occurred 1 - receive Memory overflow occurred and data was lost
3	RxRject <sup>(2)</sup>	Read/Write	0	<b>Receive Frame Rejected:</b> This bit indicates that a receive frame was rejected. 0 - no receive frame rejected 1 - receive frame was rejected
2	RxCmpl	Read/Write	0	<b>Receive Complete:</b> This bit indicates that a packet was successfully received. 0 - no frame received 1 - frame received

Table 10: Interrupt Status Register Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
1	AutoNeg	Read/Write	0	<b>Auto Negotiation Complete:</b> This bit indicates that auto negotiation of the SGMII or 1000 Base-X interface has completed. 0 - auto negotiation not complete 1 - auto negotiation complete
0	HardAcsCmplt	Read/Write	0	<b>Hard register Access Complete:</b> This bit indicates that an access of the TEMAC component has completed. 0 - Hard register access is not complete 1 - Hard register access is complete

**Notes:**

- This bit will reset to "0" but may change to "1" immediately after reset is removed. This bit may remain at "0" for some time in systems that are using MGTs when the MGTs are not yet ready for use.
- Please refer to [Figure 2, page 5](#) for conditions that will cause the receive frame reject interrupt to occur. The receive frame reject interrupt will occur for any of the following reasons:
  - The frame does not meet the Ethernet frame requirements as determined by the hard TEMAC core (bad FCS, bad length, etc).
  - In addition to the frame being good but not meeting the destination address filtering by the hard TEMAC, the frame also does not match one of the 4 multicast table entries, it is not a broadcast frame, it does not match the unicast address register, and the Hard TEMAC core is not in promiscuous mode.
  - The core was built to support extended multicast address filtering (C\_MCAST\_EXTEND=1), but the hard TEMAC core is not in promiscuous mode.
  - The frame is good and meets the destination address filtering by the hard TEMAC but it is a multicast frame and the multicast reject bit is set in the soft RAF register.
  - The frame is good and meets the destination address filtering by the hard TEMAC but it is a broadcast frame and the broadcast reject bit is set in the soft RAF register.



DS759\_08

Figure 8: AXI Ethernet Interrupt Structure

### Interrupt Pending Registers (IP) - Offset 0x0000\_0010

The Interrupt Pending Register is shown in Figure 9. This register combined with the IS, IE, MIS, and MIE registers define the interrupt interface of the AXI Ethernet. The Interrupt Pending register uses one bit to represent each AXI Ethernet internal interruptible condition that is represented in the Interrupt Status Register.

If one or more interrupt is latched in the Interrupt Status Register and corresponding enable bits are set in the Interrupt Enable Register, the corresponding bit is set in the Interrupt Pending Register. If one or more bits is set in the Interrupt Pending Register, the INTERRUPT signal is driven active high out of the AXI Ethernet.

The Interrupt Pending Register always represents the state of the Interrupt Status register bitwise ANDed with the IE register. The Interrupt Pending Register is read only. To clear a bit in the Interrupt Pending Register, either the corresponding bit must be cleared in either the Interrupt Status Register or in the Interrupt Enable Register.

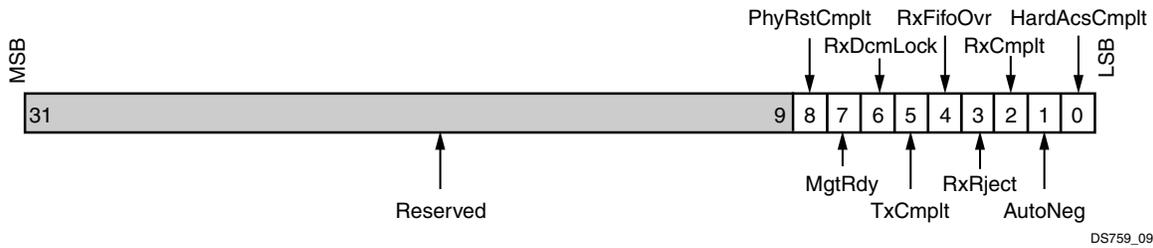


Figure 9: Interrupt Pending Registers (offset 0x0000\_0010)

Table 11 shows the Interrupt Pending Register bit definitions.

Table 11: Interrupt Pending Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 9	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
8	PhyRstCmpl	Read/Write	0	<b>PHY Reset Complete.</b> When set to “1”, this bit indicates the PHY may be accessed. This signal will not transition to “1” for 5 ms after PHY_RST_N transitions to “1”. 0 - PHY not ready 1 - PHY ready
7	MgtRdy	Read/Write	0	<b>MGT Ready:</b> This bit will indicate if the TEMAC is out of reset and ready for use. In systems that use an MGT, this bit will go to “1” when the MGT is ready to use. Prior to that time, access of TEMAC registers will not complete and the core will not operate. In systems that do not use an MGT, this signal will go to “1” immediately after reset. 0 - MGT / TEMAC not ready 1 - MGT / TEMAC ready
6	RxDcmLock	Read/Write	0	<b>Receive DCM Lock:</b> No longer used, but reserved for future use. This bit will always be one. 0 - Rx DCM not locked 1 - Rx DCM Locked
5	TxCmpl	Read/Write	0	<b>Transmit Complete:</b> This bit indicates that a frame was successfully transmitted. 0 - no frame transmitted 1 - frame transmitted
4	RxMemOvr	Read/Write	0	<b>Receive Memory Overrun:</b> This bit indicates that the receive Memory overflowed while receiving an Ethernet frame. 0 - normal operation, no overflow occurred 1 - receive Memory overflow occurred and data was lost
3	RxRjct	Read/Write	0	<b>Receive Frame Rejected:</b> This bit indicates that a receive frame was rejected. 0 - no receive frame rejected 1 - receive frame was rejected

Table 11: Interrupt Pending Register Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
2	RxCmplt	Read/Write	0	<b>Receive Complete:</b> This bit indicates that a packet was successfully received. 0 - no frame received 1 - frame received
1	AutoNeg	Read/Write	0	<b>Auto Negotiation Complete:</b> This bit indicates that auto negotiation of the SGMII or 1000 Base-X interface has completed. 0 - auto negotiation not complete 1 - auto negotiation complete
0	HardAcscmplt	Read/Write	0	<b>Hard register Access Complete:</b> This bit indicates that an access of the TEMAC component has completed. 0 - Hard register access is not complete 1 - Hard register access is complete

**Interrupt Enable Registers (IE) - Offset 0x0000\_0014**

The Interrupt Enable Register is shown in Figure 10. This register combined with the IS, IP, MIS, and MIE registers define the interrupt interface of the AXI Ethernet. The Interrupt Enable register uses one bit to represent each AXI Ethernet internal interruptible condition represented in the Interrupt Status Register.

Each bit set in the Interrupt Enable Register allows an interruptible condition bit in the Interrupt Status Register to pass through to the Interrupt Pending Register.

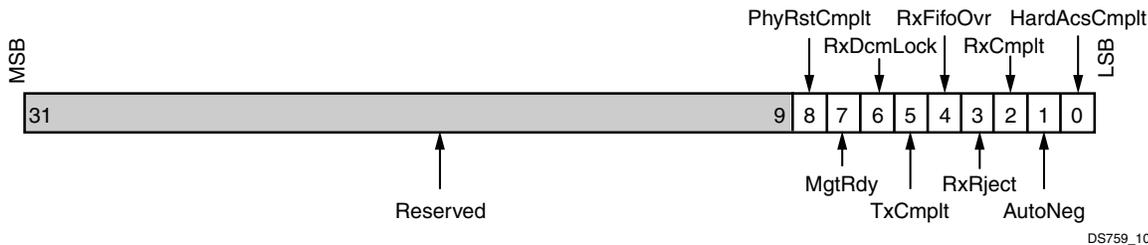


Figure 10: Interrupt Enable Registers (offset 0x0000\_0014)

Table 12 shows the Interrupt Enable Register bit definitions.

Table 12: Interrupt Enable Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 9	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
8	PhyRstCmplt	Read/Write	0	<b>PHY Reset Complete:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
7	MgtRdy	Read/Write	0	<b>MGT Ready:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
6	RxDcmLock	Read/Write	0	<b>Receive DCM Lock:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled

Table 12: Interrupt Enable Register Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
5	TxCmplt	Read/Write	0	<b>Transmit Complete:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
4	RxMemOvr	Read/Write	0	<b>Receive Memory Overrun:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
3	RxRjct	Read/Write	0	<b>Receive Frame Rejected:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
2	RxCmplt	Read/Write	0	<b>Receive Complete:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
1	AutoNeg	Read/Write	0	<b>Auto Negotiation Complete:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled
0	HardAccsCmpIt	Read/Write	0	<b>Hard register Access Complete:</b> Bit used to enable interrupt. 0 - Interrupt Disabled 1 - Interrupt Enabled

### Transmit VLAN Tag Register (TTAG) - Offset 0x0000\_0018

The Transmit VLAN Tag Register is shown in Figure 11. This register is only used when the VLAN tagging is included in the core at build-time (C\_TXVLAN\_TAG = 1). When a VLAN tag is added to a transmit frame, this is the value that is added to the frame right after the source address field. Please see the section on VLAN functions (<RD Red>"Extended VLAN Support" on page 80) for more information about how VLAN tagging is performed.

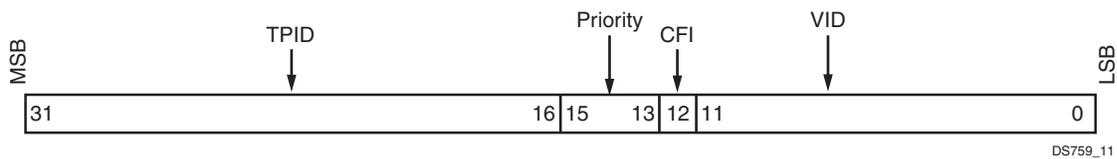


Figure 11: Transmit VLAN Tag Register (offset 0x0000\_0018)

Table 13 shows the Transmit VLAN Tag Register bit definitions.

Table 13: Transmit VLAN Tag register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	TPID	Read/Write	0x0	Tag Protocol Identifier.
15 - 13	Priority	Read/Write	0x0	User Priority.
12	CFI	Read/Write	0	Canonical Format Indicator.
11 - 0	VID	Read/Write	0x0	<b>VLAN identifier:</b> Uniquely identifies the VLAN to which the frame belongs.

### Receive VLAN Tag Register (RTAG) - Offset 0x0000\_001C

The Receive VLAN Tag Register is shown in Figure 12. This register is only used when the VLAN tagging is included in the core at build-time (C\_RXVLAN\_TAG = 1). When a VLAN tag is added to a receive frame, this is the value that is added to the frame right after the source address field. Please see the section on VLAN functions (Extended VLAN Support, page 80) for more information about how VLAN tagging is performed.

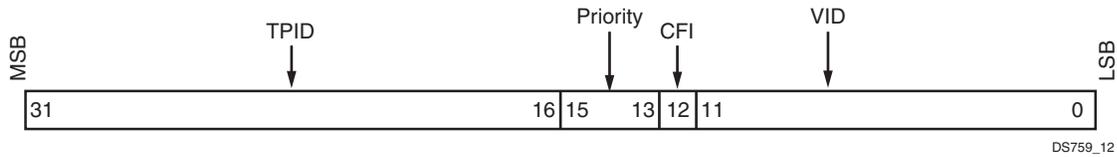


Figure 12: Receive VLAN Tag Register (offset 0x0000\_001C)

Table 14 shows the Receive VLAN Tag Register bit definitions.

Table 14: Receive VLAN Tag register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	TPID	Read/Write	0x0	Tag Protocol Identifier.
15 - 13	Priority	Read/Write	0x0	User Priority.
12	CFI	Read/Write	0	Canonical Format Indicator.
11 - 0	VID	Read/Write	0x0	<b>VLAN identifier:</b> Uniquely identifies the VLAN to which the frame belongs

### Unicast Address Word Lower Register (UAWL) - Offset 0x0000\_0020

The Unicast Address Word Lower Register is shown in Figure 13. This register and the following register are **only used when extended multicast filtering is included** in the core at build-time (C\_MCAST\_EXTEND = 1) and is enabled. These registers should not be confused with the UAW0 and UAW1 registers which are registers inside the TEMAC core which are **only used when extended multicast filtering is excluded in the core at build-time or is disabled**. When using extended multicast filtering, the TEMAC core must be placed in promiscuous address filtering mode. This register allows filtering of unicast frames not matching the address stored in these registers. Please see the section on Extended Multicast Filtering for more information (Extended Multicast Address Filtering Mode, page 73)

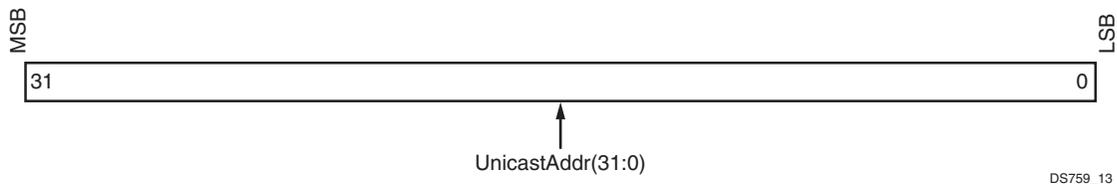


Figure 13: Unicast Address Word Lower Register (offset 0x020)

Table 15 shows the Unicast Address Word Lower Registers bit definitions.

Table 15: Unicast Address Word Lower Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	UnicastAddr	Read/Write	0x00000000	<b>Unicast Address (31:0):</b> This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

### Unicast Address Word Upper Register (UAWU) - Offset 0x0000\_0024

The Unicast Address Word Upper Register is shown in Figure 14. This register and the previous register are only used when extended multicast filtering is included in the core at build-time (C\_MCAST\_EXTEND = 1). When using extended multicast filtering, the TEMAC core must be placed in promiscuous address filtering mode. This register allows filtering of unicast frames not matching the address stored in these registers. Please see the section on Extended Multicast Filtering for more information (Extended Multicast Address Filtering Mode, page 73).

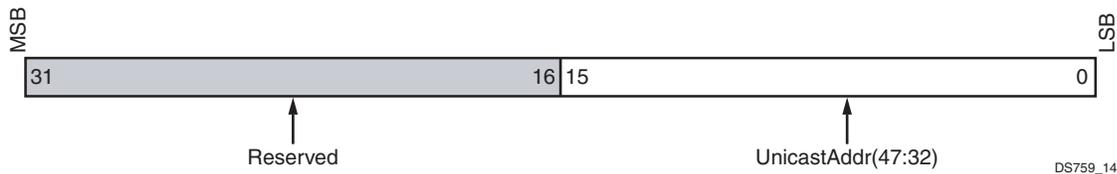


Figure 14: Unicast Address Word Upper Register (offset 0x024)

Table 16 shows the Unicast Address Word Upper Registers bit definitions.

Table 16: Unicast Address Word Upper Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
15 - 0	UnicastAddr	Read/Write	0x00000000	<b>Unicast Address (47:32):</b> This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

### VLAN TPID Word 0 Register (TPID0) - Offset 0x0000\_0028

The VLAN TPID Word 0 Register is shown in Figure 15. This register is only used when transmit and/or receive VLAN functions are included in the core at build-time (C\_TXVLAN\_TAG = 1 and/or C\_RXVLAN\_TAG = 1 and/or C\_TXVLAN\_STRP = 1 and/or C\_RXVLAN\_STRP = 1 and/or C\_TXVLAN\_TRAN = 1 and/or C\_RXVLAN\_TRAN = 1).

This register and the following register allow 4 TPID values be specified for recognizing VLAN frames for both the transmit and receive paths. The most common values for VLAN TPID are 0x8100, 0x9100, 0x9200, 0x88A8. Please

see the section on VLAN functions ([Extended VLAN Support, page 80](#)) for more information about extended VLAN functions.

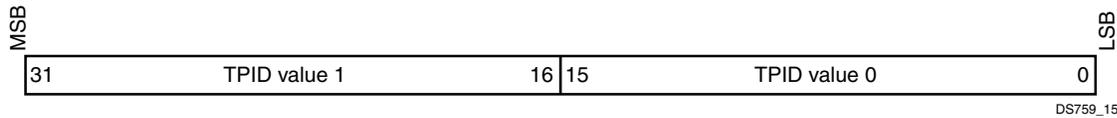


Figure 15: VLAN TPID Word 0 Register (offset 0x0000\_0028)

Table 17 shows the VLAN TPID Word 0 Registers bit definitions.

Table 17: VLAN TPID Word 0 Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	TPID value1	Read/Write	0x0	<b>TPID Value 1:</b> These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.
15 - 0	TPID value 0	Read/Write	0x0	<b>TPID Value 0:</b> These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.

### VLAN TPID Word 1 Register (TPID1) - Offset 0x0000\_002C

The VLAN TPID Word 1 Register is shown in [Figure 16](#). This register is only used when transmit and/or receive VLAN functions are included in the core at build-time (C\_TXVLAN\_TAG = 1 and/or C\_RXVLAN\_TAG = 1 and/or C\_TXVLAN\_STRP= 1 and/or C\_RXVLAN\_STRP= 1 and/or C\_TXVLAN\_TRAN = 1 and/or C\_RXVLAN\_TRAN = 1).

This register and the previous register allow 4 TPID values be specified for recognizing VLAN frames for both the transmit and receive paths. The most common values for VLAN TPID are 0x8100, 0x9100, 0x9200, 0x88A8. Please see the section on VLAN functions ([Extended VLAN Support, page 80](#)) for more information about extended VLAN functions.

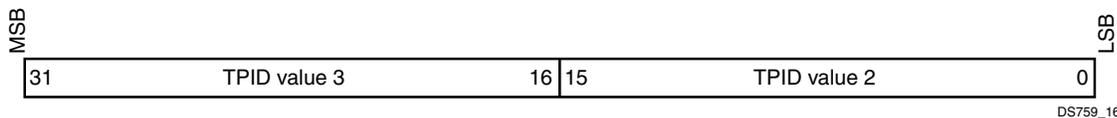


Figure 16: VLAN TPID Word 1 Register (offset 0x0000\_002C)

Table 18 shows the VLAN TPID Word 1 Registers bit definitions.

Table 18: VLAN TPID Word 1 Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	TPID value3	Read/Write	0x0	<b>TPID Value 3:</b> These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.
15 - 0	TPID value 2	Read/Write	0x0	<b>TPID Value 2:</b> These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.

### PCS PMA Soft TEMAC Status Register (PPST) - Offset 0x0000\_0030

The PCS PMA Soft TEMAC Status Register is shown in [Figure 17](#). This register reports valid information when AXI Ethernet is configured for SGMII or 1000Base-X with the Soft TEMAC operating at 10/100/1000Mbps (C\_TYPE = 1

and C\_PHY\_TYPE = 4 or 5). It provides additional information about the serial interface status. For all other configurations, this register will return zeroes.

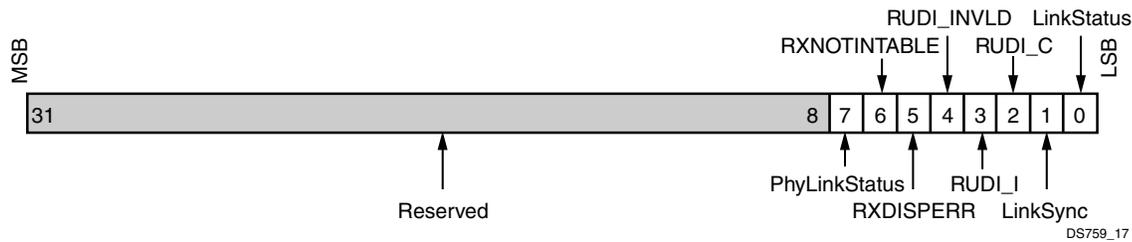


Figure 17: PCS PMA Soft TEMAC Status Register (offset 0x0000\_0030)

Table 19 shows the PCS PMA Soft TEMAC Status Register bit definitions.

Table 19: PCS PMA Soft TEMAC Status Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 8	Reserved	Read	0x000000	Reserved
7	PhyLinkStatus	Read	0	<b>PhyLinkStatus:</b> PHY Link Status (SGMII only) When operating in SGMII mode, this bit represents the link status of the external PHY device attached to the other end of the SGMII link (high indicates that the PHY has obtained a link with its link partner; low indicates that it has not linked with its link partner). When operating in 1000BASE-X mode this bit will remain low and should be ignored.
6	RXNOTINTABLE	Read	0	<b>RXNOTINTABLE:</b> Receive Not In Table. The core has received a code group which is not recognized from the 8B10B coding tables.
5	RXDISPERR	Read	0	<b>RXDISPERR:</b> Receive Disparity Error. The core has received a running disparity error during the 8B10B decoding function.
4	RUDI_INVLD	Read	0	<b>RUDI_INVLD:</b> RUDI(/INVALID/). The core has received invalid data while receiving /C/ or /I/ ordered set.
3	RUDI_I	Read	0	<b>RUDI_I:</b> RUDI(/I/). The core is receiving /I/ ordered sets (Idles)
2	RUDI_C	Read	0	<b>RUDI_C:</b> RUDI(/C/). The core is receiving /C/ ordered sets (Auto-Negotiation Configuration sequences).
1	LinkSync	Read	0	<b>LinkSync:</b> Link Synchronization. This signal indicates the state of the synchronization state machine (IEEE802.3 figure 36-9) which is based on the reception of valid 8B10B code groups. This signal is similar to Bit[0] (Link Status), but is NOT qualified with Auto-Negotiation. When high, link synchronization has been obtained and in the synchronization state machine, sync_status=OK. When low, synchronization has failed.
0	LinkStatus	Read	0	<b>LinkStatus:</b> Link Status. This signal indicates the status of the link. When high, the link is valid: synchronization of the link has been obtained <b>and</b> Auto-Negotiation (if present and enabled) has successfully completed. When low, a valid link has not been established. Either link synchronization has failed or Auto-Negotiation (if present and enabled) has failed to complete. When auto-negotiation is enabled this signal is identical to Bit[1].

**Statistics Counters - Offset 0x0000\_0200-0x0000\_03FF**

The set of 64-bit counters are only present when selected at build-time. The counters keep track of statistics for the transmit and receive Ethernet traffic and are defined in [Table 20](#).

**Table 20: Statistics Counter locations**

<b>C_BASEADDR + Offset</b>	<b>Name</b>	<b>Description</b>
0x200	Received bytes (lower 32 bits)	(RXBL) A count of bytes of frames received (destination address to frame check sequence inclusive).
0x204	Received bytes (upper 32 bits)	(RXBU) A count of bytes of frames received (destination address to frame check sequence inclusive).
0x208	Transmitted bytes (lower 32 bits)	(TXBL) A count of bytes of frames transmitted (destination address to frame check sequence inclusive).
0x20C	Transmitted bytes (upper 32 bits)	(TXBU) A count of bytes of frames transmitted (destination address to frame check sequence inclusive).
0x210	Undersize frames received (lower 32 bits)	(RXUNDRL) A count of the number of frames received (less than 64 bytes in length) but otherwise well formed.
0x214	Undersize frames received (upper 32 bits)	(RXUNDRU) A count of the number of frames received (less than 64 bytes in length) but otherwise well formed.
0x218	Fragment frames received (lower 32 bits)	(RXFRAGL) A count of the number of frames received (less than 64 bytes in length) with a bad frame check sequence field.
0x21C	Fragment frames received (upper 32 bits)	(RXFRAGU) A count of the number of frames received (less than 64 bytes in length) with a bad frame check sequence field.
0x220	64 byte Frames Received OK (lower 32 bits)	(RX64BL) A count of error-free frames received that were 64 bytes in length.
0x224	64 byte Frames Received OK (upper 32 bits)	(RX64BU) A count of error-free frames received that were 64 bytes in length.
0x228	65-127 byte Frames Received OK (lower 32 bits)	(RX65B127L) A count of error-free frames received that were between 65 and 127 bytes in length.
0x22C	65-127 byte Frames Received OK (upper 32 bits)	(RX65B127U) A count of error-free frames received that were between 65 and 127 bytes in length.
0x230	128-255 byte Frames Received OK (lower 32 bits)	(RX128B255L) A count of error-free frames received that were between 128 and 255 bytes in length.
0x234	128-255 byte Frames Received OK (upper 32 bits)	(RX128B255U) A count of error-free frames received that were between 128 and 255 bytes in length.
0x238	256-511 byte Frames Received OK (lower 32 bits)	(RX256B511L) A count of error-free frames received that were between 256 and 511 bytes in length.
0x23C	256-511 byte Frames Received OK (upper 32 bits)	(RX256B511U) A count of error-free frames received that were between 256 and 511 bytes in length.
0x240	512-1023 byte Frames Received OK (lower 32 bits)	(RX512B1023L) A count of error-free frames received that were between 512 and 1023 bytes in length.
0x244	512-1023 byte Frames Received OK (upper 32 bits)	(RX512B1023U) A count of error-free frames received that were between 512 and 1023 bytes in length.

**Table 20: Statistics Counter locations (Cont'd)**

<b>C_BASEADDR + Offset</b>	<b>Name</b>	<b>Description</b>
0x248	1024-MaxFrameSize byte Frames Received OK (lower 32 bits)	(RX1024BL) A count of error-free frames received that were between 1024 bytes and the specified IEEE 802.3-2002 maximum legal length.
0x24C	1024-MaxFrameSize byte Frames Received OK (upper 32 bits)	(RX1024BU) A count of error-free frames received that were between 1024 bytes and the specified IEEE 802.3-2002 maximum legal length.
0x250	Oversize Frames Received OK (lower 32 bits)	(RXOVRL) A count of otherwise error-free frames received that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x254	Oversize Frames Received OK (upper 32 bits)	(RXOVRLU) A count of otherwise error-free frames received that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x258	64 byte Frames Transmitted OK (lower 32 bits)	(TX64BL) A count of error-free frames transmitted that were 64 bytes in length.
0x25C	64 byte Frames Transmitted OK (upper 32 bits)	(TX64BU) A count of error-free frames transmitted that were 64 bytes in length.
0x260	65-127 byte Frames Transmitted OK (lower 32 bits)	(TX65B127L) A count of error-free frames transmitted that were between 65 and 127 bytes in length.
0x264	65-127 byte Frames Transmitted OK (upper 32 bits)	(TX65B127U) A count of error-free frames transmitted that were between 65 and 127 bytes in length.
0x268	128-255 byte Frames Transmitted OK (lower 32 bits)	(TX128B255L) A count of error-free frames transmitted that were between 128 and 255 bytes in length.
0x26C	128-255 byte Frames Transmitted OK (upper 32 bits)	(TX128B255U) A count of error-free frames transmitted that were between 128 and 255 bytes in length.
0x270	256-511 byte Frames Transmitted OK (lower 32 bits)	(TX256B511L) A count of error-free frames transmitted that were between 256 and 511 bytes in length.
0x274	256-511 byte Frames Transmitted OK (upper 32 bits)	(TX256B511U) A count of error-free frames transmitted that were between 256 and 511 bytes in length.
0x278	512-1023 byte Frames Transmitted OK (lower 32 bits)	(TX512B1023L) A count of error-free frames transmitted that were between 512 and 1023 bytes in length.
0x27C	512-1023 byte Frames Transmitted OK (upper 32 bits)	(TX512B1023U) A count of error-free frames transmitted that were between 512 and 1023 bytes in length.
0x280	1024-MaxFrameSize byte Frames Transmitted OK (lower 32 bits)	(TX1024BL) A count of error-free frames transmitted that were between 1024 and the specified IEEE 802.3-2002 maximum legal length.
0x284	1024-MaxFrameSize byte Frames Transmitted OK (upper 32 bits)	(TX1024BU) A count of error-free frames transmitted that were between 1024 and the specified IEEE 802.3-2002 maximum legal length.
0x288	Oversize Frames Transmitted OK (lower 32 bits)	(TXOVRL) A count of otherwise error-free frames transmitted that exceeded the maximum legal frame length specified in IEEE 802.3-2002.

**Table 20: Statistics Counter locations (Cont'd)**

<b>C_BASEADDR + Offset</b>	<b>Name</b>	<b>Description</b>
0x28C	Oversize Frames Transmitted OK (upper 32 bits)	(TXOVRU) A count of otherwise error-free frames transmitted that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x290	Frames Received OK (lower 32 bits)	(RXFL) A count of error-free frames received.
0x294	Frames Received OK (upper 32 bits)	(RXFU) A count of error-free frames received.
0x298	Frame Check Sequence Errors (lower 32 bits)	(RXFCSERL) A count of received frames that failed the CRC check and were at least 64 bytes in length.
0x29C	Frame Check Sequence Errors (upper 32 bits)	(RXFCSERU) A count of received frames that failed the CRC check and were at least 64 bytes in length.
0x2A0	Broadcast Frames Received OK (lower 32 bits)	(RXBCSTFL) A count of frames that were successfully received and were directed to the broadcast group address.
0x2A4	Broadcast Frames Received OK (upper 32 bits)	(RXBCSTFU) A count of frames that were successfully received and were directed to the broadcast group address.
0x2A8	Multicast Frames Received OK (lower 32 bits)	(RXMCSTFL) A count of frames that were successfully received and were directed to a non broadcast group address.
0x2AC	Multicast Frames Received OK (upper 32 bits)	(RXMCSTFU) A count of frames that were successfully received and were directed to a non broadcast group address.
0x2B0	Control Frames Received OK (lower 32 bits)	(RXCTRFL) A count of error-free frames received that contained the special Control Frame identifier in the length/type field.
0x2B4	Control Frames Received OK (upper 32 bits)	(RXCTRFU) A count of error-free frames received that contained the special Control Frame identifier in the length/type field.
0x2B8	Length/Type Out of Range (lower 32 bits)	(RXLTERL) A count of frames received that were at least 64 bytes in length where the length/type field contained a length value that did not match the number of MAC client data bytes received. The counter also increments for frames in which the length/type field indicated that the frame contained padding, but where the number of MAC client data bytes received was greater than 64 bytes (minimum frame size). The exception to the this is when the Length/Type Error Checks are disabled in the chosen MAC, which case this counter will not increment.
0x2BC	Length/Type Out of Range (upper 32 bits)	(RXLTERU) A count of frames received that were at least 64 bytes in length where the length/type field contained a length value that did not match the number of MAC client data bytes received. The counter also increments for frames in which the length/type field indicated that the frame contained padding, but where the number of MAC client data bytes received was greater than 64 bytes (minimum frame size). The exception to the this is when the Length/Type Error Checks are disabled in the chosen MAC, which case this counter will not increment.
0x2C0	VLAN Tagged Frames Received OK (lower 32 bits)	(RXVLANFL) A count of error-free VLAN frames received. This counter will only increment when the receiver is configured for VLAN operation
0x2C4	VLAN Tagged Frames Received OK (upper 32 bits)	(RXVLANFU) A count of error-free VLAN frames received. This counter will only increment when the receiver is configured for VLAN operation

Table 20: Statistics Counter locations (Cont'd)

C_BASEADDR + Offset	Name	Description
0x2C8	Pause Frames Received OK (lower 32 bits)	(RXPFL) A count of error-free frames received that: Contained the MAC Control type identifier 88-08 in the length/type field Contained a destination address that matched either the MAC Control multicast address or the configured source address of the MAC Contained the PAUSE opcode Were acted upon by the MAC
0x2CC	Pause Frames Received OK (upper 32 bits)	(RXPFU) A count of error-free frames received that: Contained the MAC Control type identifier 88-08 in the length/type field Contained a destination address that matched either the MAC Control multicast address or the configured source address of the MAC Contained the PAUSE opcode Were acted upon by the MAC
0x2D0	Control Frames Received with Unsupported Opcode (lower 32 bits)	(RXUOPFL) A count of error-free frames received that contained the MAC Control type identifier 88- 08 in the length/type field but were received with an opcode other than the PAUSE opcode.
0x2D4	Control Frames Received with Unsupported Opcode (upper 32 bits)	(RXUOPFU) A count of error-free frames received that contained the MAC Control type identifier 88- 08 in the length/type field but were received with an opcode other than the PAUSE opcode.
0x2D8	Frames Transmitted OK (lower 32 bits)	(TXFL) A count of error-free frames transmitted.
0x2DC	Frames Transmitted OK (upper 32 bits)	(TXFU) A count of error-free frames transmitted.
0x2E0	Broadcast Frames Transmitted OK (lower 32 bits)	(TXBCSTFL) A count of error-free frames that were transmitted to the broadcast address.
0x2E4	Broadcast Frames Transmitted OK (upper 32 bits)	(TXBCSTFU) A count of error-free frames that were transmitted to the broadcast address.
0x2E8	Multicast Frames Transmitted OK (lower 32 bits)	(TXMCSTFL) A count of error-free frames that were transmitted to a group destination address other than broadcast.
0x2EC	Multicast Frames Transmitted OK (upper 32 bits)	(TXMCSTFU) A count of error-free frames that were transmitted to a group destination address other than broadcast.
0x2F0	Underrun Errors (lower 32 bits)	(TXUNDRERL) A count of frames that would otherwise be transmitted by the core but could not be completed due to the assertion of TX_UNDERRUN during the frame transmission.
0x2F4	Underrun Errors (upper 32 bits)	(TXUNDRERU) A count of frames that would otherwise be transmitted by the core but could not be completed due to the assertion of TX_UNDERRUN during the frame transmission.
0x2F8	Control Frames Transmitted OK (lower 32 bits)	(TXCTRFL) A count of error-free frames transmitted that contained the MAC Control Frame type identifier 88-08 in the length/type field.
0x2FC	Control Frames Transmitted OK (upper 32 bits)	(TXCTR FU) A count of error-free frames transmitted that contained the MAC Control Frame type identifier 88-08 in the length/type field.
0x300	VLAN Tagged Frames Transmitted OK (lower 32 bits)	(TXVLANFL) A count of error-free VLAN frames transmitted. This counter will only increment when the transmitter is configured for VLAN operation.

**Table 20: Statistics Counter locations (Cont'd)**

<b>C_BASEADDR + Offset</b>	<b>Name</b>	<b>Description</b>
0x304	VLAN Tagged Frames Transmitted OK (upper 32 bits)	(TXVLANFU) A count of error-free VLAN frames transmitted. This counter will only increment when the transmitter is configured for VLAN operation.
0x308	Pause Frames Transmitted OK (lower 32 bits)	(TXPFLL) A count of error-free PAUSE frames generated and transmitted by the MAC in response to an assertion of pause_req.
0x30C	Pause Frames Transmitted OK (upper 32 bits)	(TXPFU) A count of error-free PAUSE frames generated and transmitted by the MAC in response to an assertion of pause_req.
0x310	Single Collision Frames Transmitted OK (lower 32 bits)	(TXSCL) A count of frames that are involved in a single collision but were subsequently transmitted successfully.
0x314	Single Collision Frames Transmitted OK (upper 32 bits)	(TXSCU) A count of frames that are involved in a single collision but were subsequently transmitted successfully.
0x318	Multiple Collision Frames Transmitted OK (lower 32 bits)	(TXMCL) A count of frames that are involved in more than one collision but were subsequently transmitted successfully.
0x31C	Multiple Collision Frames Transmitted OK (upper 32 bits)	(TXMCU) A count of frames that are involved in more than one collision but were subsequently transmitted successfully.
0x320	Deferred Transmit Frames (lower 32 bits)	(TXDEFL) A count of frames in which transmission was delayed on its first attempt because the medium was busy.
0x324	Deferred Transmit Frames (upper 32 bits)	(TXDEFU) A count of frames in which transmission was delayed on its first attempt because the medium was busy.
0x328	Frames Transmitted with Late Collisions (lower 32 bits)	(TXLTCL) A count of the times that a collision has been detected later than one slotTime from the start of the packet transmission. A late collision is counted twice: both as a collision and as a lateCollision.
0x32C	Frames Transmitted with Late Collisions (upper 32 bits)	(TXLTU) count of the times that a collision has been detected later than one slotTime from the start of the packet transmission. A late collision is counted twice: both as a collision and as a lateCollision.
0x330	Transmit Frames Aborted with Excessive Collisions (lower 32 bits)	(TXAECL) A count of the frames that, due to excessive collisions, are not transmitted successfully.
0x334	Transmit Frames Aborted with Excessive Collisions (upper 32 bits)	(TXAECU) A count of the frames that, due to excessive collisions, are not transmitted successfully.
0x338	Transmit Frames With Excessive Deferral (lower 32 bits)	(TXEDEFLL) A count of frames that deferred transmission for an excessive period of time.
0x33C	Transmit Frames With Excessive Deferral (upper 32 bits)	(TXEDEFU) A count of frames that deferred transmission for an excessive period of time.
0x340	Frames Received With Alignment Error (lower 32 bits)	(RXAERL) Asserted for received frames of size 64 bytes and greater which contained an odd number of received nibbles and which also contained an invalid FCS field.

Table 20: Statistics Counter locations (Cont'd)

C_BASEADDR + Offset	Name	Description
0x344	Frames Received With Alignment Error (upper 32 bits)	(RXAERU) Asserted for received frames of size 64 bytes and greater which contained an odd number of received nibbles and which also contained an invalid FCS field.

### TEMAC Receive Configuration Word 0 (RCW0) Registers - Offset 0x0000\_0400

The TEMAC Receive Configuration Word 0 Register is shown in Figure 18. This register can be written at any time but the receiver logic will only apply the configuration changes during Inter Frame gaps.

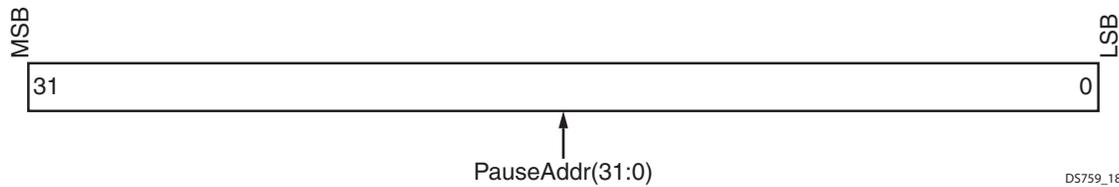


Figure 18: TEMAC Receive Configuration Word 0 (RCW0) Registers (offset 0x400)

Table 21 shows the TEMAC Receive Configuration Word 0 Registers bit definitions.

Table 21: TEMAC Receive Configuration Word 0 (RCW0) Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	PauseAddr	Read/Write	0xDDC CBBAA	<b>Pause Frame Ethernet MAC Address (31:0):</b> This address is used to match the destination address of any received flow control frames. It is also used as the source address for any transmitted flow control frames. This address is ordered so that the first byte transmitted/ received is the lowest position byte in the register. For example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in the PauseAddr(47:0) as 0xFFEED-DCCBBAA.

### TEMAC Receive Configuration Word 1 (RCW1) Registers - Offset 0x0000\_0404

The TEMAC Receive Configuration Word 1 Register is shown in Figure 19. This register can be written at any time but the receiver logic will only apply the configuration changes during Inter Frame gaps. The exception to this is the Reset bit which is effective immediately.

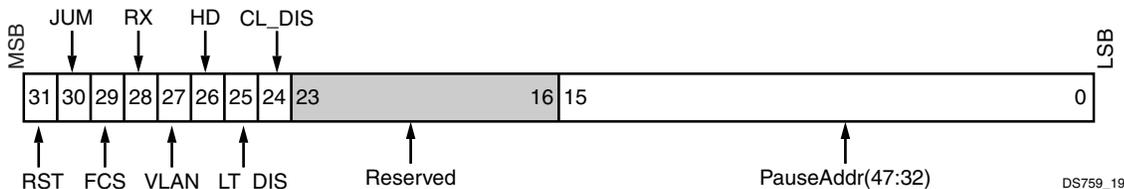


Figure 19: TEMAC Receive Configuration Word 1 (RCW1) Registers (offset 0x404)

Table 22 shows the TEMAC Receive Configuration Word1 Registers bit definitions.

Table 22: TEMAC Receive Configuration Word1 (RCW1) Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31	RST	Read/Write	0	<b>Reset:</b> When this bit is "1", the receiver is reset. The bit automatically resets to "0". The reset also sets all of the receiver configuration registers to their default values. Resetting the receiver without resetting AXI Ethernet could cause the core to be in an unknown state. 0 - no reset 1 - initiate a receiver reset
30	JUM <sup>(1)</sup>	Read/Write	1	<b>Jumbo Frame Enable:</b> When this bit is "1" the receiver accepts frames over the maximum length specified in IEEE Std 802.3-2002 specification. 0 - receive jumbo frames disabled 1 - receive jumbo frames enabled
29	FCS	Read/Write	1	<b>In-Band FCS Enable:</b> When this bit is "1", the receiver provides the FCS field with the rest of the frame data. When this bit is "0" the FCS field is stripped from the receive frame data. In either case the FCS field is verified. 0 - strip the FCS field from the receive frame data 1 - provide the FCS field with the receive frame data
28	RX	Read/Write	1	<b>Receive Enable:</b> When this bit is "1", the receiver logic is enabled to operate. When this bit is "0", the receiver ignores activity on the receive interface. 0 - receive disabled 1 - receive enabled
27	VLAN <sup>(2)</sup>	Read/Write	1	<b>VLAN Frame Enable:</b> When this bit is "1", the receiver accepts VLAN tagged frames. The maximum payload length increases by four bytes. 0 - receive of VLAN frames disabled 1 - receive of VLAN frames enabled
26	HD	Read/Write	0	<b>Half-Duplex Mode:</b> When this bit is "1", the receive operates in half-duplex mode. When this bit is "0", the receiver operates in full-duplex mode. Only full-duplex is supported so this bit should always be set to "0". 0 - full-duplex receive 1 - half-duplex receive
25	LT_DIS	Read/Write	0	<b>Length/Type Field Valid Check Disable:</b> When this bit is "1", it disables the Length/Type field check on the receive frame. 0 - perform Length/Type field check 1 - do not perform Length/Type field check
24	CL_DIS	Read/Write	0x0	<b>Control Frame Length Check Disable:</b> When this bit is 1, control frames larger than the minimum frame length can be accepted
23 - 16	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
15 - 0	PauseAddr	Read/Write	0xFFEE	<b>Pause Frame Ethernet MAC Address (47:32):</b> This address is used to match the destination address of any received flow control frames. It is also used as the source address for any transmitted flow control frames. This address is ordered so that the first byte transmitted/ received is the lowest position byte in the register. For example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in the PauseAddr(47:0) as 0xFFEEDDCCBBAA.

Table 22: TEMAC Receive Configuration Word1 (RCW1) Registers Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
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**Notes:**

1. Extended VLAN function require that jumbo frames be enabled.
2. This bit enables basic VLAN operation that is native to the TEMAC core. The TEMAC core recognizes VLAN frames when the Type/Length field contains a VLAN TAG with a TPID value of 0x8100. No other TPID values are recognized. Extended VLAN mode described later allow programmable TPID values. This bit must be "0" (disabled) when using extended VLAN mode.

**TEMAC Transmit Configuration (TC) Registers - Offset 0x0000\_0408**

The TEMAC Transmit Configuration Register is shown in Figure 20. This register can be written at any time but the transmitter logic will only apply the configuration changes during Inter Frame gaps. The exception to this is the Reset bit which is effective immediately.

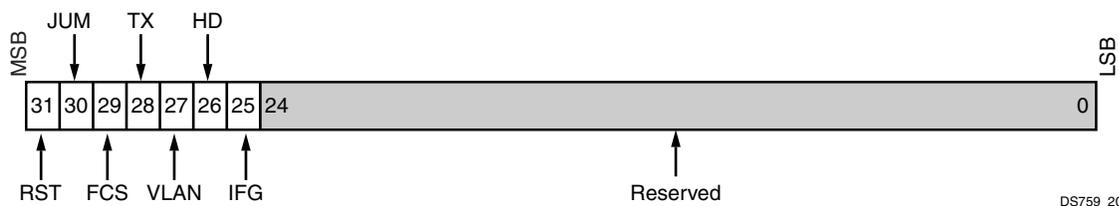


Figure 20: TEMAC Transmit Configuration Registers (offset 0x408)

Table 23 shows the TEMAC Transmit Configuration Registers bit definitions.

Table 23: TEMAC Transmit Configuration Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31	RST	Read/Write	0	<b>Reset:</b> When this bit is "1", the transmitter is reset. The bit automatically resets to "0". The reset also sets all of the transmitter configuration registers to their default values. Resetting the transmitter without resetting AXI Ethernet could cause the core to be in an unknown state. 0 - no reset 1 - initiate a transmitter reset
30	JUM <sup>(1)</sup>	Read/Write	1	<b>Jumbo Frame Enable:</b> When this bit is "1" the transmitter sends frames over the maximum length specified in IEEE Std 802.3-2002 specification. 0 - send jumbo frames disabled 1 - send jumbo frames enabled
29	FCS	Read/Write	0	<b>In-Band FCS Enable:</b> When this bit is "1", the transmitter accepts the FCS field with the rest of the frame data. When this bit is "0" the FCS field is calculated and supplied by the transmitter. In either case the FCS field is verified. 0 - transmitter calculates and sends FCS field 1 - FCS field is provided with transmit frame data
28	TX	Read/Write	1	<b>Transmit Enable:</b> When this bit is "1", the transmit logic is enabled to operate. 0 - transmit disabled 1 - transmit enabled
27	VLAN <sup>(2)</sup>	Read/Write	1	<b>VLAN Frame Enable:</b> When this bit is "1", the transmitter allows transmission of VLAN tagged frames. 0 - transmit of VLAN frames disabled 1 - transmit of VLAN frames enabled

Table 23: TEMAC Transmit Configuration Registers Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
26	HD	Read/Write	0	<b>Half-Duplex Mode:</b> When this bit is "1", the transmitter operates in half-duplex mode. When this bit is "0", the transmitter operates in full-duplex mode. Only full-duplex is supported so this bit should always be set to "0". 0 - full-duplex transmit 1 - half-duplex transmit
25	IFG	Read/Write	1	<b>Inter Frame Gap Adjustment Enable:</b> When this bit is "1", the transmitter uses the value of the IFGP register (Figure 6) to extend the transmit Inter Frame Gap beyond the minimum of 12 idle cycles (96-bit times on the Ethernet Interface). 0 - no IFGP adjustment enabled 1 - IFGP adjusted based on IFGP register
24 - 0	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.

**Notes:**

- Extended VLAN function require that jumbo frames be enabled.
- This bit enables basic VLAN operation that is native to the TEMAC core. The TEMAC core recognizes VLAN frames when the Type/Length field contains a VLAN TAG with a TPID value of 0x8100. No other TPID values are recognized. Extended VLAN mode described later allow programmable TPID values. This bit must be "0" (disabled) when using extended VLAN mode.

**TEMAC Flow Control Configuration (FCC) Registers - Offset 0x0000\_040C**

The TEMAC Flow Control Configuration Register is shown in Figure 21. This register can be written at any time but the flow control logic will only apply the configuration changes during Inter Frame gaps.

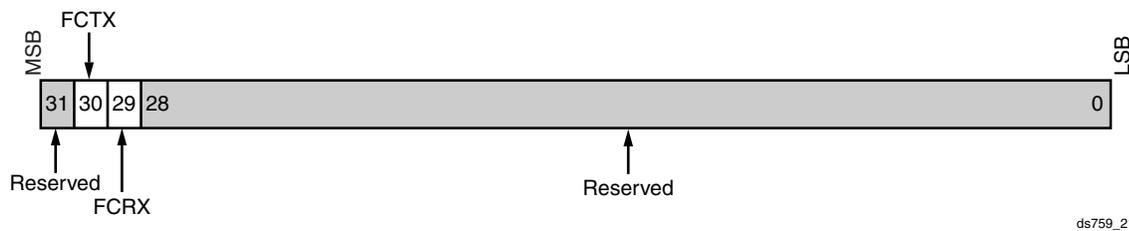


Figure 21: TEMAC Flow Control Configuration Registers (offset 0x40C)

Table 24 shows the TEMAC Flow Control Configuration Registers bit definitions.

Table 24: TEMAC Flow Control Configuration Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31	Reserved	Read	0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
30	FCTX	Read/Write	1	<b>Transmit Flow Control Enable:</b> When this bit is "1", the transmitter will send a flow control frame when a value is written to the <a href="#">Transmit Pause Frame Registers (TPF) - Offset 0x0000_0004, page 21</a> . 0 - transmit flow control frame disabled 1 - transmit flow control frame enabled
29	FCRX	Read/Write	1	<b>Receive Flow Control Enable:</b> When this bit is "1", the receive flow control frames inhibit transmitter operation. When this bit is "0", the flow control frames are passed through with other receive frames. 0 - receive flow control disabled 1 - receive flow control enabled

Table 24: TEMAC Flow Control Configuration Registers Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
28 - 0	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.

### TEMAC Ethernet MAC Mode Configuration (EMMC) Registers - Offset 0x0000\_0410

The TEMAC Ethernet MAC Mode Configuration Register is shown in Figure 22. This register can be written at any time but the Ethernet interface will only apply the configuration changes during Inter Frame gaps. This register is slightly different for implementations using the soft TEMAC (C\_TYPE = 0 or C\_TYPE = 1) and Virtex-6 hard TEMAC (C\_TYPE = 2).

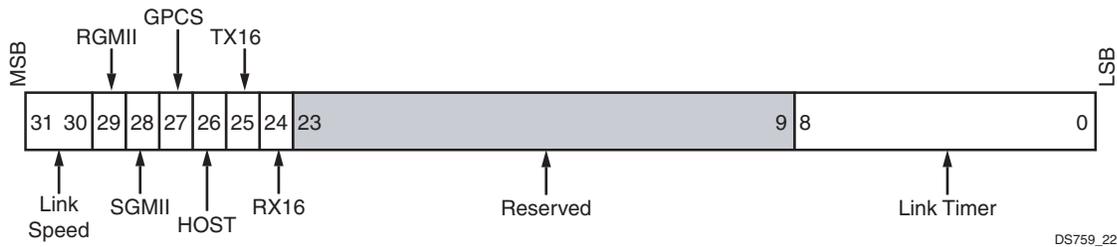


Figure 22: TEMAC Ethernet MAC Mode Configuration Registers (offset 0x410)

Table 25 shows the TEMAC Ethernet MAC Mode Configuration Registers bit definitions.

Table 25: TEMAC Ethernet MAC Mode Configuration Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 30	Link Speed	Read/Write <sup>(1)(2)</sup>	10 / 01 <sup>(3)</sup>	<b>Link Speed Selection:</b> The speed of the Ethernet interface is defined by the following values. 10 - 1000 Mb/S 01 - 100 Mb/S 00 - 10 Mb/s 11 - N/A
29	RGMI I	Read Read/Write <sup>(1)(2)</sup>	0	<b>RGMI I Mode Enable:</b> When this bit is "1", the Ethernet interface is configured in RGMI I mode. 0 - not configured in RGMI I mode 1 - configured in RGMI I mode
28	SGMI I	Read Read/Write <sup>(1)(2)</sup>	0	<b>SGMI I Mode Enable:</b> When this bit is "1", the Ethernet interface is configured in SGMI I mode. 0 - not configured in SGMI I mode 1 - configured in SGMI I mode
27	GPCS	Read Read/Write <sup>(1)(2)</sup>	0	<b>1000BASE-X Mode Enable:</b> When this bit is "1", the Ethernet interface is configured in 1000BASE-X mode. 0 - not configured in 1000BASE-X mode 1 - configured in 1000BASE-X mode
26	HOST	Read Read/Write <sup>(1)(2)</sup>	1 / 0 <sup>(4)</sup>	<b>Host Interface Enable:</b> When this bit is "1", the host interface is enabled. 0 - host interface disabled 1 - host interface is enabled

Table 25: TEMAC Ethernet MAC Mode Configuration Registers Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
25	TX16	Read Read/Write <sup>(1)(2)</sup>	0	<b>Transmit 16-bit Data Interface Enable:</b> When this bit is "1" and 1000BASE-X is being used, the transmit data interface is 16-bits wide. When this bit is "0", the transmit data interface is 8-bits wide. The 16-bit interface is not supported so this bit should always return "0". 0 - 8-bit transmit data interface 1 - 16-bit transmit data interface
24	RX16	Read Read/Write <sup>(1)(2)</sup>	0	<b>Receive 16-bit Data Interface Enable:</b> When this bit is "1" and 1000BASE-X is being used, the receive data interface is 16-bits wide. When this bit is "0", the receive data interface is 8-bits wide. The 16-bit interface is not supported so this bit should always return "0". 0 - 8-bit receive data interface 1 - 16-bit receive data interface
23-9	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
8-0	Link Timer	Read/Write <sup>(1)(2)</sup>		<b>Link Timer:</b> Sets the programmable link timer value, for operation with 1000BASE-X or SGMII modes

**Notes:**

1. The entire contents of this register are Read/Write accessible for the Virtex-6 hard TEMAC configuration, but only bits 31-30 are Read/Write accessible in the Soft TEMAC configuration
2. Only bits 31-30 are used with soft TEMAC. All other bits are reserved.
3. The Reset Value for LINK SPEED is "10" or 1000 Mb/s for all PHY interfaces except for MII which is not capable of that speed. The Reset Value for LINK SPEED for the MII interface is "01" or 100 Mb/s.
4. The use or not of the Host interface is hidden from the user and is of no concern. However, this register will return a different reset value for different TEMAC implementations. The soft TEMAC implementation will return a "0" while the Virtex-6 hard TEMAC implementation will return a "1".

**TEMAC RGMII/SGMII Configuration (PHYC) Registers - Offset 0x00000414**

The TEMAC RGMII/SGMII Configuration Register is shown in Figure 23. This register applies only to the hard TEMAC.

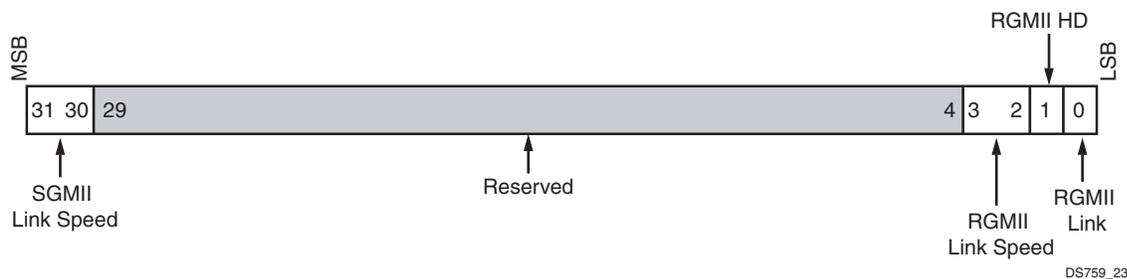


Figure 23: TEMAC RGMII/SGMII Configuration Registers (offsett 0x00000414)

Table 26 shows the TEMAC RGMII/SGMII Configuration Registers bit definitions. This register applies only to the hard TEMAC

Table 26: TEMAC RGMII/SGMII Configuration Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 30	SGMII Link Speed	Read	0x0	<b>SGMII Link Speed:</b> Valid in SGMII mode only. This displays the SGMII speed information as received from auto negotiation by the speed field of the PCS/PMA register 5 (Table 2). The speed of the Ethernet interface is defined by the following values. 10 - 1000 Mb/S 01 - 100 Mb/S 00 - 10 Mb/s 11 - N/A
29 - 4	Reserved	Read	0x0	<b>Reserved.</b> These bits are reserved for future definition and will always return zero.
3 - 2	RGMII Link Speed	Read	0x0	<b>RGMII Link Speed:</b> Valid in RGMII mode only. This displays the RGMII speed information as encoded by the PHY to the TEMAC by GMII_RX_DV and GMII_RX_ER during the IFG. The speed of the Ethernet interface is defined by the following values. 10 - 1000 Mb/S 01 - 100 Mb/S 00 - 10 Mb/s 11 - N/A
1	RGMII HD	Read	0	<b>RGMII Half-Duplex Mode:</b> Valid in RGMII mode only. When this bit is “1”, the interface operates in half-duplex mode. When this bit is “0”, the interface operates in full-duplex mode. This information is encoded by the PHY to the TEMAC by GMII_RX_DV and GMII_RX_ER during the IFG. Only full-duplex is supported so this bit should always be set to “0”. 0 - full-duplex 1 - half-duplex
0	RGMII Link	Read	0	<b>RGMII Link:</b> Valid in RGMII mode only. When this bit is “1”, the link is up. When this bit is “0”, the link is down. This information is encoded by the PHY to the TEMAC by GMII_RX_DV and GMII_RX_ER during the IFG. 0 - link is down 1 - link is up

### MII Management (MDIO) Configuration (MC) Registers - Offset 0x0000\_0500

The MII Management Configuration Register is shown in Figure 24.

This register provides control for the TEMAC PHY MII management (MDIO) interface. The MDIO interface supplies a clock to the external device, MDC. This clock is derived from the HostClk input signal using the value in the Clock Divide[5:0].

The frequency of the MDIO clock is given by the following equation:

$$f_{MDC} = \frac{f_{HOSTCLK}}{(1 + \text{Clock Divide}[5:0]) \times 2}$$

To comply with the IEEE 802.3-2002 specification for this interface, the frequency of the MDC should not exceed 2.5 MHz.

To prevent MDC from being out of specification, the Clock Divide[5:0] value powers up at 000000. While this value is in the register, it is impossible to enable the MDIO interface.

Even if the MDIO interface is enabled by setting bit 6 of this register, the MDIO port will still be disabled until a non-zero value has been written into the clock divide field.

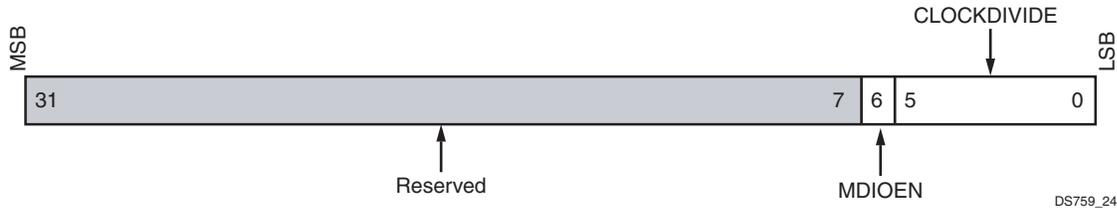


Figure 24: MII Management (MDIO) Configuration Registers (offset 0x500)

Table 27 shows the MII Management Configuration Register bit definitions.

Table 27: MII Management (MDIO) Configuration (MC) Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31-7	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
6	MDIOEN	Read/Write	0	<b>MDIO Enable:</b> When this bit is "1", the MDIO (MII Management) interface is used to access the PHY. 0 - MDIO disabled 1 - MDIO enabled
5 - 0	CLOCK DIVIDE	Read/Write	0x0	<b>Clock Divide:</b> This value is used to derive the MDC (MII Management interface clock) signal. The maximum permitted frequency is 2.5 MHz.

### MII Management (MDIO) Control Register (MCR) - Offset 0x0000\_0504

The MII Management Control Register is shown in Figure 25. This register can be written at any time but the Ethernet interface will only apply the configuration changes during Inter Frame gaps. This register is slightly different for implementations using the soft TEMAC (C\_TYPE = 0 or C\_TYPE = 1) and Virtex-6 hard TEMAC (C\_TYPE = 2).

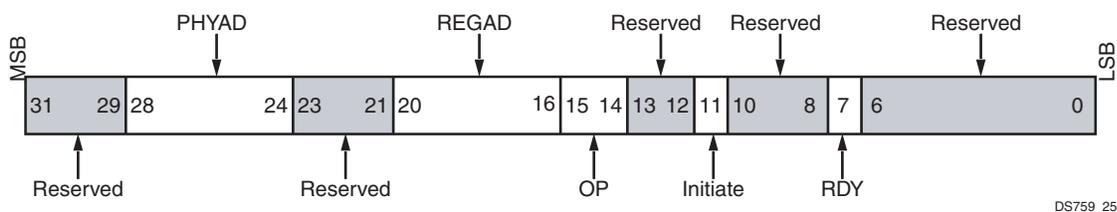


Figure 25: MII Management (MDIO) Control Register (offset 0x504)

Table 25 shows the MII Management Control Register bit definitions.

Table 28: MII Management (MDIO) Control Register (MCR) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 29	Reserved	Reserved	000	Reserved

Table 28: MII Management (MDIO) Control Register (MCR) Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
28-24	PHYAD	Read/Write	00000	<b>PHY Physical Address:</b> The physical address of the PHY.
23-21	Reserved	Reserved	000	Reserved
20-16	REGAD	Read/Write <sup>(1)</sup>	00000	<b>PHY Register Address:</b> These bits represent the register to be accessed in a particular PHY, as indicated in the PHYAD field.
15-14	OP	Read/Write	00	<b>Operation Code.</b> These bits determine if a read or write is going to be performed. 01 - Write 10 - Read
13-12	Reserved	Read/Write	00	Reserved
11	Initiate	Read/Write <sup>(2)</sup>	0	<b>Initiate:</b> This bit must be set to “1” to initiate a MDIO transaction. 0 = Do not start an MDIO transaction 1 = Initiate an MDIO transaction
10-8	Reserved	Read/Write	000	Reserved
7	RDY	Read	1	<b>Ready:</b> This bit indicates if the MII Management interface is ready to accept a new transaction. 0 = Cannot accept a new transaction 1 = Ready to accept a new transaction
6-0	Reserved	Reserved	0000000	Reserved

**Notes:**

1. The first 16 registers (0-15) are defined by IEEE Std 802.3-2005. The remaining 16 registers (16-31) are reserved for PHY vendors' own register definition.
2. This bit clears upon a write.

**MII Management (MDIO) Write Data (MWD) Register - Offset 0x0000\_0508**

The MII Management Write Data Register is shown in Figure 26. This register is a temporary storage location for data to be written to a PHY register (internal or external) via the MDIO interface. A MDIO write is initiated by writing to the MII Management Control Register with the physical PHY address (PHYAD), the PHY's register to be accessed (REGAD), the access type, and setting the Initiate bit after providing the data to this register.

This register is only used for writing to PHY registers. When reading from PHY registers, the data will be stored MII Management Read Data Register. For more information on using the MDIO interface for accessing PHY registers, please see [Using the Address Filters, page 56](#).

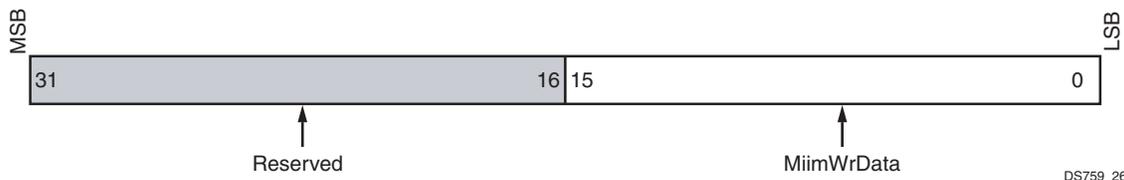


Figure 26: MII Management (MDIO) Write Data Register (offset 0x508)

Table 29 shows the MII Management Write Data Register bit definitions.

Table 29: MII Management (MDIO) Write Data (MWD) Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
15 - 0	Write Data	Read/Write	0x0	<b>MII Management Write Data:</b> This field temporarily holds data to be written to a PHY register.

### MII Management (MDIO) Read Data (MRD) Register - Offset 0x0000\_050C

The MII Management Read Data Register is shown in Figure 27. This register is a temporary storage location for data to be read from a PHY register (internal or external) via the MDIO interface. A MDIO read is initiated by writing to the MII Management Control Register with the physical PHY address (PHYAD), the PHY's register to be accessed (REGAD), the access type, and setting the Initiate bit.

This register is only used for temporarily storing the data read from the PHY registers. For more information on using the MDIO interface for accessing PHY registers, see Using the Address Filters, page 56.

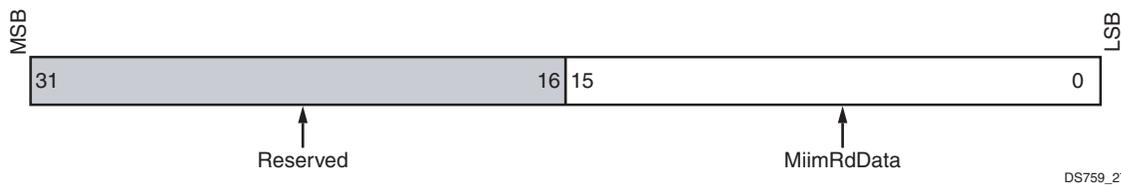


Figure 27: MII Management (MDIO) Read Data Register (offset 0x50C)

Table 25 shows the MDIO Ethernet MAC Mode Configuration Registers bit definitions.

Table 30: MII Management (MDIO) Read Data (MRD) Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	Reserved	Read/Write	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
15 - 0	Read Data	Read/Write	0x0	<b>MII Management Read Data:</b> This field temporarily holds data to be read from a PHY register.

### MDIO Interrupt Status (MIS) Register - Offset 0x00000600

The MDIO Interrupt Status register is shown in Figure 28.

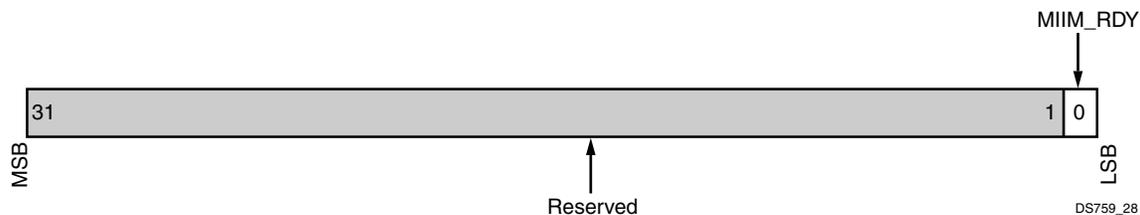


Figure 28: MDIO Interrupt Status Register - Offset 0x00000600

Table 31 shows the MDIO Interrupt Status Registers bit definitions.

Table 31: MDIO Interrupt Status Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	Read	0	Reserved
0	MIIM_RDY	Read/Write	0	<b>MII Management Interrupt Status:</b> This bit is set by either the MIIM interface or by writing a '1' to it. In either case, it indicates an interrupt is pending. The interrupt is cleared by writing a '0' to this bit. 0 - no interrupt pending/clear interrupt 1 - interrupt pending/set interrupt

### MDIO Interrupt Pending (MIP) Register - Offset 0x00000620

The MDIO Interrupt Enable Register is shown in Figure 29. Please refer to Figure 8 for the structure of the interrupt registers.

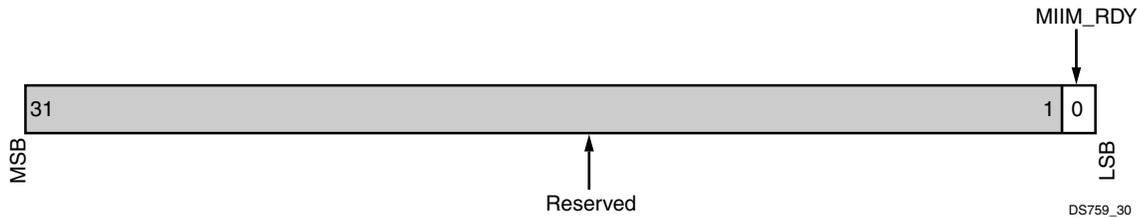


Figure 29: MDIO Interrupt Pending Register - Offset 0x00000620

Table 32 shows the MDIO Interrupt Pending Register bit definitions.

Table 32: MDIO Interrupt Pending Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	Read	0	Reserved
0	MIIM_RDY	Read	0	<b>MII Management Interrupt Pending:</b> This bit indicates an interrupt is pending if the corresponding bit in the MIS and MIE are set. 0 - no interrupt pending 1 - interrupt pending

### MDIO Interrupt Enable (MIE) Register - Offset 0x00000640

The MDIO Interrupt Enable Register is shown in Figure 30. Please refer to Figure 8 for the structure of the interrupt registers.

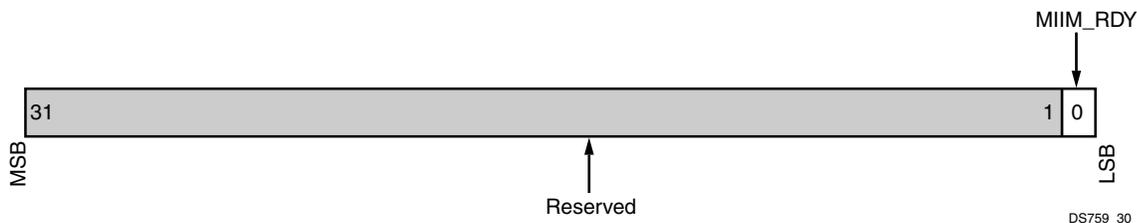


Figure 30: MDIO Interrupt Enable Register - Offset 0x00000640

Table 33 shows the MDIO Interrupt Enable Register bit definitions.

Table 33: MDIO Interrupt Enable Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	Read	0	Reserved
0	MIIM_RDY	Read/Write	0	<b>MII Management Interrupt Enable:</b> When set, this bit allows an interrupt in the MIS register to generate an interrupt in the MIP register. 0 - Disable interrupt 1 - Enable interrupt

### MDIO Interrupt Clear (MIC) Register - Offset 0x00000660

The MDIO Interrupt Clear Register is shown in Figure 31. Please refer to Figure 8 for the structure of the interrupt registers.

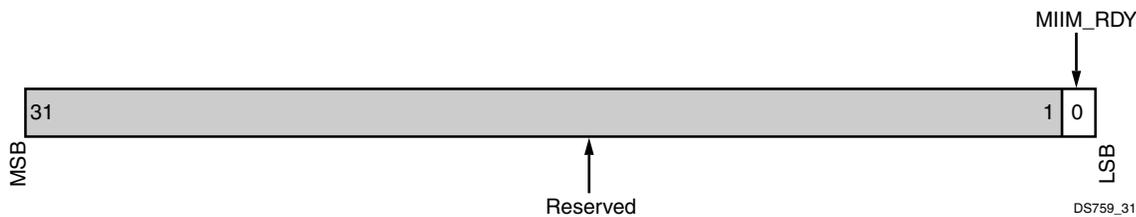


Figure 31: MDIO Interrupt Clear Register - Offset 0x00000660

Table 34 shows the MDIO Interrupt Clear Register bit definitions.

Table 34: MDIO Interrupt Clear Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	Read	0	Reserved
0	MIIM_RDY	Read/Write	0	<b>MII Management Clear Enable:</b> Writing a '1' to this bit will clear the corresponding interrupt in the MIS register. This bit is self clearing. 0 - Do not clear Interrupt 1 - Clear Interrupt

### TEMAC Unicast Address Word 0 (UAW0) Registers - Offset 0x00000700

The TEMAC Unicast Address Word 0 Register is shown in Figure 32.

The Unicast Addresses Registers combine to provide a 48 bit ethernet station address. Word 0 provides the low order 32 bits of the address while word 1 provides the high order 16 bits.

This register's reset value is slightly different for implementations using the soft TEMAC (C\_TYPE = 0 or C\_TYPE = 1) and Virtex-6 hard TEMAC (C\_TYPE = 2).

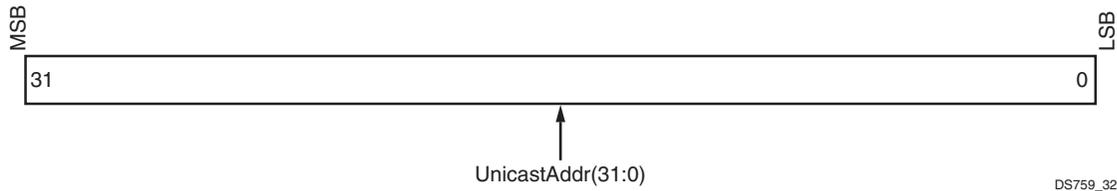


Figure 32: TEMAC Unicast Address Word 0 Registers (offset 0x00000700)

Table 35 shows the TEMAC Unicast Address Word 0 Registers bit definitions.

Table 35: TEMAC Unicast Address Word 0 Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	UnicastAddr	Read/Write	0xDDCCBBAA 0xFFFFFFFF <sup>(1)</sup>	<b>Unicast Address (31:0):</b> This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCBBAA.

**Notes:**

1. This register will return a different reset value for different TEMAC implementations. The soft TEMAC implementation will return a 0xFFFFFFFF while the Virtex-6 hard TEMAC implementation will return a 0xDDCCBBAA.

**TEMAC Unicast Address Word 1 (UAW1) Registers - Offset 0x00000704**

The TEMAC Unicast Address Word 1 Register is shown in Figure 33.

The Unicast Addresses Registers combine to provide a 48 bit ethernet station address. Word 0 provides the low order 32 bits of the address while word 1 provides the high order 16 bits.

This register's reset value is slightly different for implementations using the soft TEMAC (C\_TYPE = 0 or C\_TYPE = 1) and Virtex-6 hard TEMAC (C\_TYPE = 2).

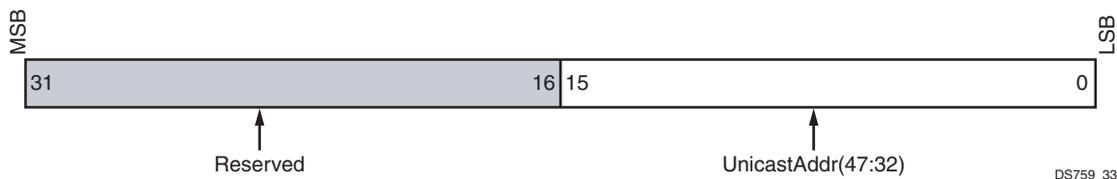


Figure 33: TEMAC Unicast Address Word 1 Registers (offset 0x00000704)

Table 36 shows the TEMAC Unicast Address Word 1 Registers bit definitions.

Table 36: TEMAC Unicast Address Word 1 Registers Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.

Table 36: TEMAC Unicast Address Word 1 Registers Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
15 - 0	UnicastAddr	Read/Write	0x0000FFEE 0xFFFFFFFF <sup>(1)</sup>	<b>Unicast Address (47:32):</b> This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

**Notes:**

1. This register will return a different reset value for different TEMAC implementations. The soft TEMAC implementation will return a 0xFFFFFFFF while the Virtex-6 hard TEMAC implementation will return a 0x0000FFEE.

**Filter Mask Index (FMI) Register - Offset 0x00000708**

The TEMAC Address Filter Mode Register is shown in Figure 34.

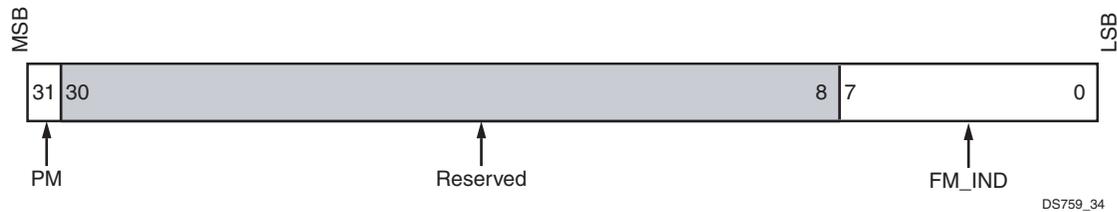


Figure 34: Filter Mask Index Register (offset 0x00000708)

Table 37 shows the TEMAC Address Filter Mask Register bit definitions.

Table 37: Filter Mask Index Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31	PM <sup>(1)</sup>	Read/Write	0	<b>Promiscuous Receive Address Mode Enable:</b> When this bit is "1", the receive address filtering is disabled and all destination addresses are accepted. When this bit "0", the receive address filtering is enabled. 0 - address filtering enabled 1 - address filtering disabled (all addresses accepted)
30 - 8	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
7 - 0	FM_IND	Read/Write	0x00	<b>Filter Mask Index:</b> Provides the address index for the filter table. Once set, it does not need to be changed until another address filter entry needs accessed. 0x00 = Filter 0 0x01 = Filter 1 0x02 = Filter 2 0x03 = Filter 3

**Notes:**

1. Extended Multicast Filtering require the promiscuous mode be enabled/ address filtering is disabled.

### Address Filter (AF0) Register 0 (31:0)- Offset 0x00000710

This register can be used to filter any address type, not just multicast addresses. Before accessing this register, set the Filter Mask Index (FM\_IND) to the appropriate setting. See [Using the Address Filters, page 56](#) for more information.

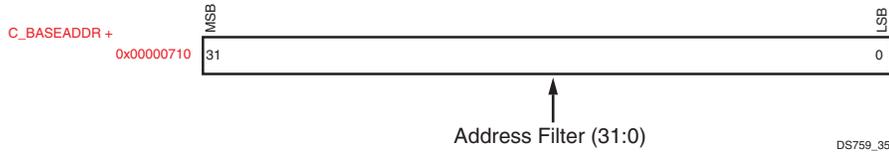


Figure 35: Address Filter Register 0

Table 37 shows the Address Filter Register bit definitions.

Table 38: Address Filter Register 0 Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Address Filter (31:0)	Read/Write	0xFFFFFFFF	<b>Address Filter (31:0):</b> This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Addr(47:0) as 0xFFEEDDCBBAA.

### Address Filter (AF1) Register 1 (47:32) - Offset 0x00000714

This register can be used to filter any address type, not just multicast addresses. Before accessing this register, set the Filter Mask Index (FM\_IND) to the appropriate setting. See [Using the Address Filters, page 56](#) for more information.

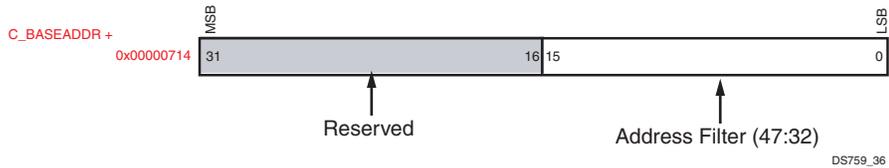


Figure 36: Address Filter Register 1

Table 37 shows the Address Filter Register bit definitions.

Table 39: Address Filter 1 Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 16	Reserved	Read	0x0000	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
15 - 0	Address Filter (47:32)	Read/Write	0xFFFF	<b>Address Filter(47:32):</b> This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Addr(47:0) as 0xFFEEDDCBBAA.

To update an address filter, first select the address filter to be accessed (bottom bits of the Filter Mask Index Register (note the msb of this register provides the Promiscuous mode control), then access the associated register.

**Transmit VLAN Data Table - Offset 0x0000\_4000-0x0000\_7FFF**

This table is used for data to support transmit VLAN tagging, VLAN stripping, and VLAN translation. The table is always 4K entries deep but the width depends on how many of the VLAN functions are included at build time. VLAN translation requires 12 bits at each location while VLAN stripping and VLAN tagging require 1 bit each at each location.

When all transmit VLAN functions are included, the table is 14 bits wide. If VLAN functions are not included, the bits for those functions will not be present and writes to those bits will have no effect while reads will return zero.

The table may be either 1-bit, 2-bits, 12-bits, 13-bits, or 14-bits wide depending on which features are present. The table must be initialized by software via the AXI4-Lite and is addressed on 32-bit word boundaries.

The transmit VLAN Table entry with all VLAN functions present is shown in Figure 37 while Figure 38 shows the transmit VLAN Table entry with only the translation field. Note that the bit locations for the functions do not change even when some functions are not used in the build.

Please see the section on VLAN functions for more details (Extended VLAN Support, page 80).

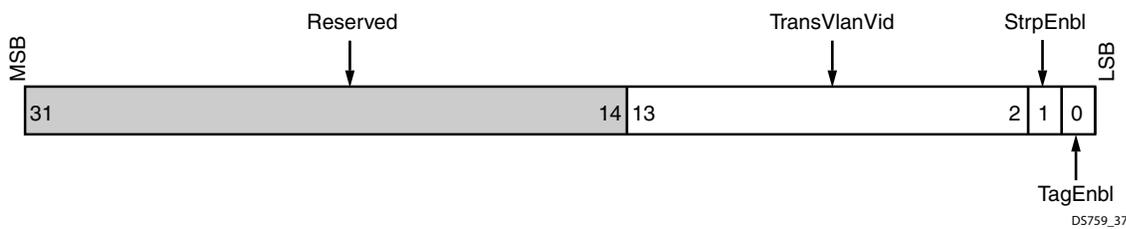


Figure 37: Transmit VLAN Table entry w/ all fields (offset 0x0000\_4000-0x0000\_7FFF)

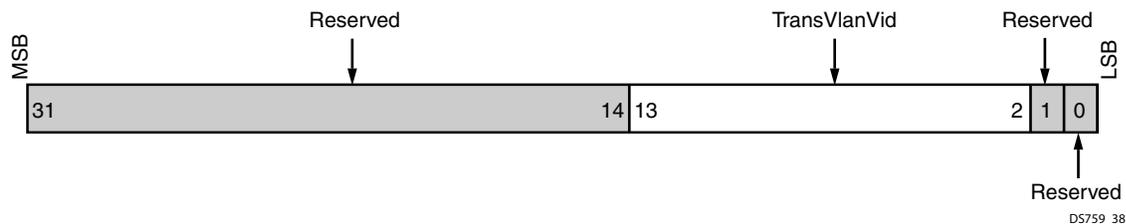


Figure 38: Transmit VLAN Table entry w/ one field (offset 0x0000\_4000-0x0000\_7FFF)

**Receive VLAN Data Table - Offset 0x0000\_8000-0x0000\_BFFF**

This table is used for data to support receive VLAN tagging, VLAN stripping, and VLAN translation. The table is always 4K entries deep but the width depends on how many of the VLAN functions are included at build time. VLAN translation requires 12 bits at each location while VLAN stripping and VLAN tagging require 1 bit each at each location.

When all receive VLAN functions are included, the table is 14 bits wide. If VLAN functions are not included, the bits for those functions will not be present and writes to those bits will have no effect while reads will return zero.

The table may be either 1-bit, 2-bits, 12-bits, 13-bits, or 14-bits wide depending on which features are present. The table must be initialized by software via the AXI4-Lite and is addressed on 32-bit word boundaries.

The receive VLAN Table entry with all VLAN functions present is shown in Figure 39 while Figure 40 shows the receive VLAN Table entry with only the translation field. Note that the bit locations for the functions do not change even when some functions are not used in the build.

Please see the section on VLAN functions for more details (Extended VLAN Support, page 80).

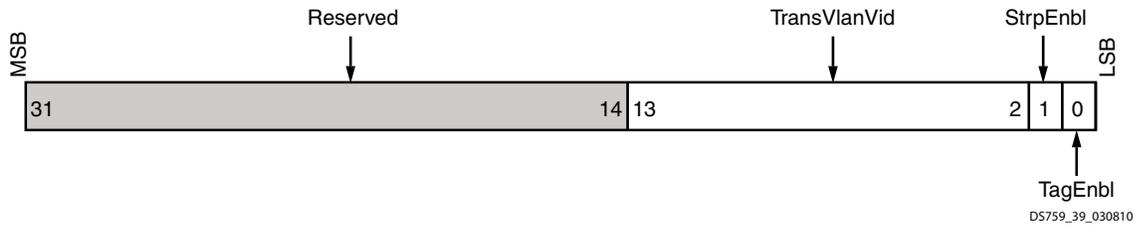


Figure 39: Receive VLAN Table entry w/ all fields (offset 0x0000\_8000-0x0000\_BFFF)

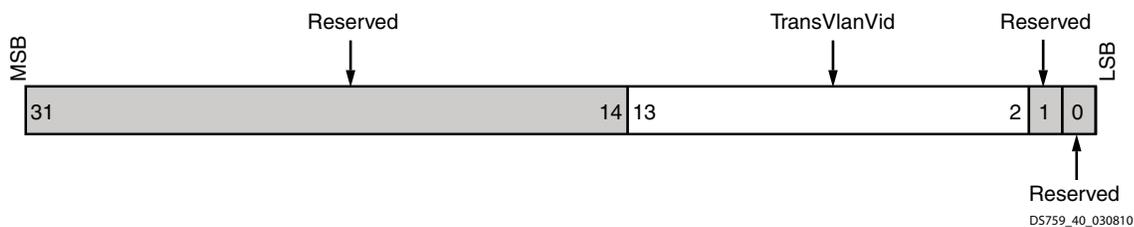


Figure 40: Receive VLAN Table entry w/ one field (offset 0x0000\_8000-0x0000\_BFFF)

## AVB Addressing

### Receive PTP Packet Buffer - Offset 0x00010000 - 0x00010FFF

The Receive PTP Packet Buffer is 4 kb . Please refer to UG492 for more information.

### Transmit PTP Packet Buffer - Offset 0x00011000 - 0x000117FF

The Transmit PTP Packet Buffer is divided into eight identical buffer sections with each section containing 256 bytes. Please refer to UG492 for more information.

### AVB Tx/Rx Configuration - Offset 0x00012000 - 0x0001201B

Please refer to UG492 for more information.

### AVB RTC Configuration - Offset 0x00012800 - 0x000128FF

Please refer to UG492 for more information.

### Address Filter Configuration - Offset 0x00013000 - 0x000130FF

Please refer to UG492 for more information.

### Multicast Address Table - Offset 0x0002\_0000-0x0003\_FFFF

The Multicast Address Table entry is shown in Figure 42. The multicast address table is only present when extended multicast address filtering is selected at build-time (C\_MCAST\_EXTEND = 1). The purpose of the table is to allow the AXI Ethernet to support reception of frames addressed to many multicast addresses while providing some of the filtering in hardware to off load some of the overhead required for filtering in software.

While a MAC multicast address is defined as any 48 bit MAC address that has bit 0 (LSb) set to 1 (for example 01:00:00:00:00:00), in most cases the MAC multicast address is created from a IP multicast address as shown in Figure 41.

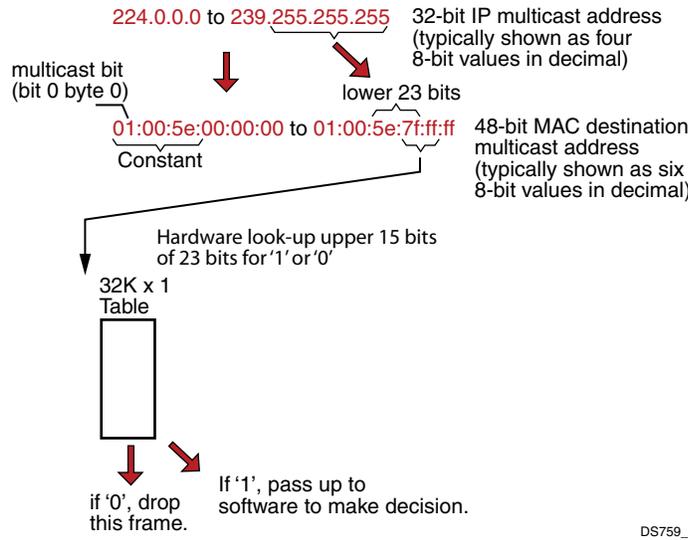


Figure 41: Mapping IP Multicast Addresses to MAC Multicast Addresses

When a multicast address frame is received while this extended multicast filtering is enabled, the AXI Ethernet first verifies that the first 24 bits are 01:00:5E and then will use the upper 15 bits of the unique 23 bit MAC multicast address to index this memory. If the associated memory location contains a 1 then the frame is accepted and passed up to software for a comparison on the full 23-bit address. If the memory location is a 0 or the upper 24 bits are not 01:00:5E then the frame is not accepted and it is dropped.

The memory is 1-bit wide but is addressed on 32-bit word boundaries. The memory is 32K deep. This table must be initialized by software via the AXI4-Lite interface

When using the extended multicast address filtering, the TEMAC must be set to promiscuous mode so that all frames are available for filtering. When doing this the TEMAC no longer checks for a unicast address match. Additional registers (UAWL and UAWU) are available to provide unicast address filtering while in this mode.

For builds that have the extended multicast address filtering enabled, promiscuous mode can be achieved by making sure that the TEMAC is in promiscuous mode and by clearing the EMultiFltrEnbl bit (bit 19) in the Reset and Address Filter register (RAF).

Please see the section on Extended Multicast Filtering for more details ([Extended Multicast Address Filtering Mode](#), page 73).

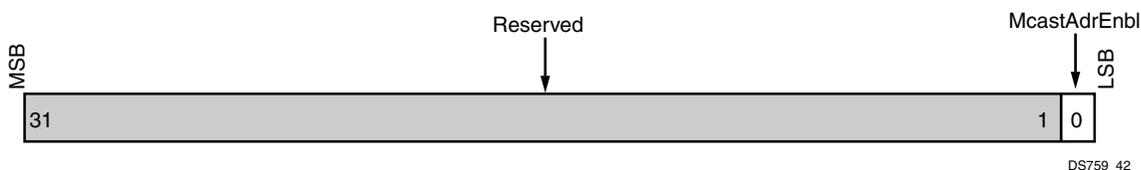


Figure 42: Multicast Address Table entry (offset 0x0002\_0000-0x0003\_FFFF)

Table 40 shows the Multicast Address Table bit definitions.

Table 40: Multicast Address Table Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	Read	0x0	<b>Reserved:</b> These bits are reserved for future definition and will always return zero.
0	McastAdrEnbl	Read/Write	0	<b>Multicast Address Enable:</b> This bit indicates that the received multicast frame with this upper 15 bits of the unique 23-bit MAC multicast address field should be accepted or rejected. 0 - Drop this frame 1 - Accept this frame

**Using the Address Filters**

There are 4, 4-bit (6 byte) registers, that can be used for address filtering. The address filters can be accessed by first setting the Filter Mask Index in the Filter Mask Index Register. While the Filter Mask Index is set, the Address Filter Registers can be set accessed. Please refer to Figure 43.

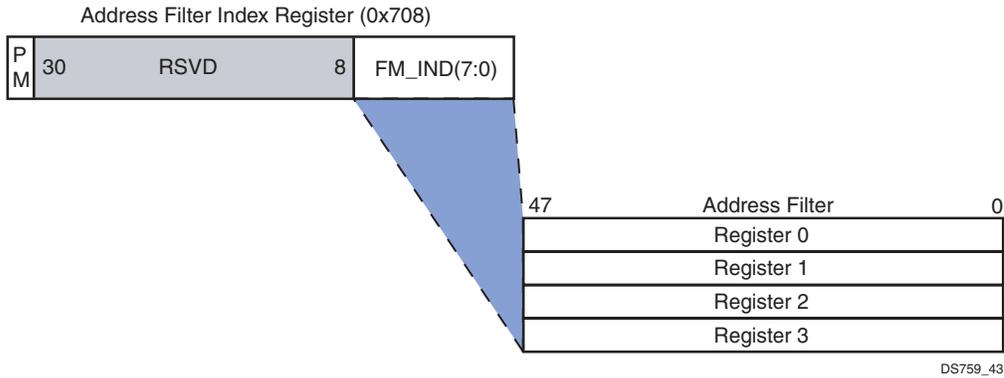


Figure 43: Address Filter Access

**Using the MII Management to Access Internal or External PHY Registers**

The MII Management interface is used to access PHY registers either in devices external to the FPGA or, in the case of SGMII or 1000BASE-X PHYs, PHY registers internal to the Hard TEMAC silicon component as described in Internal 1000BASE-X PCS/PMA Management Registers, page 96 and Soft TEMAC Implementations, page 102.

Prior to any MII Management accesses taking place, the MII Management Configuration register must be written with a valid CLOCK\_DIVIDE value and the MDIOEN bit must be set.

The determination as to which PHY registers are accessed, is by the value of the PHYAD field in the MII Management Control register. Each PHY, internal or external, should have a unique 5-bit PHY address excluding “00000” which is define as a broadcast PHY address.

The MII Management interface is defined in IEEE Std 802.3, Clause 22 as a two-wire interface with a shared bi-directional serial data bus and a clock with a maximum permitted frequency of 2.5 MHz. As a result, MII Management access can take many AXI4-Lite clock cycles to complete.

To write to a PHY register, the data must be written to the MII Management Data Write register. The PHY address (PHYAD) and PHY Register (REGAD) be written to the MII Management Control Register. Setting the Initiate bit in the MII Management Control Register starts the operation. The format of the PHYAD and REGAD in the MII Management Control Register is shown in Figure 44.

To read from a PHY register, the PHY address and register number are written to the MII Management Control Register. Setting the Initiate bit in the MII Management Control Register starts the operation. When the operation completes, the PHY register value is available in the MII Management Read Data Register.

To access the internal SGMII or 1000BASE-X registers, the PHYAD should match that set by the parameter C\_PHYADDR.

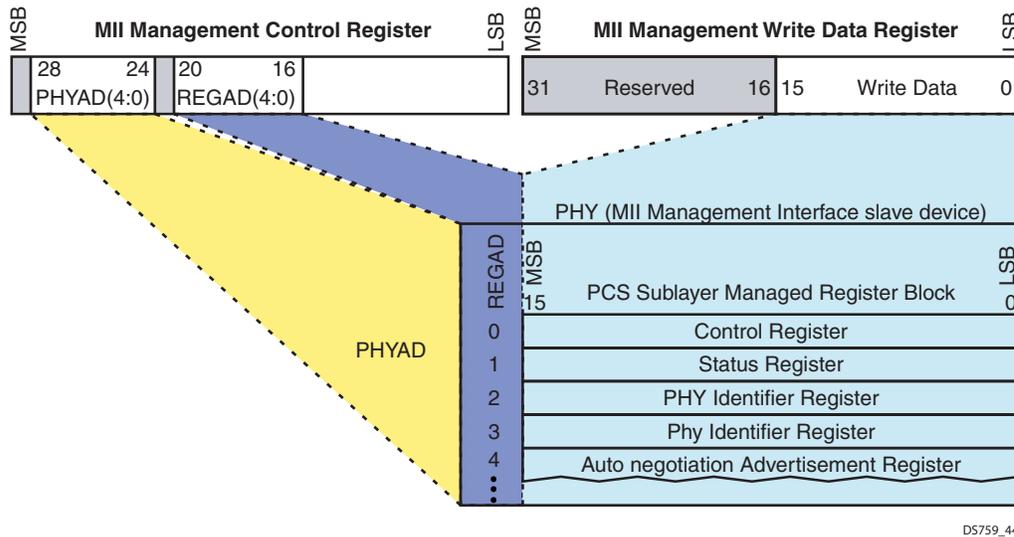


Figure 44: MII Management Write Register Field Mapping

Table 41 provides an example of a PHY register Write via the MII Management Interface.

Table 41: Example of a PHY Register Write via the MII Management Interface

Register	Access	Value	Activity
MIIM Write Data Reg	Write	0x0000ABCD	Write the value that will be written to the PHY register (we chose 0xABCD for this case).
MII Management Control Register	Write	0x01024800	Initiate the write to the MII Management Control register by setting the PHYAD (00001), REGAD(00010), OP (01), and Initiate bit (1).
MII Management Control Register	Read	0x01024880	Poll the MII Management Control register bit 7. When set to “1”, the data has been written.

Table 42: Example of a PHY Register Read via the MII Management Interface

Register	Access	Value	Activity
MII Management Control Register	Write	0x01028800	Initiate the write to the MII Management Control register by setting the PHYAD (00001), REGAD(00001), OP (10), and Initiate bit (1).
MII Management Control Register	Read	0x01028880	Poll the MII Management Control register bit 7. When set to “1”, the read data is available.
MII Management Read Data Register	Read		Read data provided by PHY register.

After a transfer has been initiated on the MDIO interface, it is also possible to access a non-MDIO register in the memory space normally. The MDIO transfer has completed when the RDY bit in the MII Management Control register is “1”. This bit can either be polled, or the interrupt can be monitored.

If the MII Management Control register is rewritten in an attempt to start a new transfer, the data will be captured; however, the transfer will not take place until the current transaction completes. If the previous transaction were a read, the read data will be valid when the first transaction completes. If the previous transaction were a write, the MII Management Write Data register can be written after the first transaction completes.

The MII Management Control register should be checked to ensure all MDIO transactions have been completed before accessing the data or initiating a transfer.

## Including or Excluding I/O in the Physical Interfaces

To allow the AXI Ethernet to be easy to use, the core includes BUFG, IBUFG, IBUF, OBUF and other FPGA resources to correctly connect the external interface signals to the FPGA I/O.

Some users may find that this prevents them from being able to make custom connections on these signals which may be required for their system. By setting the parameter `C_INCLUDE_IO` to "0", these resources will not be automatically provided. In this case the user will be responsible for making the appropriate connections.

## Partial TCP/UDP Checksum Off Load in Hardware

When using TCP or UDP Ethernet protocols, data integrity is maintained by calculating and verifying checksum values over the TCP and UDP frame data. Normally this checksum functionality is handled by the protocol stack software which can be relatively slow and use significant processor utilization for large frames at high Ethernet data rates.

An alternative is to off load some of this transmit checksum generation and receive checksum verification in hardware. This is possible by including checksum off loading in the AXI Ethernet using parameters. Including the checksum off load functions are a trade off between using more FPGA resources and getting higher Ethernet performance while freeing up processor use for other functions.

When using the TCP/UDP checksum off load function, checksum information is passed between the software and the AXI Ethernet by using AXI4-Stream Control and AXI4-Stream Status interface. [Table 43](#), [Table 45](#), [Figure 46](#), [Table 47](#), [Table 48](#), [Table 49](#), [Table 50](#), [Table 51](#), [Table 52](#), and [Figure 48](#) show the checksum off load fields.

The use of the TCP / UDP checksum off load function requires that the core connected to the AXI Ethernet via the AXI4-Stream Control and AXI4-Stream Data interfaces. Please refer to the [Mapping Xilinx AXI DMA Buffer Descriptor Fields to AXI4-Streaming Fields](#) section for more information.

`TX_CSBEGIN` is the beginning offset which points to the first byte that needs to be included in the checksum calculation. The first byte is indicated by a value of zero. The beginning position must be 16 bit aligned. With TCP and UDP you would want to set this value to skip over the Ethernet frame header as well as the IP datagram header so that the checksum calculation is started in the proper place in the TCP or UDP segment. Operating systems may provide functions to calculate this value as it is normally variable based on the variable IP datagram header size. In all cases, the `TX_CSBEGIN` value must be 14 or larger to be valid.

`TX_CSINSERT` is the offset which points to the location where the checksum value should be written into the TCP or UDP segment header. This value must be 16 bit aligned and can not be in the first 8 bytes of the frame. Again, operating systems may provide functions to calculate this value as it is normally variable based on the variable IP datagram header size.

`TX_CSCNTRL` is a 16 bit field however only the least significant bit is defined. This bit will control the insertion of the checksum into the frame data. If set to a "1" then the checksum will be written into the transmit frame otherwise not modification of the frame will occur.

TX\_CSINIT is a 16-bit seed that can be used to insert the TCP or UDP pseudo header into the checksum calculation. In many cases the protocol stack will calculate the pseudo header checksum value and place it in the header checksum field of the transmit frame. In those cases this field should be zeroed. If the protocol stack does not provide the pseudo header checksum in the header checksum field location of the transmit frame, then that field should be zeroed and the pseudo header checksum value must be calculated and placed in the TX\_CSINIT field of the buffer descriptor.

In order for the transmit checksum to be calculated correctly, the transmit Ethernet FCS must not be provided as part of the transmit data and the transmit FCS calculation and insertion must be enabled in the AXI Ethernet.

There is a special case for checksums of UDP datagrams. From the UDP RFC 768:

If the computed checksum is zero, it is transmitted as all ones (the equivalent in one's complement arithmetic). An all zero transmitted checksum value means that the transmitter generated no checksum (for debugging or for higher level protocols that don't care).

If the frame encapsulates a UDP datagram, and if the resulting checksum is zero, then a value of all ones is used. This case does not exist for TCP because a checksum of zero is legal.

RX\_CSRAW is the raw receive checksum calculated over the entire Ethernet payload. It is calculated starting at byte 14 of the Ethernet frame with the count starting at zero, not one (the byte following the Type/Length field) and continues until the end of the Ethernet frame. If the receive Ethernet FCS stripping is not enabled in the AXI Ethernet, the FCS will also be included in the checksum. The application is required to calculate the checksum of the fields which should not have been included to subtract them from the RAW checksum value. In most cases, the protocol software which allows receive checksum off loading will require a pass or fail indication. The application will have to compare the adjusted raw checksum value with the checksum field of the TCP or UDP header and provide the pass or fail indication.

## AXI4-Stream Interface

The Ethernet frame data to be transmitted and the frame data that is received passes between the AXI Ethernet and the rest of the embedded system via AXI4-Stream interfaces. In many cases the other end of the AXI4-Stream interfaces will be connected to a soft IP DMA controller implemented in FPGA fabric.

However, any custom logic may be used to connect to the AXI4-Stream interface as long as it meets the requirements of the AXI Ethernet AXI4-Stream interface.

The AXI4-Stream interface is a high-performance, synchronous, point-to-point connection which, in its general use case, is described in its specification listed in the [Reference Documents, page 120](#) section.

This section will describe the specific 32-bit implementation used by the AXI Ethernet core to transfer transmit and receive Ethernet frame data with the rest of the embedded system.

The AXI4-Stream model used is called *Packetized* and *Aligned Strobe* which is defined in the subsequent sections.

### Packetized

Data is transferred in packets rather than as a continuous stream. The signals \*\_TLAST are used to indicate the last 32-bit word of a packet being transferred.

### Aligned Strobe

A write strobe is used for each byte (\*\_TSTRB(3:0)) in the data bus (4 write strobes in our case). Null strobes are not allowed at the beginning, in the middle of a transfer, or at the end of a transfer. This means that the first word

transferred and every additional word up until the last must contain a valid 32-bit value. The last word may be sparse which means it may contain 4, 3, 2, or 1 valid byte(s) aligned to the right and the write strobes will be used to indicate which bytes are valid. \*\_TLAST is used to indicate the last data of a frame.

In some cases the write strobe signals may be tied to the active state ("1"). This will be discussed later in this document.

## Throttling

The driver of the AXI4-Stream will use the \*\_TVALID to throttle during a transfer. By taking \*\_TVALID inactive the current transfer is held until it is active again. The receiver of the AXI4-Stream will use the \*\_TREADY signal to throttle during a transfer. By taking \*\_TREADY inactive the current transfer is held until it is active again.

## Dual Channel AXI4-Stream

The transmit AXI4-Stream interface utilizes two AXI4-Stream busses. The AXI4-Stream Data Bus is used for frame data only while the AXI4-Stream Control Bus contains control information. Similarly, the receive AXI4-Stream interface utilizes two AXI4-Stream busses. The AXI4-Stream Data Bus is used for frame data only, and the AXI4-Stream Status Bus provides status information.

The control/status and data busses must have the same clock source but there is no synchronization between the two busses with regards to frame to frame data.

The transmit AXI4-Stream control bus may be configured to use one of two format types; Normal Transmit or Receive Status Transmit. This configuration is controlled by the first nibble (4-bits aligned left) of the first word transferred on the transmit control bus and the receive status bus. A value of 0xA identifies the transfer as a Normal Transmit control packet. A value of 0x5 identifies the transfer as a Receive Status packet. All other values are currently undefined and are ignored. These transfer types will be defined in detail later in this document.

The receive AXI4-Stream interface only supports one format type.

## Functional Description

The AXI4-Stream interface transfers data in one direction only. The Ethernet transmit interface will use an AXI4-Stream Data interface and an AXI4-Stream Control interface. The Ethernet receive interface will use an AXI4-Stream Data interface and an AXI4-Stream Status interface.

The AXI4-Stream interfaces used in this implementation are 32-bits wide, have side-band control signals, and will typically operate with a clock between 100 and 125 MHz.

Data is transferred across the AXI4-Stream Data interfaces. Additional control information is transferred across the transmit AXI4-Stream Control interface and additional status information is transferred across the receive AXI4-Stream Status interface.

For the transmit data path the *Source* will be the embedded system, typically a DMA controller, and the *Destination* will be the AXI Ethernet. For the receive data path the *Source* will be the AXI Ethernet and the *Destination* will be the embedded system, typically a DMA controller.

Control signals are used to mark the start and end of data across the AXI4-Stream interfaces as well as to signal the readiness of the Source and Destination and to indicate which bytes in the 32-bit path contain valid data. The destination uses the \*\_TREADY signal to indicate it is able to receive data, while the source uses \*\_TVALID to indicate when valid data is on the bus and the \*\_TLAST signal to indicate the last 8, 16, 24, or 32 bits of data.

## Transmit AXI4-Stream Interface

The transmit control block must maintain coherence between the data and control busses. Since data frames may vary from 1 byte to over 9 kb in length and the control information for each frame is a constant, six 32-bit words, care must be taken under conditions where the buffer for the frame data or control data fills up to prevent an out of sequence condition to occur. To maintain coherency, the AXI4-Stream data ready signal is held **not ready** until a AXI4-Stream control stream has been received. Once this has occurred, the AXI4-Stream data ready signal will be driven **ready** (as long as there is buffer space available) and the AXI4-Stream control ready signal will be held **not ready** until the data stream transfer is complete.

Please refer to [Figure 45](#) and [Figure 47](#). Note that the write strobe signals for the control and status busses are always in the active state (0xF). Also note that the right most write strobe signal for the data bus is always in the active state (0x1, 0x3, 0x7, or 0xF). These signals may be tied off rather than routing signals from the AXI4-Stream source to the destination. The AXI Ethernet core will provide these ports to be compliant with the standard; however, there will not be any logic based on these inputs which will be considered constants.

The transmit interface may encounter two AXI4-Stream transfer types; Normal Transmit or Receive Status Transmitt

### Normal Transmit AXI4-Stream Transfer - Flag=0xA

The Normal Transmit transfer is utilized to connect AXI Ethernet to an external core. [Figure 45](#) illustrates the waveforms when connected to a core such as AXI\_DMA or AXI\_FIFO\_MM\_S. AXI\_DMA supports advanced features such as partial CSUM offloading of extended VLAN features; however, AXI\_FIFO\_MM\_S does not support any of the advance features.

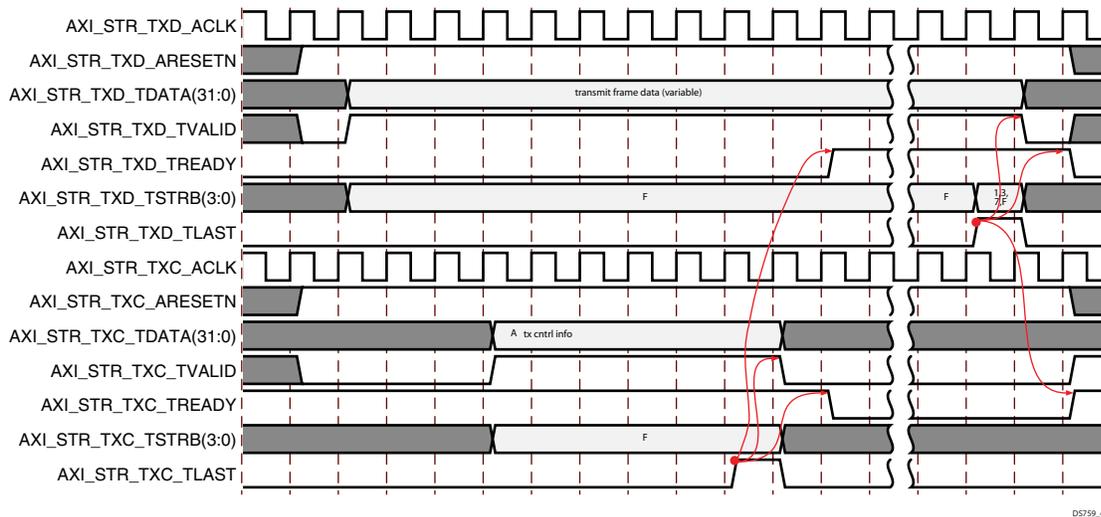


Figure 45: Normal Transmit AXI4-Stream Waveform

### Normal Transmit AXI4-Stream Control Words

The Normal Transmit AXI4-Stream Control frame always contains six 32-bit control words (words 0 to 5). Of these words, only control words 0, 1, 2, and 3 are used by the AXI Ethernet. [Figure 46](#), [Table 43](#), [Table 45](#), and [Table 46](#) show the definitions of these words.

If the transmit AXI4-Stream control word bits 1:0 are “00” (TX\_CSCNTRL is disabled) or if the parameter C\_TXCSUM is “0” (the transmit checksum off load function is not included in build), then none of the transmit AXI4-Stream control words are used and no transmit checksum off load will take place.

If the parameter C\_TXCSUM is “1”, then transmit checksum off load can be controlled on a frame by frame basis by setting or clearing the transmit AXI4-Stream control word 1 bits 1:0 to “01” (TX\_CSCNTRL).

For more details about how the transmit AXI4-Stream control words are used for transmit checksum off load, please see [Partial TCP/UDP Checksum Off Load in Hardware](#), page 58.

The transmit AXI4-Stream Data strobes are used to indicate how many bytes in the last 32-bit word of the payload are valid data. A “1” is used to indicate valid bytes. For example, AXI\_STR\_TXD\_STRB(3:0) = “0001” would indicate that only the first byte of the last word of the payload [AXI\_STR\_TXD(7:0)] is valid and the remaining three bytes are unused. AXI\_STR\_TXD\_STRB(3:0) = “0011” would indicate that the first two bytes of the last word of the payload [Axi\_Str\_TxD(15:0)] are valid and the remaining two bytes are unused.

Refer to [Figure 46](#) for the Transmit AXI4-Stream Control Word definition.

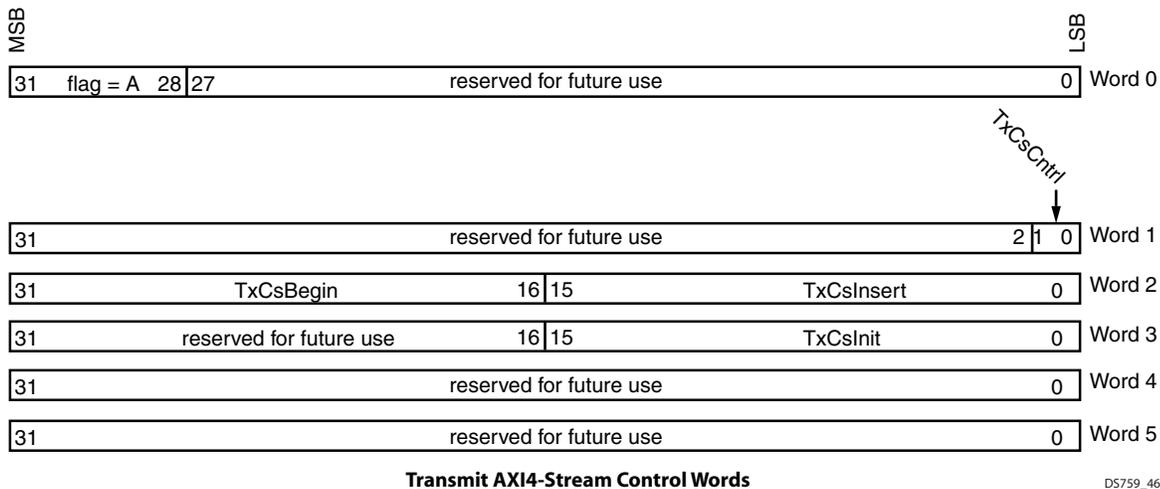


Figure 46: Transmit AXI4-Stream Control Words

Table 43: Transmit AXI4-Stream Control Word 0 - TAG

Bit(s)	Name	Description
31-28	Flag	1010 = Normal Transmit Frame 0101 = Receive Status Transmit Frame All other selections are reserved.
27-0	Reserved	Reserved for future use

Table 44: Transmit AXI4-Stream Control Word 1- APP0

Bit(s)	Name	Description
31-2	Reserved	Reserved for future use
1-0	TxCsumCntrl	<b>Transmit Checksum Enable:</b> 00 = No transmit checksum offloading should be performed on this frame 01 = Partial transmit checksum offloading should be performed on this frame based upon other data provided in the control words. For the partial checksum to be performed, C_TXCSUM must be set to 1. 10 = Reserved 11 = Reserved

Table 45: Transmit AXI4-Stream Control Word 2- APP1

Bit(s)	Name	Description
31-16	TxCsBegin	<b>Transmit Checksum Calculation Starting Point:</b> This value is the offset to the location in the frame to the first byte that needs to be included in the checksum calculation. The first byte is indicated by a value of zero. The beginning position must be 16-bit aligned.
15-0	TxCsInsert	<b>Transmit Checksum Insertion Point:</b> This value is the offset to the location in the frame where the checksum value should be written into the TCP or UDP segment header. The value must be 16-bit aligned and cannot be in the first 8 bytes of the frame. It also should not contain a value that exceeds the length of the frame.

Table 46: Transmit AXI4-Stream Control Word 3- APP2

Bit(s)	Name	Description
31-16	Reserved	Undefined value.
15-0	TxCsInit	<b>Transmit Checksum Calculation Initial Value:</b> This value is a 16-bit seed that can be used to insert the TCP or UDP pseudo header into the checksum calculation. please see <a href="#">Partial TCP/UDP Checksum Off Load in Hardware, page 58</a> for more information on using this field.

### Receive Status Transmit AXI4-Stream Transfer - Flag=0x5

The Receive Status transfer is utilized when the receive AXI4-Stream interface is tied directly to the transmit AXI4-Stream interface for the purpose of looping back Ethernet receive data to the Ethernet transmit interface with no external intervention. In that case the status transfer will enable the receive data frame to be presented to the TEMAC transmitter and the status content will be ignored. Obviously no advanced checksum off load or VLAN functions will be allowed for these operations even if they were included in the core at build time. Note the different identification flag value in [Figure 47](#).

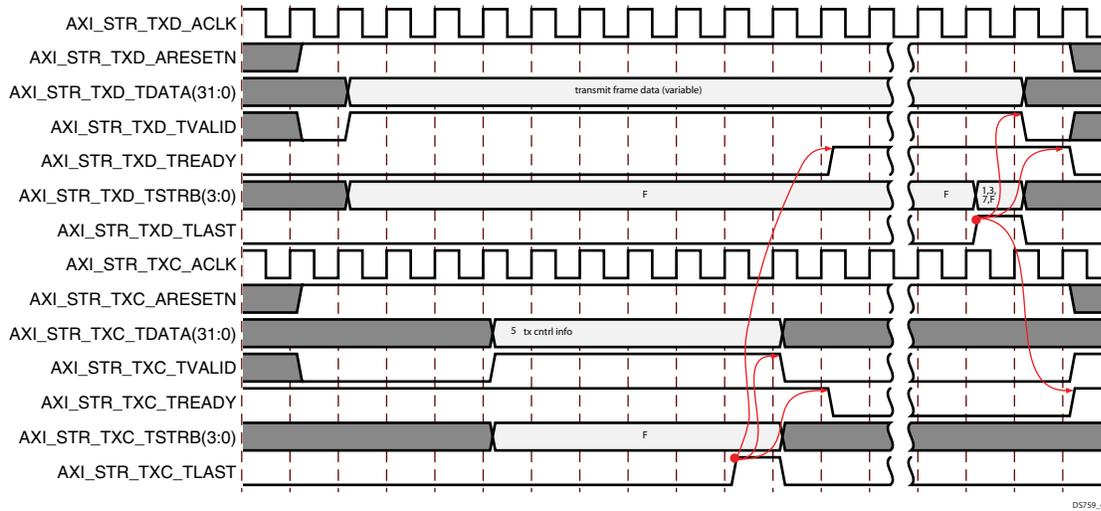


Figure 47: Receive Status Transmit AXI4-Stream Waveform

### Receive AXI4-Stream Interface

Unlike the transmit AXI4-Stream Control interface, the receive AXI4-Stream Status interface has only one format type (TAG/FLAG).

The receive interface has been designed to allow throttling on both the AXI4-Stream Status bus and the AXI4-Stream Data bus. After receiving ethernet data, the receive interface transfers the AXI4-Stream Status information before the AXI4-Stream Data information. Please refer to Figure 50 for a receive waveform diagram. This diagram shows what signals are required when connected to a core such as AXI\_DMA. When connecting to a core such as AXI\_FIFO\_MM\_S, a signal minimization can be made because the receive status bus information is not required. In this case, the external core must actively drive the signals AXI\_STR\_RXS\_ACLK and AXI\_STR\_RXS\_ARESETN, AXI\_STR\_RXS\_TREADY must be tied HIGH, and all of the AXI\_STR\_RXS\* inputs to the external core can be left open.

For the loop back of the receive AXI4-Stream to transmit AXI4-Stream to work, the receive AXI4-Stream Data bus will be throttled by the transmit AXI4-Stream Data bus until the receive AXI4-Stream Status has been received by the transmit channel.

### Receive AXI4-Stream Status Words

The receive AXI4-Stream Status frame always contain six 32-bit status words (words 0 to 5). Figure 48, Table 47, Table 48, Table 49, Table 50, Table 51, and Table 52 show the definitions of these words. Reserve fields do not have defined values.

If the parameter C\_RXCSUM is “0”, the receive checksum off load function is not included in the build and receive AXI4-Stream Status word 4, bits 15-0 will always be zero. If C\_RXCSUM is “1”, the raw checksum will be calculated for every frame received and will be placed in the receive AXI4-Stream Status word 4. For more information about using the receive raw checksum value, please see Partial TCP/UDP Checksum Off Load in Hardware, page 58.

Receive AXI4-Stream Status word 5, bits 15-0 will always contain the number of bytes in length of the frame being sent across the receive AXI4-Stream Status interface.

The AXI\_STR\_RXD\_STRB(3:0) bus is used to indicate how many bytes in the last 32-bit word of the AXI4-Stream Data bus. A “1” is used to indicate valid bytes. For example, AXI\_STR\_RXD\_STRB(3:0) = “0001” would indicate that only the first byte of the last word of the AXI4-Stream Data bus [AXI\_STR\_RXD\_DATA(7:0)] is valid and the

remaining three bytes are unused. AXI\_STR\_RXD\_STRB(3:0) = "0011" would indicate that the first two bytes of the last word of the payload [AXI\_STR\_RXD\_DATA(15:0)] are valid and the remaining two bytes are unused.

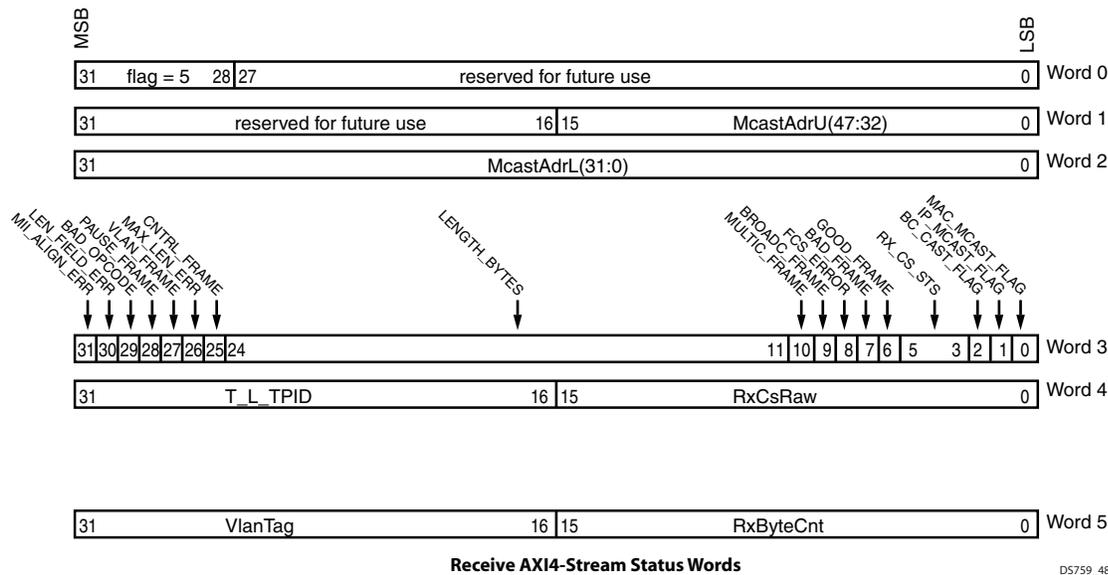


Figure 48: Receive AXI4-Stream Status Words

Table 47: Receive AXI4-Stream Status Word 0 - TAG

Bits(s)	Name	Description
31-28	Flag	0x5 = Receive Status Frame
27-0	Reserved	Undefined value.

Table 48: Receive AXI4-Stream Status Word 1 - APP0

Bits(s)	Name	Description
31-16	Reserved	Undefined value.
15-0	MCAST_ADR_U	<b>Multicast Address (47:32):</b> These are the upper 16 bits of the multicast destination address of this frame. This value is only valid if the AXI4-Stream Status word 2 bit 0 is a 1. The address is ordered so the first byte received is the lowest positioned byte in the register; for example, MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA. This word would be 0xFFEE.

Table 49: Receive AXI4-Stream Status Word 2- APP1

Bits(s)	Name	Description
31-0	MCAST_ADR_L	<b>Multicast Address (31:0):</b> These are the lower 32 bits of the multicast destination address of this frame. This value is only valid AXI4-Stream Status word 2 bit 0 is a 1. The address is ordered so the first byte received is the lowest positioned byte in the register; for example, MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA. This word would be 0xDDCCBBAA.

Table 50: Receive AXI4-Stream Status Word 3- APP2

Bit(s)	Name	Description
31	MII_ALIGN_ERR	<b>MII Alignment Error:</b> Used in 10/100 MII mode. Asserted if the previous frame received has an incorrect FCS value and a misalignment occurs when the 4-bit MII data bus is converted to the 8-bit GMII data bus.
30	LEN_FIELD_ERR	<b>Length Field Error:</b> Asserted if the LT field contains a length value that does not match the number of Ethernet MAC client data bytes received. Also asserted High if the LT field indicates that the frame contains padding but the number of Ethernet MAC client data bytes received is not equal to 64 bytes (minimum frame size). This bit is not defined when LT field error-checks are disabled or when received frames are less than the legal minimum length.
29	BAD_OPCODE	<b>Bad OP Code:</b> Asserted if the previous frame is error free. Contains the special control frame identifier in the LT field, but contains an OPCODE unsupported by the Ethernet MAC (any OPCODE other than PAUSE).
28	PAUSE_FRAME	<b>Pause Frame:</b> Asserted if the previous frame is error-free. Contains the special control frame identifier in the LT field. Contains a destination address matching either the Ethernet MAC control multicast address or the configured source address of the Ethernet MAC. Contains the supported PAUSE OPCODE and is acted upon by the Ethernet MAC.
27	VLAN_FRAME	<b>VLAN Frame:</b> Asserted if the previous frame contains a VLAN identifier in the LT field when receiver VLAN operation is enabled.
26	MAX_LEN_ERR	<b>Maximum Length Error:</b> Asserted if the previous frame exceeded the specified IEEE Std 802.3-2005 maximum legal length. This is only valid if jumbo frames are disabled.
25	CNTRL_FRAME	<b>Control Frame:</b> Asserted if the previous frame contains the special control frame identifier in the LT field.
24 - 11	LENGTH_BYTES	<b>Length Bytes:</b> The length of the previous frame in number of bytes. The count sticks at 16383 for any jumbo frames larger than this value.
10	MULTIC_FRAME	<b>Multicast Frame:</b> Asserted if the previous frame contains a multicast address in the destination address field.
9	BROADC_FRAME	<b>Broadcast Frame:</b> Asserted if the previous frame contained the broadcast address in the destination address field.
8	FCS_ERR	<b>FCS Error:</b> Asserted if the previous frame received has an incorrect FCS value or the Ethernet MAC detects error codes during frame reception.
7	BAD_FRAME	<b>Bad Frame:</b> Asserted if the previous frame received contains errors.
6	GOOD_FRAME	<b>Good Frame:</b> Asserted if the previous frame received is error-free.
5-3	RX_CS_STS	<b>Receive CSUM Status:</b> Reserved: These bits are tied to Zero.
2	BCAST_FLAG	<b>Broadcast Frame Flag:</b> This bit, when 1, indicates that the current frame is a Broadcast frame that has passed the hardware address filtering.
1	IP_MCAST_FLAG	<b>IP Multicast Frame Flag:</b> This bit, when 1, indicates that the current frame is a multicast frame that appears to be formed from an IP multicast frame (the first part of the destination address is 01:00:5E) that has passed the hardware multicast address filtering.
0	MAC_MCAST_FLAG	<b>MAC Multicast Frame Flag:</b> This bit, when 1, indicates that the current frame is a MAC multicast frame that has passed the hardware multicast address filtering.

Table 51: Receive AXI4-Stream Status Word 4- APP3

Bit(s)	Name	Description
31-16	T_L_TPID	<b>Type Length VLAN TPID:</b> This is the value of the 13th and 12th bytes of the frame (index starts at zero). If the frame is not VLAN type, this will be the type/length field. If the frame is VLAN type, this will be the value of the VLAN TPID field prior to any stripping, translation or tagging.

Table 51: Receive AXI4-Stream Status Word 4- APP3

Bit(s)	Name	Description
15-0	RX_CSRAW	<b>Receive Raw Checksum:</b> This value is the raw receive checksum calculated over the entire Ethernet frame starting at byte 14 (index starts at zero). If the receive FCS stripping is not enabled, the FCS will be included in the checksum and must be removed by the application.

Table 52: Receive AXI4-Stream Status Word 5- APP4

Bit(s)	Name	Description
31-16	VLAN_TAG	<b>VLAN Priority CFI and VID:</b> This is the value of the 15th and 14th bytes of the frame (index starts at zero). If the frame is VLAN type, this will be the value of the VLAN priority, CFI, and VID fields prior to any stripping, translation, or tagging. If the frame is not VLAN type, this will be the first 2 bytes of the data field.
15-0	RX_BYTECNT	<b>Receive Frame Length (Bytes):</b> This value is the number of bytes in the Ethernet frame which is in the receive AXI4-Stream Data interface.

## Mapping Xilinx AXI DMA Buffer Descriptor Fields to AXI4-Streaming Fields

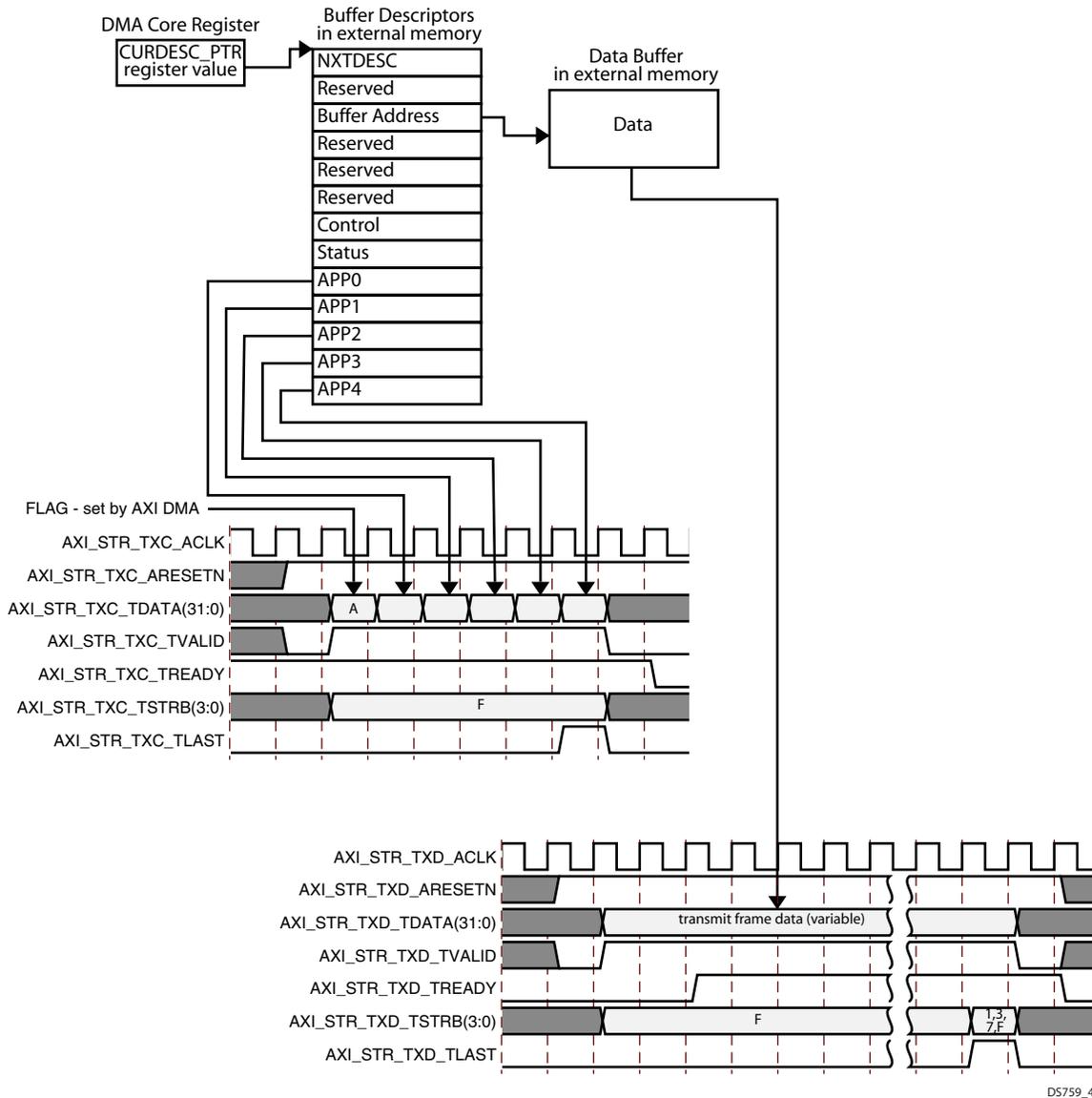
The AXI Ethernet requires that certain AXI4-Stream Control/Status words be used to support TCP / IP Checksum Off load. The AXI Ethernet does not have any requirements on how the AXI4-Stream words are created or where the data comes from, only that the correct values are in each field.

At the time that this document is written, Xilinx provides a core that may be used to provide the require AXI4-Stream functionality to implement TCP / IP Checksum Off load: AXI\_DMA\_v1\_00\_a. Please refer to the documents list in [Reference Documents, page 120](#) for more information.

The AXI DMA core is designed to operate with many AXI4-Stream cores in addition to the AXI Ethernet so their documents are necessarily general and do not make reference specifically to the data used for TCP/ IP Checksum Off load. This document will briefly show the mapping between how these two core's data maps to the fields in the AXI4-Stream for the purposes of TCP / IP Checksum Off load.

Please note that the information that follows is specific to these two core's implementation at the time that this document is written and that the implementation may change in the future. If the implementation of these two cores does change, this data sheet will not necessarily be updated to show the new implementation.

The AXI DMA core uses registers to point to data areas in external memory called Buffer Descriptors. The Buffer Descriptors are five 32-bit words in external memory and contain AXI DMA operation control information, pointers to other areas of external memory which contain data to move which are called Data Buffers, and generic Application Defined words which map to AXI4-Stream Control and AXI4-Stream Status words. [Figure 49](#) shows the mapping between the AXI DMA Buffer Descriptor words in external memory and the fields in the transmit AXI4-Stream case and [Figure 50](#) shows the mapping for the receive AXI4-Stream case. Please note that the first word in the AXI\_STR\_TXC\_TDATA data contains the Flag information that is directly set by the AXI DMA core, and the first word in the AXI\_STR\_RXS\_TDATA data contains the Flag information that is set by AXI Ethernet.



DS759\_49

Figure 49: Transmit AXI DMA Buffer Descriptor AXI4-Stream Field Mapping

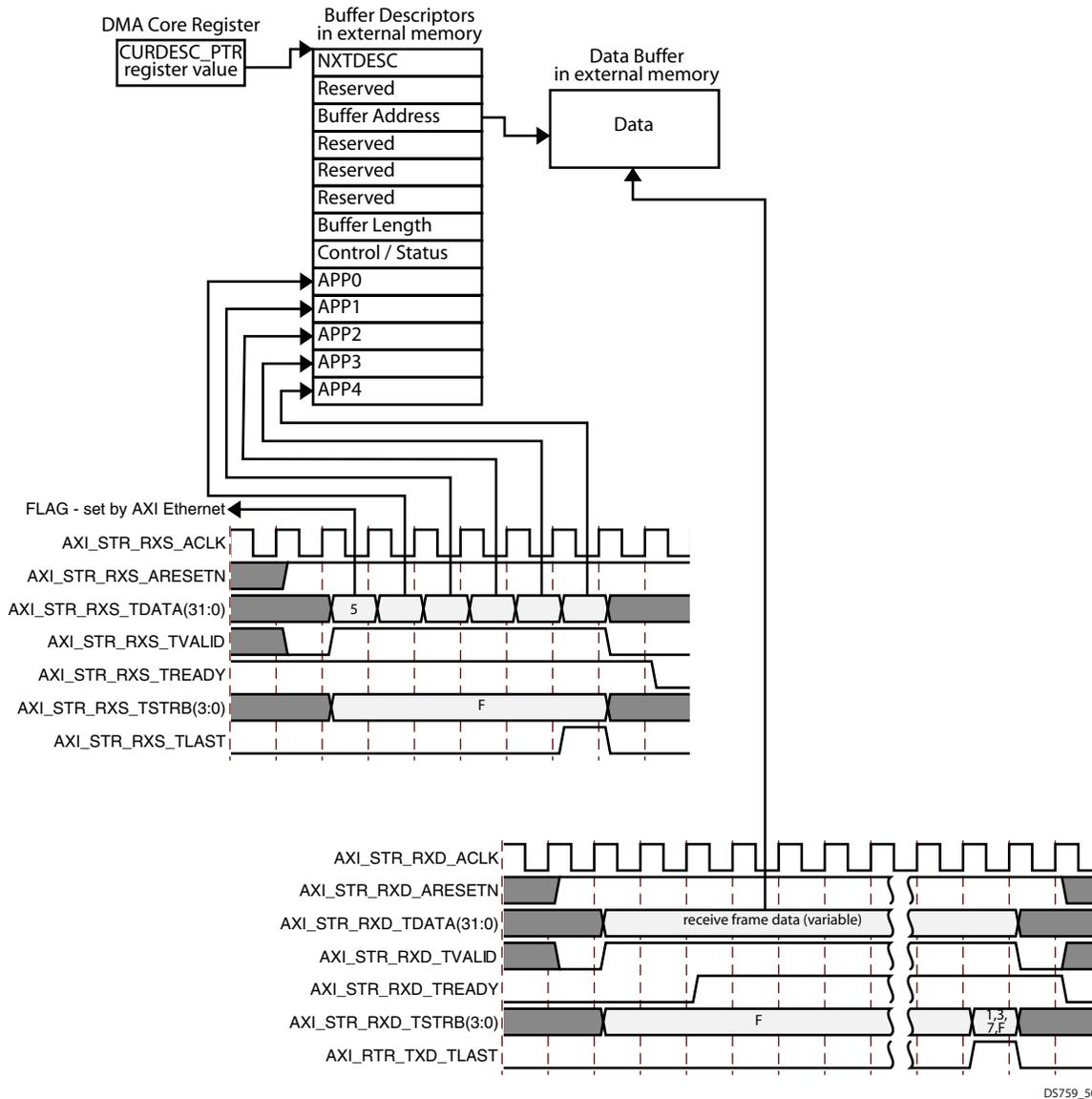


Figure 50: Receive AXI DMA Buffer Descriptor AXI4-Stream Field Mapping

## Frame Transmission

### Padding

When fewer than 46 bytes of data are supplied to the AXI Ethernet, the transmitter will add padding up to the minimum frame length. However, when the FCS field is being provided as part of the frame by the user, the frame must already be padded if necessary to maintain the minimum frame length.

### FCS Pass Through

The AXI Ethernet can calculate and add the FCS field to each transmitted frame or it can pass through an FCS field supplied with the frame data by the user. When a user supplied FCS field is passed through, the user must supply

padding as necessary to ensure that the frame meets the minimum frame length requirement. FCS insertion or pass through is controlled by the TC register bit 29 (page 40).

### Virtual LAN (VLAN) Frames

When transmitting VLAN frames (if enabled by the TC register bit 27 page 40) without extended VLAN mode, the user must supply the VLAN type tag 0x8100 as well as the two byte tag control field along with the rest of the frame data. More information about the tag control field is available in the IEEE Std 802.3-2002 specification.

### Maximum Frame Length and Jumbo Frames

The maximum length of a frame specified in the IEEE Std 802.3-2002 specification is 1518 bytes for non-VLAN tagged frames. VLAN tagged frames can be extended to 1522 bytes. When jumbo frame handling is disabled (TC register bit 30 page 40) and the user attempts to transmit a frame that exceeds the maximum legal length, the AXI Ethernet inserts an error code to corrupt the current frame and the frame is truncated to the maximum legal length. When jumbo frame handling is enabled, frames longer than the legal maximum are transmitted error free. Jumbo frames are restricted by the AXI Ethernet design to less than 16 kb.

## Frame Reception

### Frame Reception with Errors

An unsuccessful frame reception (for example, a fragment frame or a frame with an incorrect FCS) will be dropped and not passed to the user. A Receive Reject interrupt will be activated (see bit 28 in Table 10).

### FCS Pass Through or Stripping

If the Length/Type field has a length interpretation, the received frame could be padded to meet the minimum frame size specification. If FCS Pass Through is disabled (RCW1 register bit 29 page 39) and Length/Type field error checking is enabled (RCW1 register bit 25 page 39), the padding is stripped along with the FCS field and is not passed to the user. If FCS Pass Through is disabled (RCW1 register bit 29 page 39) and Length/Type field error checking is also disabled, the padding is not stripped and is passed to the user but the FCS field is stripped and is not passed to the user.

If the FCS Pass Through is enabled, any padding will be passed to the user along with the FCS field. Even though the FCS is passed up to the user, it is also verified and the frame will be dropped if the FCS is incorrect. A Receive Reject interrupt will be activated (see bit 28 in Table 10).

Table 53: Receive Frame FCS Field and Pad Field Stripping or Pass Through

	FCS Pass Through (RCW1 register bit 29 = 1)	FCS Strip (RCW1 register bit 29 = 0)
Length/Type field error check (RCW1 register bit 25 = 0)	FCS and padding (if present) fields passed to user for all accepted frames	FCS and padding (if present) fields stripped and not passed to user for all accepted frames
Length/Type field error ignore (RCW1 register bit 25 = 1)	FCS and padding (if present) fields passed to user for all accepted frames	FCS field stripped and not passed to user but padding (if present) passed to user for all accepted frames

## Virtual LAN (VLAN) Frames

Received VLAN tagged frames will be passed to the user if VLAN frame reception is enabled (RCW1 register bit 27 [page 39](#)). This is the basic native VLAN support provided by the TEMAC core. For more information about extended VLAN functions, please refer to those sections which follow.

## Maximum Frame Length and Jumbo Frames

The maximum length of a frame specified in the IEEE Std 802.3-2002 specification is 1518 bytes for non-VLAN tagged frames. VLAN tagged frames can be extended to 1522 bytes. When jumbo frame handling is disabled (RCW1 register bit 30 [page 39](#)) and a received frame exceeds the maximum legal length, the frame is dropped and a Receive Reject interrupt will be activated (see bit 28 in [Table 10](#)). When jumbo frame handling is enabled, frames longer than the legal maximum are received in the same way as shorter frames. Jumbo frames are restricted by the AXI Ethernet design to less than 16 K Bytes.

## Length/Type Field Error Checks

Length/Type field error checking is specified in IEEE Std 802.3. This functionality must be enabled (RCW1 register bit 25 [page 39](#)) to comply with this specification. Disabling Length/Type checking is intended only for specific applications, such as when using over a proprietary backplane.

### Enabled

When Length/Type error checking is enabled, the following checks are made on all frames received. (If either of these checks fails, the frame is dropped and a Receive Reject interrupt will be activated (see bit 28 in [Table 10](#)).

- A value greater than or equal to decimal 46 but less than decimal 1536 in the length/type field is checked against the actual data length received.
- A value less than decimal 46 in the length/type field is checked to ensure the data field is padded to exactly 46 bytes. The resultant frame is now the minimum frame size: 64 bytes total in length.

Additionally, if FCS passing is disabled, the length/type field will be used to strip the FCS field **AND** any padding that may exist. **NEITHER** will be passed to the user.

### Disabled

When the length/type error checking is disabled, the length/type error checking above is not performed and a frame that has only these errors will be accepted.

Additionally, if FCS passing is disabled, the length/type field is **NOT** used to determine padding that may exist and the FCS field **WILL** be stripped but any padding that may exist in the frame **WILL NOT** be stripped and **WILL** be passed to the user.

## Address Filtering

### Basic Mode

The receive address filtering function accepts or rejects received frames by examining the destination address field. Part of this function is carried out in the Hard TEMAC silicon component and part is carried out based on the bit settings in the Control Register (page 19). Figure 51 shows the address filtering flow. The decisions shown in white are made in the Hard TEMAC silicon component while the decisions shown in grey are made based on the Control Register settings.

The filtering functions includes:

Hard TEMAC Silicon component functions:

- Programmable unicast destination address matching
- Four programmable multicast address matching
- Broadcast address recognition (0xFFFF\_FFFF\_FFFF)
- Optional pass through mode with address filter disabled (promiscuous mode)
- Pause control frame address recognition (0x0100 00C2 8001)

Control Register enabled functions:

- Enable or reject received multicast frames
- Enable or reject received broadcast frames

Receive address filtering eliminates the software overhead required to process frames that aren't relevant to a particular Ethernet interface by checking the Destination Address (DA) field of the received frame.

The unicast address and multicast addresses are programmed in software via the AXI4-Lite bus as are the Address Filter enable bit, Multicast Address enable bit, and Broadcast Address enable bit. The pause frame address and broadcast address are predefined and do not need programming.

Please refer the footnote in Table 10, page 23 for a more detailed description on the conditions that can cause the receive reject interrupt to be set.

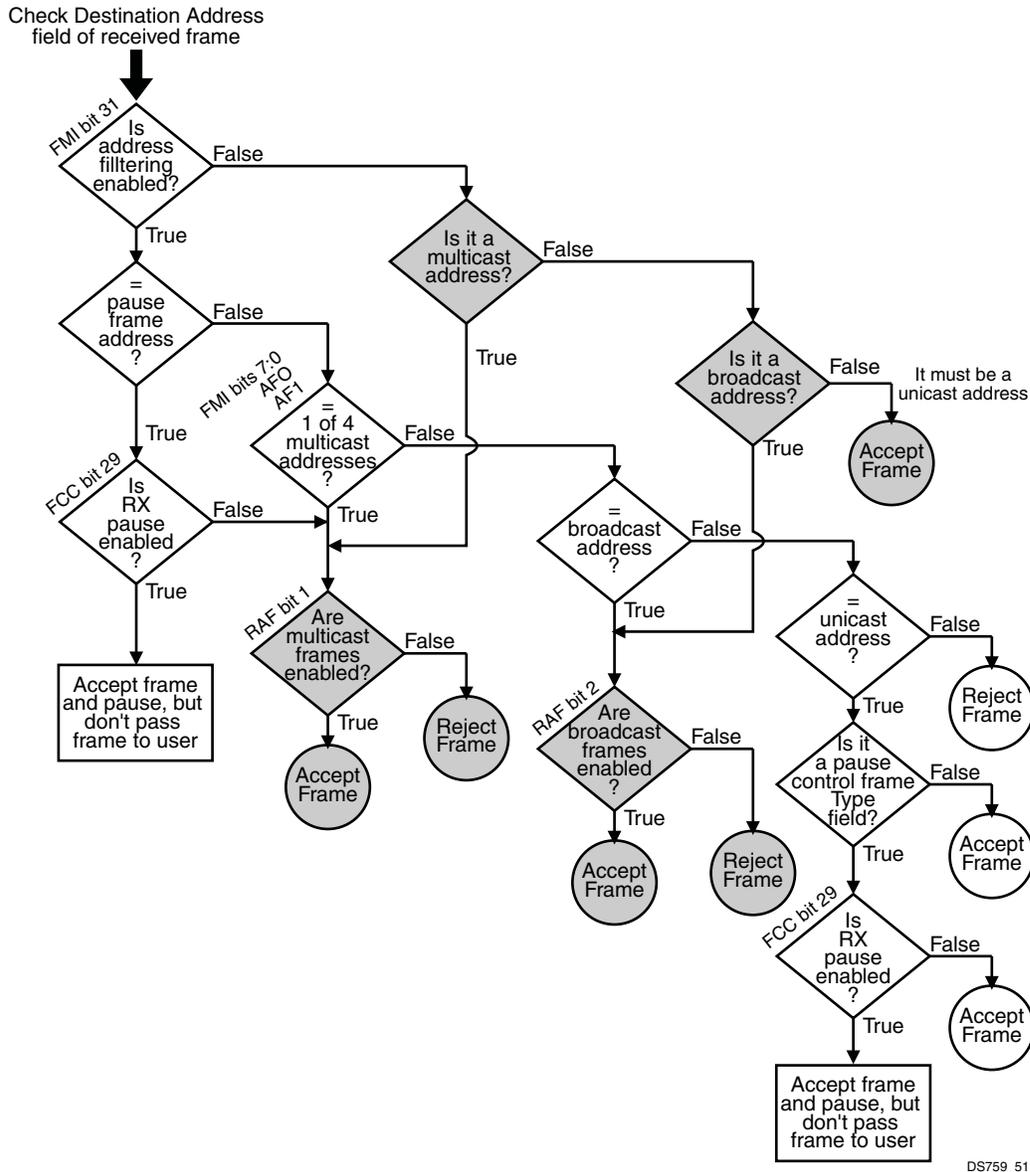


Figure 51: Receive Address Basic Filtering Flow

### Extended Multicast Address Filtering Mode

#### General

Currently the hard TEMAC core provides up to 4 multicast addresses that may be specified for receive address validation (i.e., if an incoming multicast frame’s receive address matches one of the 4 specified addresses, it is accepted). Some users require the ability to use many more multicast address values to filter receive addresses.

While this could be supported with promiscuous mode and software application filtering, some degree of hardware off loading is desired to reduce processor utilization.

Including extended multicast address filtering at build-time by setting parameters C\_MCAST\_EXTEND to 1 provides additional logic for address filtering beyond what is built in to the TEMAC core itself.

The TEMAC core will prevent receiving any multicast frames if they do not match one of the 4 entries in the built-in multicast address table. As a result, the TEMAC core will have to be placed in promiscuous address mode to force it to pass all multicast frames through to the extended multicast address filtering logic.

However, with the core in this mode means it will also pass through all unicast address frames. To not increase the processor load for unicast address filtering, additional unicast address filtering will have to be added to the extended multicast address filtering logic. The user must make sure that the TEMAC core is in promiscuous receive address mode when using this extended multicast address filtering mode.

**Implementation Details**

Received multicast frames that meet all other hardware verification requirements will receive a first level address filtering in hardware. Frames that pass this initial filtering will be passed up to software drivers with information provided by hardware to assist the software drivers in providing the second level/final address filtering. If the frame does not pass hardware filtering, the frame will be dropped and no action will be required by the software drivers.

While a MAC multicast address is defined as any 48 bit MAC address that has bit 0 (LSb) set to 1 (for example 01:00:00:00:00:00), in most cases the MAC multicast address is created from a IP multicast address as shown in Figure 52. It is these IP multicast addresses that are a subset of MAC multicast addresses that are filtered by the extended multicast address filtering mode.

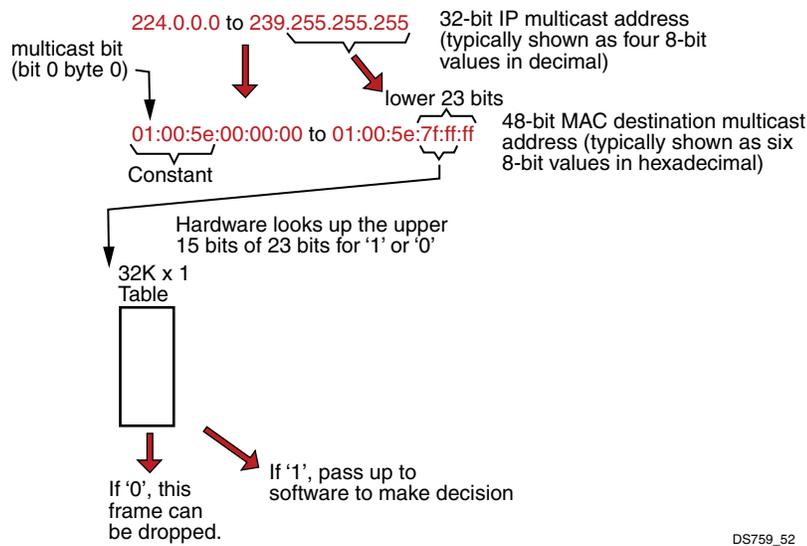


Figure 52: Mapping IP Multicast Addresses to MAC Multicast Addresses

When a multicast address frame is received while this extended multicast filtering is enabled, the AXI Ethernet first verifies that the first 24 bits are 01:00:5E and then will use the upper 15 bits of the unique 23 bit MAC multicast address to index this memory. If the associated memory location contains a 1 then the frame is accepted and passed up to software for a comparison on the full 23-bit address. If the memory location is a 0 or the upper 24 bits are not 01:00:5E then the frame is not accepted and it is dropped.

The memory is 1-bit wide but is addressed on 32-bit word boundaries. The memory is 32K deep. This table must be initialized by software via the AXI4-Lite interface

When using the extended multicast address filtering, the TEMAC must be set to promiscuous mode so that all frames are available for filtering. In this mode the TEMAC no longer checks for a unicast address match. Additional

registers [Table 14 shows the Receive VLAN Tag Register bit definitions](#), and [Unicast Address Word Upper Register \(UAWU\) - Offset 0x0000\\_0024](#) are available to provide unicast address filtering while in this mode.

For builds that have the extended multicast address filtering enabled, promiscuous mode can be achieved by making sure that the TEMAC is in promiscuous mode and by clearing the EMultiFltrEnbl bit (bit 19) in the [Reset and Address Filter Registers \(RAF\) - Offset 0x0000\\_0000](#).

When a received frame is accepted and passed up to software, additional information is provided in the receive AXI4-Stream Status words to help the software perform the additional address filtering with less overhead.

Receive AXI4-Stream Status words 0 and 1 include the destination address of the frame and word 2 includes bits to indicate if the frame had a destination address that was the broadcast address, a MAC multicast address, or an IP multicast address (and if none of those bits are set, it was a unicast address). Please see the section on [Mapping Xilinx AXI DMA Buffer Descriptor Fields to AXI4-Streaming Fields, page 67](#) for more information.

This allows the software to make decisions about the destination address without accessing the address from within the receive AXI4-Stream Data transfer. When using a Xilinx AXI DMA core, this means the information needed by the software for filtering is in the buffer descriptor and a decision can be made regarding accepting or rejecting the frame without accessing the data buffer itself thus reducing memory access and buffer indexing overhead.

## Flow Control

The flow control function is defined by IEEE Std 802.3-2002 Clause 31. The AXI Ethernet can be configured to send pause frames and to act upon the pause frames received. These two behaviors can be configured independently (asymmetrically). To enable or disable transmit and receive flow control, refer to the FCC register ([page 41](#)).

Flow control can be used to prevent data loss when an Ethernet interface is unable to process frames fast enough to keep up with the rate of frames provided by another Ethernet interface. When this occurs, the Ethernet interface that requires relief can transmit a pause control frame to the link partner to request it cease transmitting for a defined period of time.

### Transmitting a Pause Control Frame

For the AXI Ethernet, a pause frame transmission can be initiated by writing a pause value to the [Transmit Pause Frame Registers \(TPF\) - Offset 0x0000\\_0004, page 21](#) while transmit pause processing is enabled (FCC register bit 30 is 1 [page 41](#)).

Requesting the transmit of a pause frame will not interrupt a transmission in progress but the pause frame will be transmitted after the frame in progress. A request to transmit a pause frame will result in the transmission of a pause frame even if the transmitter itself is already paused due to the reception of a pause frame.

The destination address supplied with the transmitted pause control frame can be set by writing to the RCW0 and RCW1 registers ([page 43](#)).

### Receiving a Pause Control Frame

When an error free frame is received by the AXI Ethernet, it examines the following information:

1. The destination address field is compared to the pause control address and the configured unicast address.
2. The Length/Type field is compared against the control type code (0x8808).
3. The opcode field contents are matched against the pause control opcode (0x0001).

If compare step 2 or 3 fails or if flow control for the receiver is disabled (FCC register bit 29 is 0 [page 41](#)), the frame is ignored by the flow control logic and is passed to the user.

If the frames passes all 3 compare steps and receive flow control is enabled, the pause parameter in the frame is used to inhibit transmitter operation for the time defined in the IEEE Std 802.3-2002 specification, a Receive Reject interrupt will be activated (see bit 28 in Table 10), and the frame will not be passed up to software.

If the transmitter is paused and a second pause frame is received, the current pause value of the transmitter is replaced with the new pause value received in the new pause frame including a possible value of 0x0.

## Statistics Vectors

### Transmit Statistics Vector

The transmitter provides 32 bits of statistics for each frame transmitted as well as a signal which can be used to count the total number of bytes transmitted. The 32-bit value is driven out one bit at a time following the transmission of each frame (shown in Figure 53) for the Hard TEMAC core. Logic can be used to de-multiplex the transmit statistics. The Soft TEMAC core provides statistics information by means of a 32-bit vector for one clock cycle as shown in Figure 54.

Table 54 shows the bit definition of the transmit statistics.

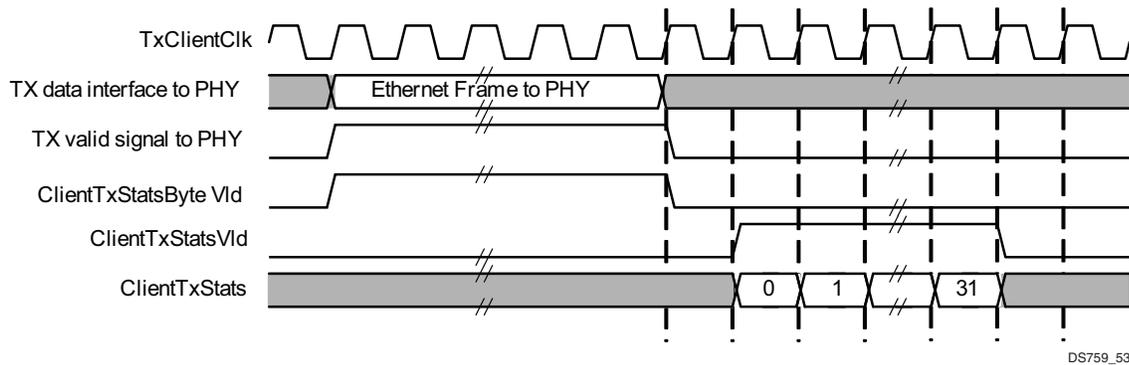


Figure 53: Hard TEMAC Transmit Statistics Waveforms

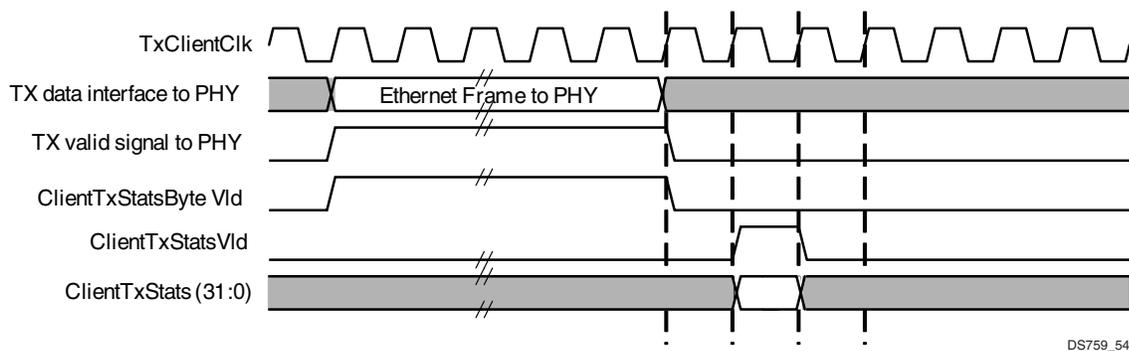


Figure 54: Soft TEMAC Transmit Statistics Waveforms

Table 54: Transmit Statistics Bit Definitions

ClientTxStats	Name	Description
31	PAUSE_FRAME_TRANSMITTED	Asserted if the previous frame was a pause frame initiated by writing to the TPF register.
30	BYTE_VALID	Hard TEMAC: This bit is reserved in the Hard TEMAC configuration. The value returned is undefined.  Soft TEMAC: Asserted if a MAC frame byte (Destination Address to FCS inclusive) is in the process of being transmitted. This is valid on every clock cycle. Do not use this as an enable signal to indicate that data is present on the transmit data pins going to the PHY.
29	Reserved (driven to zero)	Returns 0.
28 - 25 <sup>(1)</sup>	TX_ATTEMPTS(3:0)	Full Duplex: Returns 0s Half Duplex: The number of attempts that have been made to transmit the previous frame. This is a 4-bit number: 0 should be interpreted as 1 attempt; 1 as 2 attempts, up until 15 as 16 attempts. Only full-duplex is supported.
24 <sup>(1)</sup>	Reserved (driven to zero)	Returns 0.
23 <sup>(1)</sup>	EXCESSIVE_COLLISION	Full Duplex: Returns 0s Half Duplex: Asserted if a collision has been detected on each of the last 16 attempts to transmit the previous frame. Only full-duplex is supported.
22 <sup>(1)</sup>	LATE_COLLISION	Full Duplex: Returns 0s Half Duplex: Asserted if a late collision occurred during frame transmission. Only full-duplex is supported.
21 <sup>(1)</sup>	EXCESSIVE_DEFERRAL	Full Duplex: Returns 0s Half Duplex: Asserted if the previous frame was deferred for an excessive amount of time as defined by the constant "maxDeferTime" in <i>IEEE 802.3-2005</i> . Only full-duplex is supported.
20 <sup>(1)</sup>	TX_DEFERRED	Full Duplex: Returns 0s Half Duplex: Asserted if transmission of the frame was deferred. Only full-duplex is supported.
19	VLAN_FRAME	Asserted if the previous frame contains a VLAN identifier in the Length/Type field when transmitter VLAN operation is enabled
18 - 5	FRAME_LENGTH_COUNT	The length of the previous frame in number of bytes. The count sticks at 16838 for jumbo frames larger than this value.
4	CONTROL_FRAME	Asserted if the previous frame has the special Control type code 0x8808 in the Length/Type field
3	UNDERRUN_FRAME	Asserted if the previous frame contains an underrun error.
2	MULTICAST_FRAME	Asserted if the previous frame contains a multicast address in the destination address field.
1	BROADCAST_FRAME	Asserted if the previous frame contains a broadcast address in the destination address field.
0	SUCCESSFUL_FRAME	Asserted if the previous frame is transmitted without error.

**Notes:**

- Bits 28:20 are for Half-Duplex only. These bits will return Zero in Full Duplex mode.

## Receive Statistics Vector

The receiver provides 27 bits of statistics for each frame transmitted as well as a signal which can be used to count the total number of bytes transmitted. The 28-bit value is driven out six bits at a time following the transmission of each frame (shown in Figure 55) for the Hard TEMAC core. Logic can be used to de-multiplex the receive statistics. The Soft TEMAC core provides statistics information by means of a 28-bit vector for one clock cycle as shown in Figure 56.

Table 55 shows the bit definition of the receive statistics. Bits 28 to 20 will always be driven to zero because half-duplex is not supported.

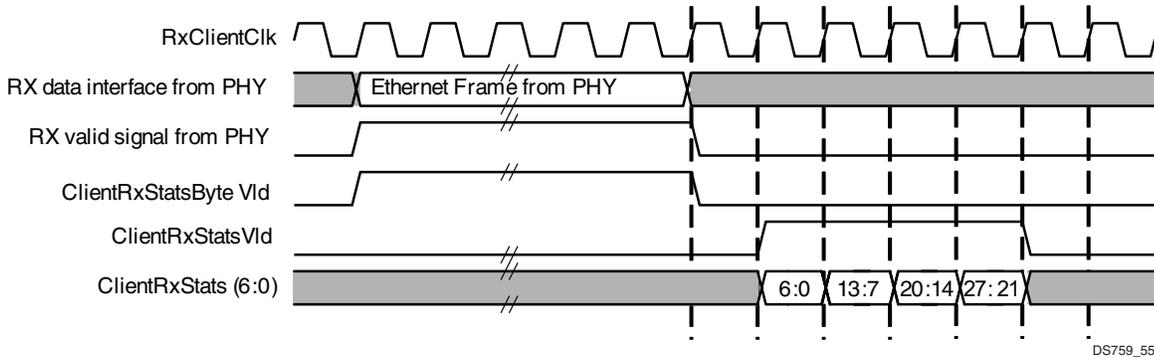


Figure 55: Hard TEMAC Receive Statistics Waveforms

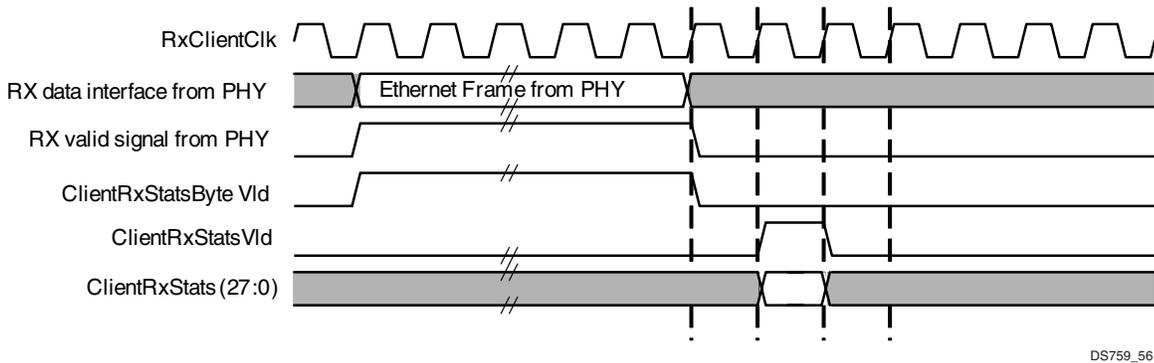


Figure 56: Soft TEMAC Receive Statistics Waveforms

Table 55: Receive Statistics Bit Definitions

ClientRxStats	Name	Description
27	ADDRESS_MATCH	When the Ethernet MAC is configured in Address Filtering mode, asserted if the previous frame successfully passed the address filter. When the Ethernet MAC is configured in promiscuous mode, this bit is always asserted.
26	ALIGNMENT_ERROR	Used in 10/100 MII mode. Asserted if the previous frame received has an incorrect FCS value and a misalignment occurs when the 4-bit MII data bus is converted to the 8-bit GMII data bus.
25	Length/Type Out Of Range	Asserted if the Length/Type field contains a length value that does not match the number of Ethernet MAC client data bytes received. Also asserted High if the Length/Type field indicates that the frame contains padding but the number of Ethernet MAC client data bytes received is not equal to 64 bytes (minimum frame size).  This bit is not defined when Length/Type field error-checks are disabled or when received frames are less than the legal minimum length.
24	BAD_OPCODE	Asserted if the previous frame is error free. Contains the special control frame identifier in the LT field, but contains an OPCODE unsupported by the Ethernet MAC (any OPCODE other than PAUSE).
23	FLOW_CONTROL_FRAME	Asserted if the previous frame is error-free. Contains the special control frame identifier in the LT field. Contains a destination address matching either the Ethernet MAC control multicast address or the configured source address of the Ethernet MAC. Contains the supported PAUSE OPCODE and is acted upon by the Ethernet MAC.
22	BYTE_VALID	Hard TEMAC: This bit is reserved in the Hard TEMAC configuration. The value returned is undefined.  Soft TEMAC: Asserted if a MAC frame byte (Destination Address to FCS inclusive) is in the process of being received. This is valid on every clock cycle. Do not use this as an enable signal to indicate that data is present on the receive data pins going to the receive client interface.
21	VLAN_FRAME	Asserted if the previous frame contains a VLAN identifier in the Length/Type field when the receiver VLAN operation is enabled.
20	OUT_OF_BOUNDS	Asserted if the previous frame exceeded the specified IEEE Std 802.3-2005 maximum legal length. This is only valid if jumbo frames are disabled.
19	CONTROL_FRAME	Asserted if the previous frame contains the special control frame identifier in the Length/Type field.
18 - 5	FRAME_LENGTH_COUNT	The length of the previous frame in number of bytes. The count sticks at 16383 for any jumbo frames larger than this value.
4	MULTICAST_FRAME	Asserted if the previous frame contains a multicast address in the destination field.
3	BROADCAST_FRAME	Asserted if the previous frame contains the broadcast address in the destination field.
2	FCS_ERROR	Asserted if the previous frame received has an incorrect FCS value or the Ethernet MAC detects error codes during frame reception.
1	BAD_FRAME <sup>(1)</sup>	Asserted if the previous frame received contains errors.
0	GOOD_FRAME <sup>(1)</sup>	Asserted if the previous frame received is error free.

**Notes:**

1. If the length/type field error checks are disabled, then a frame containing this type of error is marked as a GOOD\_FRAME, providing no additional errors were detected.

## Extended VLAN Support

### VLAN General Information

VLAN (or Virtual Local Area Network) frames are used to segregate Ethernet traffic within a larger physical LAN. VLAN frames are created by inserting a four byte VLAN TAG field in an Ethernet frame where the two byte Type/Length field would normally occur thus extending the overall frame by 4 bytes. The VLAN TAG field is further broken down into additional fields as shown in [Figure 57](#).

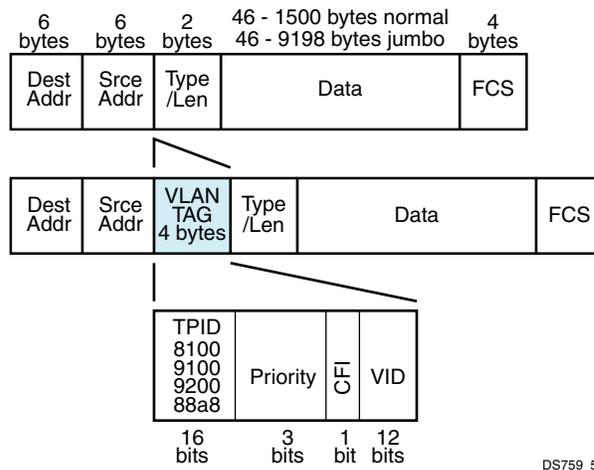


Figure 57: VLAN Frame Showing VLAN Tag Field

The TEMAC core provides basic VLAN support that can be enabled or disabled independently. This basic support recognizes VLAN frames that have a TPID value of 0x8100. When basic VLAN function is enabled, the TEMAC core will allow good VLAN frames with this TPID value to be processed for validation and address filtering rather than being dropped.

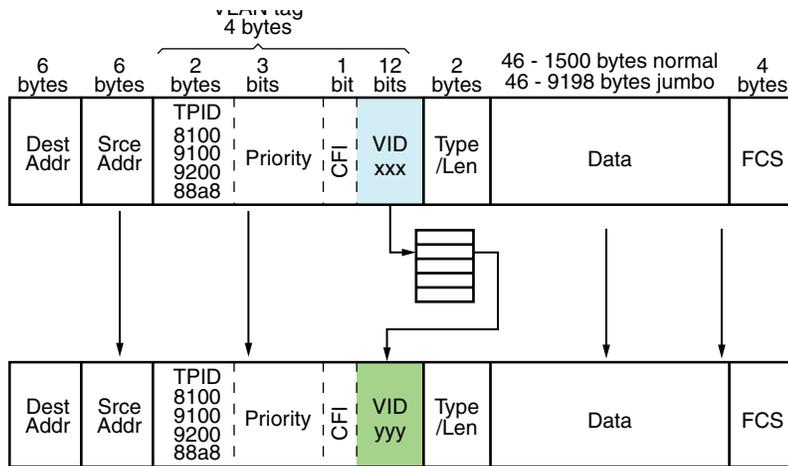
However, some applications require using a TPID value other than 0x8100 or will have multiple VLAN tags within one frame (referred to as double tagging, triple tagging, etc.). Additionally, some common operations are performed on VLAN frames that can be off-loaded from software to hardware to reduce processor utilization. Some of these tasks, translation, stripping, and auto tagging, are available when the extended VLAN support is included in the core at build-time by setting the appropriate parameters.

The extended VLAN functions are available individually and independently between the transmit and receive paths.

To use the extended VLAN functions, the circuitry must be included at build time by setting the appropriate parameters and also the functions must be enabled at run time by setting the New Functions enable bit (bit 20) of the [Reset and Address Filter Registers \(RAF\) - Offset 0x0000\\_0000](#).

## VLAN Translation

VLAN translation will enable the AXI Ethernet core to replace the VLAN ID (VID) value of the VLAN Tag field of a VLAN frame with a new VID as it passes through the AXI Ethernet core in either the transmit or receive direction.



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Figure 58: VLAN VID Translation

The TEMAC core will not recognize transmitting or receiving VLAN frames with a TPID other than 0x8100 when VLAN mode is enabled. If VLAN mode is disabled, then the maximum length of a normal frame will not be extended from 1518 to 1522 bytes. Additionally, multiple tagging is also not supported because of the even larger frame sizes.

To support multiple VLAN tagging and the use of TPID values other than 0x8100 in the outer tag, jumbo frame mode must be used with basic VLAN mode disabled. Using this setting will eliminate automatic invalidating (by the TEMAC core) of any frames that normally would be too large for *normal* frame sizes. The user must enable jumbo frame mode and disable VLAN mode when needed for extended VLAN mode.

### Transmit Path

When transmitting frames, the outgoing frame is detected as a VLAN frame by recognizing a VLAN Tag Protocol Identifier value (TPID) in the Type/Length field by comparing it against user defined values in the [VLAN TPID Word 0 Register \(TPID0\) - Offset 0x0000\\_0028](#) and [VLAN TPID Word 1 Register \(TPID1\) - Offset 0x0000\\_002C](#). Note that the TPID values are shared between the receive and transmit paths.

Once a VLAN frame is identified, the 12-bit Unique VLAN Identifier (VID) is used to access The [TEMAC Receive Configuration Word 0 \(RCW0\) Registers - Offset 0x0000\\_0400](#) to supply a replacement VID value which is substituted into the outgoing frame.

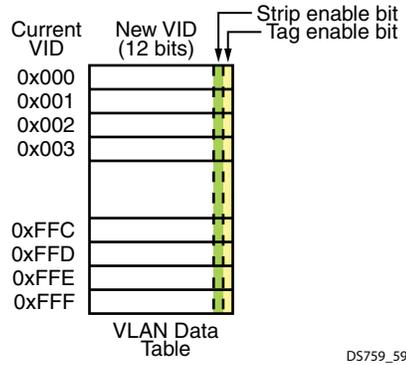


Figure 59: VLAN Data Table

Using transmit In-Band FCS mode of the TEMAC core is not allowed when using VLAN translation because the user provided FCS field value would not be correct for the new VID field.

For double, triple, etc. tagged VLAN frames, only the outer VID will be translated.

The following TPID values are commonly used to flag VLAN frames: 0x8100, 0x9100, 0x9200, and 0x88a8 however, the TPID values used to identify VLAN frames are programmable via the TPID registers.

Transmit and receive VLAN translation can be enabled separately with their respective parameters.

For VID values that do not need translated, the VLAN data table location associated with their value must be initialized to that same value.

### Receive Path

The receive operates similarly to the transmit side. The frame first passes through address filtering and validation processing before being checked for a VLAN TPID.

Receive FCS stripping in the TEMAC core is required when using VLAN translation because the FCS field that arrives with the frame will no longer be valid with the new TPID value. Please note that although receive stripping is enabled, any padding if present will not be stripped due to the TYPE / LENGTH field of the receive frame containing a VLAN tag rather than a length value.

### VLAN Tagging and Double Tagging (Stacking)

VLAN tagging allows the TEMAC to insert a pre-defined VLAN tag in select Ethernet frames as they pass through the core in either the transmit or receive direction.

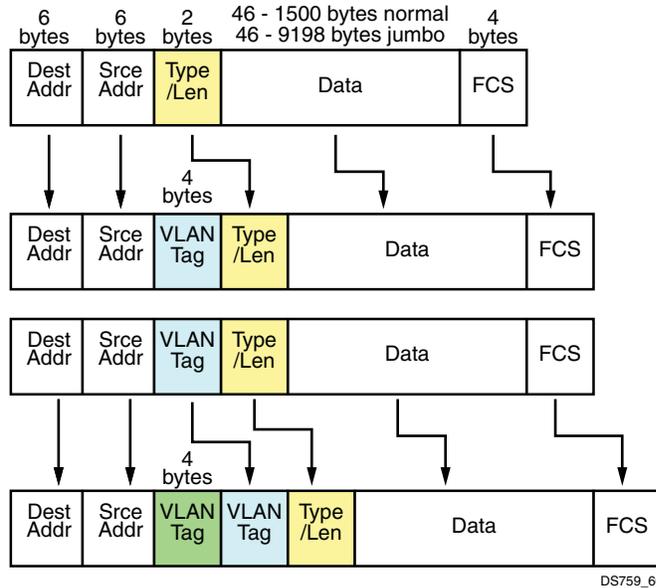


Figure 60: VLAN Tagging

**General**

One VLAN tag will be added depending on mode of operation:

- Non-VLAN frames will get one VLAN tag added to become single VLAN tagged frames.
- VLAN tagged frames will receive another VLAN tag and no checking will be performed to see how many VLAN tags the frame already has (if there are already 3 tags it will now have 4).

Therefore, in cases that require adding a VLAN tag, one VLAN tag will be added to the existing frame.

The TEMAC core’s basic VLAN mode extends the maximum normal frame size validation by 4 bytes. This mode does not extend to multiple VLAN tagging. Multiple VLAN frames that exceed 1522 bytes would be discarded as being too long. As mentioned previously, this requires the use of jumbo frame mode which will eliminate the automatic invalidation of frames that normally would be too large for normal frame sizes.

When VLAN tagging is enabled at build time with the appropriate parameter, a field in the [Reset and Address Filter Registers \(RAF\) - Offset 0x0000\\_0000](#) will be used to select one of four VLAN tagging modes and the [Transmit VLAN Tag Register \(TTAG\) - Offset 0x0000\\_0018](#) and [Receive VLAN Tag Register \(RTAG\) - Offset 0x0000\\_001C](#) will be used to hold the VLAN tag value which will be inserted.

The four VLAN tagging modes which are selectable at run time are:

1. Do not add tags to any frames
2. Add one tag to all frames
3. Add one tag only to frames that are already VLAN tagged
4. Add one tag only to select frames that are already VLAN tagged based on VID value

The fourth mode requires a method for specifying which tagged frames should receive an additional VLAN tag. The [TEMAC Receive Configuration Word 0 \(RCW0\) Registers - Offset 0x0000\\_0400](#) and [Receive VLAN Data Table - Offset 0x0000\\_8000-0x0000\\_BFFF, page 53](#) are used for this purpose. A 1 in the tag enable field for a TPID value indicates that frame should receive an additional tag.

Again, transmit In-Band FCS mode is not allowed and receive FCS stripping is required when using VLAN tagging because FCS field value would not be correct for the frame with the additional VLAN tag. Although receive stripping is enabled, any padding if present will not be stripped because the TYPE / LENGTH field of the receive frame contains a VLAN tag rather than a length value. However, the length field is still present.

## VLAN Stripping

VLAN stripping allows the TEMAC to remove a VLAN tag in select Ethernet frames as they pass through the AXI Ethernet core in either the transmit or receive direction.

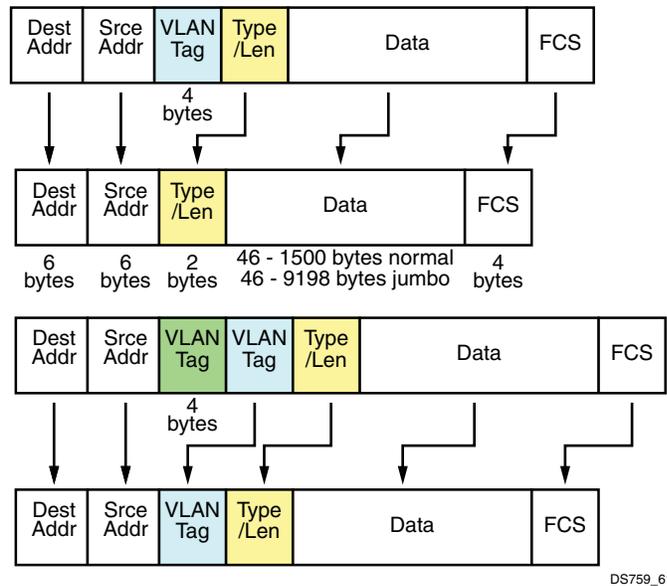


Figure 61: VLAN Stripping

### General

One VLAN tag will be removed:

- Non-VLAN frames will not be changed
- VLAN tagged frames will have the outer VLAN tag removed and we won't check to see how many VLAN tags it already has (if there are 4 tags we will make it 3).

When VLAN stripping is enabled at build time with the appropriate parameter, a field in the [Reset and Address Filter Registers \(RAF\) - Offset 0x0000\\_0000](#) will be used to select one of three VLAN stripping modes.

1. Do not strip tags from any frames
2. Strip one tag from all VLAN tagged frames
3. Strip one tag only from select VLAN tagged frames based on VID value

The third mode requires a method for specifying which tagged frames should be stripped. The [TEMAC Receive Configuration Word 0 \(RCW0\) Registers - Offset 0x0000\\_0400](#) and [Receive VLAN Data Table - Offset 0x0000\\_8000-0x0000\\_BFFF, page 53](#) are used for this purpose. A 1 in the strip enable field for a TPID value indicates that frame should have its VLAN tag stripped.

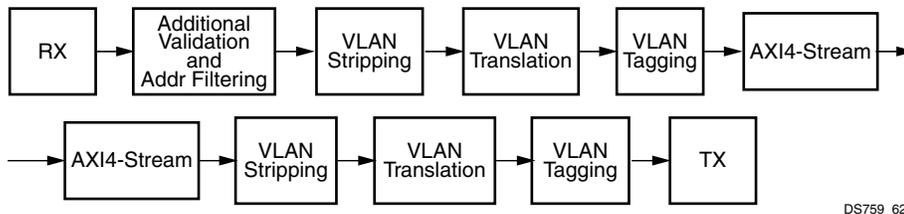
Again, transmit In-Band FCS mode is not allowed and receive FCS stripping is required when using VLAN stripping because FCS field value would not be correct for the frame with the VLAN tag removed. Please note that

although receive stripping is enabled, any padding if present will not be stripped due to the TYPE / LENGTH field of the receive frame containing a VLAN tag rather than a length value.

## Order of VLAN Functions when Combined

When multiple VLAN functions are combined, the order of processing for both transmit and receive is:

1. VLAN Stripping
2. VLAN Translation
3. VLAN Tagging



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Figure 62: Order of Extended VLAN Functions

## Ethernet Audio Video Bridging (AVB)

Ethernet AVB functionality is supported with AXI Ethernet. The parameter C\_AVB must be set to "1" to enable the core. Please refer to [UG492 LogiCORE IP Ethernet AVB Endpoint User Guide](#) for more information on AVB.

### AVB Frames AXI4-Stream Interface

The AVB AXI4-Stream interface is a limited interface in that it does not allow throttling from the external connections. As a result, some of the standard AXI4-Stream signals are missing from the port list as well as the addition of the TUSER signals. Both transmit and receive busses are 8 bits wide which eliminates the need of the write strobe signal bus. For both busses, the AXI Ethernet provides the AXI4-Stream clocks and clock enables which are derived from the internal Ethernet clocks.

The AVB AXI4-Stream interface will be connected to external logic that currently is not provided by Xilinx, although several third party partners have created this logic, have tested it with the Core Generator system core, and have integrated it into AVB systems. This external logic takes time sensitive audio or video information and splits it into Ethernet frames using a protocol encoding that is similar to TCP/IP. This is all done in FPGA fabric logic.

Ethernet AVB frames are passed back and forth to the Ethernet via the AVB AXI4-Stream interfaces. Internal to AXI Ethernet, the AVB frames and the legacy frames are multiplexed and demultiplexed based on a prioritization and time slotting method. The AVB function in AXI Ethernet responsible for helping to choose the most accurate AVB system clock in the Ethernet network and synchronizes to the clock so all AVB nodes are synchronized.

### Transmit Interface

AXI Ethernet provides the signal AXI\_STR\_AVBTX\_ACLK which is derived from the TEMAC transmit client interface clock. This clock operates at 125 MHz when operating at 1 Gbps and is 25 MHz or 2.5 MHz when operating at 100 Mbps or 10 Mbps respectively. During a transfer, AXI Ethernet will use the TEMAC transmit client interface clock enable to toggle AXI\_STR\_AVBTX\_TREADY. The clock enable is HIGH for every clock cycle when operating at 1 Gbps and toggles every other clock cycle for 100 Mbps and 10 Mbps. When AXI Ethernet is ready to transmit an AVB frame, it will drive the AXI\_STR\_AVBTX\_TREADY signal HIGH. When the external logic is ready

to transmit a frame, it will drive the AXI\_STR\_AVBTX\_TVALID signal HIGH and provide the first byte of data on the AXI\_STR\_AVBTX\_TDATA bus. At this point the external logic must provide a new byte of data on every clock cycle that the AXI\_STR\_AVBTX\_TREADY signal is HIGH while TVALID is active until the end of the frame is reached. The external logic can not throttle the AVB transmit interface. AXI Ethernet will accept the first byte and will then drive AXI\_STR\_AVBTX\_TREADY LOW until the TEMAC has started the transmit, then it will drive it back to HIGH and continue to use it as a clock enable for the remainder of that frame.

On the last byte of the frame, the external logic will drive the AXI\_STR\_AVBTX\_TLAST signal HIGH for one clock cycle with AXI\_STR\_AVBTX\_TREADY. If it does not have any additional frames to transmit, it will remove the TVALID signal when it takes the TLAST signal LOW. However, if another frame is ready, the external logic will leave the TVALID signal HIGH.

The TUSER signal is intended to allow the external logic to indicate that the current frame in progress has an error such as an underflow and the frame should be aborted. It is intended that this be connected to the underflow input of the AVB to force the current frame to be aborted, but the current AVB core does not provide an AVB underflow input. Figure 63 below shows a transmit AXI4-Stream waveform for 1 Gbps mode where there are additional AVB frames available after the completion of the current frame. Figure 64 shows the TX client interface operating at 100Mbps.

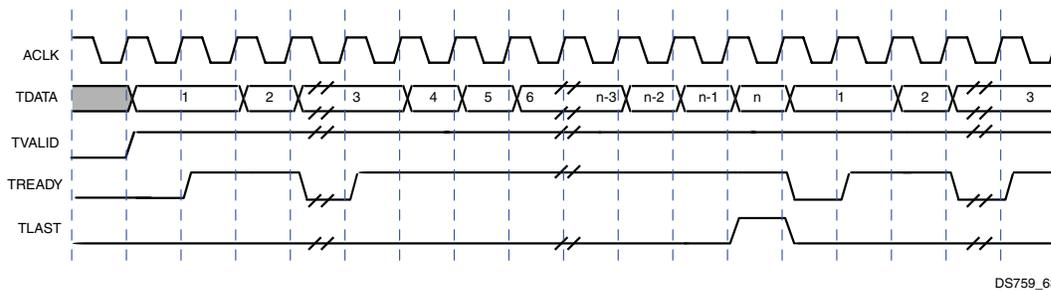


Figure 63: 1000Mbps Transmit AVB AXI4-Stream (back-to-back)

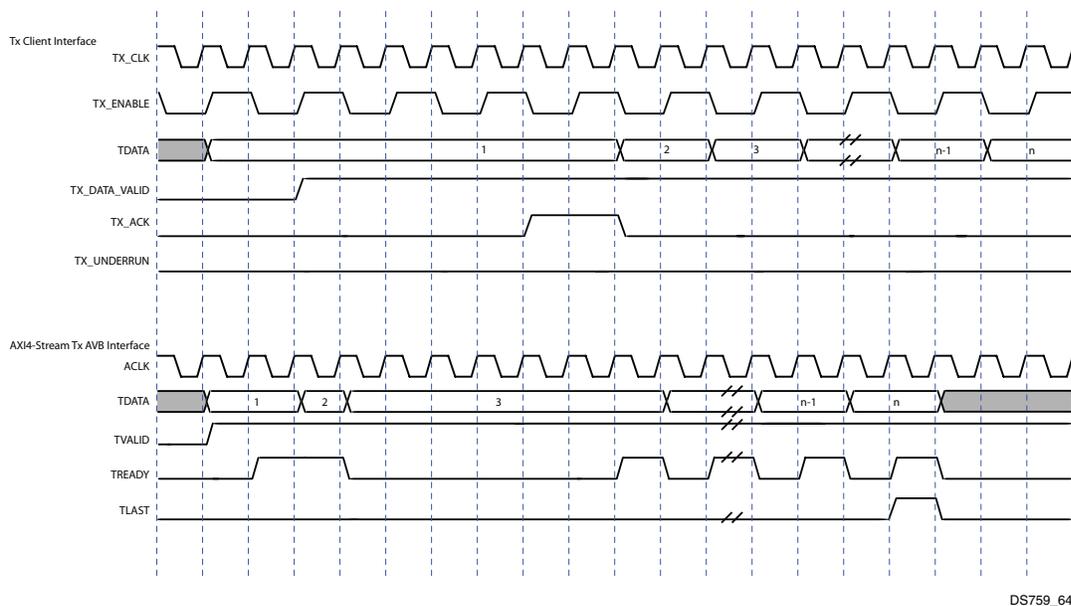


Figure 64: 100Mbps Transmit AVB AXI4-Stream

## Receive Interface

The receive interface provides an AXI4-Stream clock and which is derived from the TEMAC receive client interface and will use the AXI\_STR\_AVBRX\_TVALID signal as a clock enable derived from the receive client interface clock enable. These signals behave similarly to the transmit interface when the Ethernet bus speed changes.

When AXI Ethernet has received an AVB frame to transfer over the AXI4-Stream to the external logic, it will drive the AXI\_STR\_AVBRX\_TVALID signal HIGH and will provide a new AXI\_STR\_AVBRX\_TDATA byte value on each clock cycle when AXI\_STR\_AVBRX\_TVALID signal is HIGH. The destination cannot throttle and must always be ready to receive a frame. After AXI Ethernet transfers the second to last byte, it will drive the AXI\_STR\_AVBRX\_TVALID signal LOW and wait until it gets a good or bad frame indication from the TEMAC before it finishes the frame. When it receives the good or bad frame indication, it will drive the AXI\_STR\_AVBRX\_TVALID signal HIGH again for one clock/AXI\_STR\_AVBRX\_TVALID cycle along with the last byte value. It will drive the AXI\_STR\_AVBRX\_TUSER signal HIGH if the frame is bad. If the frame is good, it will drive AXI\_STR\_AVBRX\_TUSER signal LOW while driving the AXI\_STR\_AVBRX\_TLAST signal HIGH.

All receive frames, good or bad, that meet the address filtering rules, will appear on the receive AXI\_STREAM interface with the only indication of good vs. bad being the value of AXI\_STR\_AVBRX\_TUSER during AXI\_STR\_AVBRX\_TLAST.

Figure 65 the receive waveforms for AVB interface operating at 100Mbps.

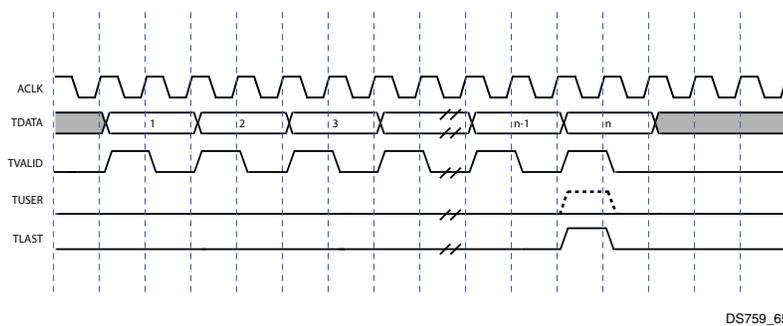


Figure 65: 100Mbps Receive AVB AXI4-Stream

## Virtex-6 Hard TEMAC Implementations

### Introduction to Physical Interfaces

The Hard TEMAC silicon component in the Virtex-6 FPGA devices is independent of, and can connect to, any type of physical layer device. The AXI Ethernet provides additional circuitry around the Hard TEMAC silicon component to allow easy use of several common physical layer device interfaces.

The following are two types of physical layer interfaces:

- **BASE-T** provide a link between the AXI Ethernet and copper mediums. This functionality can be provided in a AXI Ethernet system by connecting to external BASE\_T PHY devices which are readily available. This connection can be made using the MII, GMII/MII, RGMII, and SGMII interfaces.
  - Virtex-6 devices support GMII/MII at 2.5 V only.
- **BASE-X** provide a link between AXI Ethernet and (usually) fiber optic mediums. AXI Ethernet system can provide this function at 1000 Mb/S (1000BASE-X) by using a GTX or GTP transceiver.

## Media Independent Interface (MII)

The Media Independent Interface (MII), defined in IEEE 802.3 clause 22, is a parallel interface that connects at 10-Mb/S and/or 100-Mb/S to external PHY devices.

The MII design uses clock enables. Please refer to [UG368](#) Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when AXI Ethernet parameter `C_INCLUDE_IO = "1"`. When the parameter `C_INCLUDE_IO = "0"`, any BUFGs, IBUFGs, IBUFS, and OBUFS are not used.

### ***Virtex 6 Hard TEMAC MII Constraints***

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

## Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (GMII), defined in IEEE 802.3 clause 35, is an extension of the MII used to connect at 1-Gb/S to the PHY devices.

MII can be considered a subset of GMII, and as a result, GMII/MII together can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

When the GMII interface is selected with parameters for AXI Ethernet, a GMII/MII interface is used which is capable of all three Ethernet speeds.

The GMII design uses clock enables. Please refer to [UG368](#) Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when AXI Ethernet parameter `C_INCLUDE_IO = "1"`. One modification has been performed to the receive clock when `C_INCLUDE_IO = 1`. The AXI Ethernet design has been modified such that `GMII_RX_CLK` is not connected to an `IODELAY` element. It connects directly to the `BUFIO` and `BUFR`. When the parameter `C_INCLUDE_IO = "0"`, any `IBUFGs`, `IBUFS`, `OBUFS`, `BUFGMUXs`, `BUFIOs`, `BUFRs`, and `IODELAYs` are not used.

### ***Virtex 6 Hard TEMAC GMII Constraints***

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

## Reduced Gigabit Media Independent Interface (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the GMII/MII. RGMII achieves a 50% reduction in the pin count compared with GMII, and is therefore favored over GMII/MII by PCB designers. This is achieved with the use of double-data-rate (DDR) flip-flops.

RGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

For more information on RGMII, refer to the *Hewlett-Packard RGMII Specification, version 1.3 and 2.0*.

The RGMII design uses clock enables. Please refer to [UG368](#) Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when AXI Ethernet parameter `C_INCLUDE_IO = "1"` for both RGMII Version 2.0 and RGMII Version 1.3. When the parameter `C_INCLUDE_IO = "0"`, the `BUFR`, `BUFIO` and `IODELAY` on the `RGMII_RXC` signal are not used.

### ***Virtex 6 Hard TEMAC RGMII Constraints***

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

## Serial Gigabit Media Independent Interface (SGMII)

The Serial-GMII (SGMII) is an alternative interface to the GMII/MII that converts the parallel interface of the GMII into a serial format. This radically reduces the I/O count and is therefore often favored by PCB designers. This is achieved by using a GTX transceiver.

SGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

The SGMII physical interface was defined by Cisco Systems, Inc. The data signals operate at a rate of 1.25 Gb/S. Differential pairs are used to provide signal integrity and minimize noise. The sideband clock signals defined in the specification are not implemented in AXI Ethernet. Instead, the GTX transceiver is used to transmit and receive the differential data at the required rate using clock data recovery. For more information on SGMII, refer to the *Serial GMII Specification v1.7*.

Please refer to [UG368](#) Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the AXI Ethernet parameter C\_INCLUDE\_IO = "1". When the parameter C\_INCLUDE\_IO = "0", MGTCLK\_P connects directly to the Serial Transceiver; therefore the IBUFDS is not used.

### Virtex 6 Hard TEMAC SGMII Constraints

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### SGMII Auto-Negotiation

The external SGMII capable PHY device performs auto negotiation with its link partner on the PHY Link (Ethernet bus) in resolving operational speed and duplex mode, then performs a secondary auto negotiation with the GTX transceiver across the SGMII Link. This transfers the results of the PHY with Link Partner auto negotiation across the SGMII to AXI Ethernet.

The results of the SGMII auto negotiation can be read from the SGMII Management Auto negotiation Link Partner Ability Base Register ([Table 62](#)). The duplex mode and speed of AXI Ethernet should then be set to match (see [TEMAC Receive Configuration Word 1 \(RCW1\) Registers - Offset 0x0000\\_0404](#), page 38, [TEMAC Transmit Configuration \(TC\) Registers - Offset 0x0000\\_0408](#), page 40, and [TEMAC Ethernet MAC Mode Configuration \(EMMC\) Registers - Offset 0x0000\\_0410](#), page 42).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

1. By polling the auto negotiation complete bit of SGMII Management Status Register (Register 1, bit 5 [Table 58](#)).
2. By using the auto negotiation complete interrupt (see [Interrupt Status Registers \(IS\) - Offset 0x0000\\_000C](#), page 22 and SGMII Management Auto Negotiation Interrupt Control Register [Table 67 on page 94](#).)

### Loopback

There are two possible loopback positions:

1. **Loopback in the Hard TEMAC silicon component.** When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the GTX transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the GTX transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
2. **Loopback in the GTX transceiver.** The GTX transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the GTX transceiver. However, this data is also transmitted out of the GTX transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the SGMII Management Control Register bit 14 (Table 57 on page 90) while the loopback position can be controlled by writing the SGMII Management Loopback Control Register bit 0 (Table 68 on page 95).

### Internal SGMII Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the SGMII PCS sublayer, including the status of both the SGMII Link and the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the SGMII auto negotiation function which occurs between AXI Ethernet and the external PHY device (typically a tri-speed BASE-T PHY).

These registers are accessed via the MII Management interface (Using the Address Filters, page 56). These registers are only valid when using the SGMII PHY interface.

Table 56: Internal SGMII Management Registers

Register Name	Register Address (REGAD)
SGMII Control Register (Register 0)	0
SGMII Status Register (Register 1)	1
SGMII PHY Identifier (Register 2 and 3)	2,3
SGMII Auto Negotiation Advertisement Register (Register 4)	4
SGMII Auto Negotiation Link Partner Ability Base Register (Register 5)	5
SGMII Auto Negotiation Expansion Register (Register 6)	6
SGMII Auto Negotiation Next Page Transmit Register (Register 7)	7
SGMII Auto Negotiation Next Page Receive Register (Register 8)	8
SGMII Extended Status Register (Register 15)	15
SGMII Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
SGMII Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 57 shows the Hard TEMAC Internal SGMII PCS Management Control Register bit definitions.

Table 57: SGMII Management Control Register (Register 0) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the GTX transceiver is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down

Table 57: SGMII Management Control Register (Register 0) Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to signal full duplex mode.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to disable COL test.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 58 shows the Hard TEMAC Internal SGMII PCS Management Status Register bit definitions.

Table 58: SGMII Management Status Register (Register 1) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a 1 for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up

Table 58: SGMII Management Status Register (Register 1) Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 59 shows the first Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 59: SGMII Management PHY Identifier (Register 2) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 60 shows the second Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 60: SGMII Management PHY Identifier (Register 3) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 61 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Advertisement Register bit definitions.

Table 61: SGMII Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	All bits	Read	0x0001	SGMII defined value sent from the MAC to the PHY.

Table 62 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 62: SGMII Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	PHY Link Status	Read	1	This refers to the link status of the PHY with its Link Partner across the medium. 0 - Link Down 1 - Link Up
14	Acknowledge	Read	0	Used by Auto-negotiation function to indicate reception of a link partner's base or next page
13	Reserved	Returns 0	0	Always return zero.
12	Duplex Mode	Read	0	1 = Full Duplex 0 = Half Duplex

**Table 62: SGMII Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions (Cont'd)**

Bit(s)	Name	Core Access	Reset Value	Description
10-11	Speed	Read	00	00 - Reserved 01 - 1000 Mbps 10 - 100 Mbps 11 - 10 Mbps
1-9	Reserved	Returns 0s	000000000	Always return zeros.
0	Reserved	Returns 1	1	Always return one.

Table 63 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Expansion Register bit definitions.

**Table 63: SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 64 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Transmit Register bit definitions.

**Table 64: SGMII Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 - 10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 65 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Receive Register bit definitions.

Table 65: SGMII Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 - 10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 66 shows the Hard TEMAC Internal SGMII PCS Management Extended Status Register bit definitions.

Table 66: SGMII Management Extended Status Register (Register 15) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 67 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Interrupt Control Register bit definitions.

Table 67: SGMII Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 68 shows the Hard TEMAC Internal SGMII PCS Management Loopback Control Register bit definitions.

Table 68: SGMII Management Loopback Control Register (Register 17) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the GTX transceiver 1 - loopback (when enabled) occurs in the GTX transceiver

## 1000BASE-X PCS/PMA

Please refer to [UG368](#) Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when AXI Ethernet parameter C\_INCLUDE\_IO = "1". When the parameter C\_INCLUDE\_IO = "0", MGTCLK\_P connects directly to the Serial Transceiver; hence the IBUFDS is not used.

### PCS/PMA

The Physical Coding Sublayer (PCS) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and 37 and performs the following:

- Encoding (and decoding) of GMII data octets to form a sequence of ordered sets
- 8B/10B encoding (and decoding) of the sequence ordered sets
- 1000BASE-X Auto-Negotiation for information exchange with the link partner

The Physical Medium Attachment (PMA) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and performs the following:

- Serialization (and de serialization) of code-groups for transmission (and reception) on the underlying serial PMD
- recovery of clock from the 8B/10B coded data supplied by the PMD

1000BASE-X PCS/PMA functionality is provided by connecting the Hard TEMAC silicon component to a GTX transceiver.

### PMD

The Physical Medium Dependent (PMD) sublayer is defined in IEEE 802.3 clause 38 for 1000BASE-LX and 1000BASE-SX (long and short wave laser). This type of PMD is provided by the external GBIC or SFP optical transceiver which should be connected directly to the ports of the GTX transceiver.

### Virtex 6 Hard TEMAC 1000BASE-X Constraints

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### 1000BASE-X Auto-Negotiation

1000BASE-X auto negotiation is described in IEEE Std 802.3, clause 37. This function allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (the link partner on Ethernet), and detect corresponding operational modes advertised by the link partner.

The results of the auto negotiation can be read from the 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Table 75). The duplex mode and speed of AXI Ethernet should then be set to match (see TEMAC Receive Configuration Word 1 (RCW1) Registers - Offset 0x0000\_0404, page 38, TEMAC Transmit Configuration (TC) Registers - Offset 0x0000\_0408, page 40, and TEMAC Ethernet MAC Mode Configuration (EMMC) Registers - Offset 0x0000\_0410, page 42).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

- By polling the auto negotiation complete bit of 1000BASE-X Management Status Register (Register 1, bit 5 Table 71).

By using the auto negotiation complete interrupt (Interrupt Status Registers (IS) - Offset 0x0000\_000C, page 22 and 1000BASE-X Management Auto Negotiation Interrupt Control Register Table 80 on page 102.)

### Loopback

There are two possible loopback positions:

1. **Loopback in the Hard TEMAC silicon component.** When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the GTX transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the GTX transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
2. **Loopback in the GTX transceiver.** The GTX transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the GTX transceiver. However, this data is also transmitted out of the GTX transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the 1000BASE-X Management Control Register bit 14 (Table 70 on page 97) while the loopback position can be controlled by writing the 1000BASE-X Management Loopback Control Register bit 0 (Table 81 on page 102).

### Internal 1000BASE-X PCS/PMA Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the 1000BASE-X PCS/PMA sublayer, including the status of the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the 1000BASE-X auto negotiation function which occurs between AXI Ethernet and its link partner, the Ethernet device connected at the far end of the PHY Link.

These registers are accessed via the MII Management interface (Using the Address Filters, page 56). These registers are only valid when using the 1000BASE-X PHY interface.

When using 1000BASE-X, AXI Ethernet is typically connected to an external optical transceiver device such as a GBIC or SFP transceiver.

Table 69: Internal 1000BASE-X PCS/PMA Management Registers

Register Name	Register Address (REGAD)
Control Register (Register 0)	0
Status Register (Register 1)	1
PHY Identifier (Register 2 and 3)	2,3
Auto Negotiation Advertisement Register (Register 4)	4

Table 69: Internal 1000BASE-X PCS/PMA Management Registers (Cont'd)

Register Name	Register Address (REGAD)
Auto Negotiation Link Partner Ability Base Register (Register 5)	5
Auto Negotiation Expansion Register (Register 6)	6
Auto Negotiation Next Page Transmit Register (Register 7)	7
Auto Negotiation Next Page Receive Register (Register 8)	8
Extended Status Register (Register 15)	15
Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 70 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Control Register bit definitions.

Table 70: 1000BASE-X Management Control Register (Register 0) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the GTX transceiver is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to signal full duplex mode.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to disable COL test.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 71 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Status Register bit definitions.

Table 71: 1000BASE-X Management Status Register (Register 1) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a 1 for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 72 shows the first Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 72: 1000BASE-X Management PHY Identifier (Register 2) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 73 shows the second Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 73: 1000BASE-X Management PHY Identifier (Register 3) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 74 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Advertisement Register bit definitions.

Table 74: 1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - next page functionality is not advertised 1 - next page functionality is advertised
14	Reserved	Returns 0s	0	Always return zeros.
12 - 13	Remote Fault	Read/Write self clearing after auto negotiation	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read/write	0x3	00 - No pause 01 - Symmetric pause 10 - Asymmetric pause towards link partner 11 - both symmetric pause and asymmetric pause towards link partner
6	Half Duplex	Returns 0	0	Always return zeros because half duplex is not supported.
5	Full Duplex	Read/Write	1	0 - full duplex mode is not advertised 1 - full duplex mode is advertised
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 75 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 75: 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - next page functionality is not supported 1 - next page functionality is supported
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.

**Table 75: 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions (Cont'd)**

Bit(s)	Name	Core Access	Reset Value	Description
12 - 13	Remote Fault	Read/	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read	0x	00 - no pause 01 - asymmetric pause supported 10 - symmetric pause supported 11 - both symmetric pause and asymmetric pause supported
6	Half Duplex	Read	0	0 - half duplex mode is not supported 1 - half duplex mode is supported
5	Full Duplex	Read/	0	0 - full duplex mode is not supported 1 - full duplex mode is supported
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 76 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Expansion Register bit definitions.

**Table 76: 1000BASE-X Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 77 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Transmit Register bit definitions.

**Table 77: 1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.

**Table 77: 1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions (Cont'd)**

Bit(s)	Name	Core Access	Reset Value	Description
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 78 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Receive Register bit definitions.

**Table 78: 1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 79 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Extended Status Register bit definitions.

**Table 79: 1000BASE-X Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 80 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Interrupt Control Register bit definitions.

**Table 80: 1000BASE-X Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 81 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Loopback Control Register bit definitions.

**Table 81: 1000BASE-X Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the GTX transceiver 1 - loopback (when enabled) occurs in the GTX transceiver

## Soft TEMAC Implementations

### Introduction to Physical Interfaces

The soft TEMAC implementation is independent of, and can connect to, any type of physical layer device. AXI Ethernet provides additional circuitry around the soft TEMAC to allow easy use of two of the most common physical layer device interfaces.

Because the soft TEMAC uses more logic and clock resources than a Hard TEMAC implementation, it is less likely that multiple channels will be used in one device.

Please refer to [Table 1](#) and [Table 2](#) for supported voltages with the different device families.

### Media Independent Interface (MII)

The Media Independent Interface (MII), defined in IEEE 802.3 clause 22, is a parallel interface that connects at 10-Mb/S and/or 100-Mb/S to external PHY devices.

Please refer to [UG138](#) LogiCORE IP Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme.

### **Soft TEMAC MII Constraints**

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### **Gigabit Media Independent Interface (GMII)**

The Gigabit Media Independent Interface (GMII), defined in IEEE 802.3 clause 35, is an extension of the MII used to connect at 1-Gb/S to the PHY devices.

MII can be considered a subset of GMII, and as a result, GMII/MII together can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

When the GMII interface is selected with parameters for AXI Ethernet, a GMII/MII interface is used which is capable of all three Ethernet speeds.

Please refer to [UG138](#) LogicCORE IP Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme.

### **Soft TEMAC GMII Constraints**

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### **Reduced Gigabit Media Independent Interface (RGMII)**

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the GMII/MII. RGMII achieves a 50% reduction in the pin count compared with GMII, and is therefore favored over GMII/MII by PCB designers. This is achieved with the use of double-data-rate (DDR) flip-flops.

RGMII can carry Ethernet traffic at 10 Mbps, 100 Mbps, and 1 Gbps.

For more information on RGMII, refer to the *Hewlett-Packard RGMII Specification, version 1.3 and 2.0*.

The RGMII design uses clock enables. Please refer to [UG138](#) LogicCORE IP Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when AXI Ethernet parameter C\_INCLUDE\_IO = "1". When the parameter C\_INCLUDE\_IO = "0", all of the logic in the RGMII PHY module (rgmii\_if) has been removed with the exception of the receiver clock.

### **Spartan 6 Soft TEMAC RGMII Constraints**

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### **Serial Gigabit Media Independent Interface (SGMII)**

The Serial-GMII (SGMII) is an alternative interface to the GMII/MII that converts the parallel interface of the GMII into a serial format. This radically reduces the I/O count and is therefore often favored by PCB designers. This is achieved by using a GTP transceiver.

SGMII can carry Ethernet traffic at 10 Mbps, 100 Mbps, and 1 Gbps.

The SGMII physical interface was defined by Cisco Systems, Inc. The data signals operate at a rate of 1.25 Gb/S. Differential pairs are used to provide signal integrity and minimize noise. The sideband clock signals defined in the specification are not implemented in AXI Ethernet. Instead, the GTP transceiver is used to transmit and receive the differential data at the required rate using clock data recovery. For more information on SGMII, refer to the *Serial GMII Specification v1.7*.

Please refer to [UG155](#) LogicCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII for an equivalent diagram of the clock management scheme when AXI Ethernet parameter C\_INCLUDE\_IO = "1" for Virtex-6 and Spartan-6 devices. When the parameter C\_INCLUDE\_IO = "0", MGTCLK\_P connects directly to the Serial Transceiver; hence the IBUFDS is not used.

### **Spartan 6 Soft TEMAC SGMII Constraints**

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### **SGMII Auto-Negotiation**

The external SGMII capable PHY device performs auto negotiation with its link partner on the PHY Link (Ethernet bus) resolving operational speed and duplex mode and then in turn performs a secondary auto negotiation with the GTP transceiver across the SGMII Link. This transfers the results of the PHY with Link Partner auto negotiation across the SGMII to the AXI Ethernet.

The results of the SGMII auto negotiation can be read from the SGMII Management Auto negotiation Link Partner Ability Base Register ([Table 88 on page 107](#)). The duplex mode and speed of AXI Ethernet should then be set to match (see [TEMAC Receive Configuration Word 1 \(RCW1\) Registers - Offset 0x0000\\_0404, page 38](#), [TEMAC Transmit Configuration \(TC\) Registers - Offset 0x0000\\_0408, page 40](#), and [TEMAC Ethernet MAC Mode Configuration \(EMMC\) Registers - Offset 0x0000\\_0410, page 42](#)).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

By polling the auto negotiation complete bit of SGMII Management Status Register (Register 1, bit 5 [Table 58 on page 91](#)).

By using the auto negotiation complete interrupt (<RD Red>see "[Interrupt Status Registers \(IS\) - Offset 0x0000\\_000C" on page 22](#) and SGMII Management Auto Negotiation Interrupt Control Register [Table 93 on page 109](#).)

### **Loopback**

Unlike the hard TEMAC, there is only one possible loopback position:

- **Loopback in the Soft TEMAC silicon component.** When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the GTP transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the GTP transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.

Loopback can be enabled or disabled by writing to the SGMII Management Control Register bit 14 ([Table 83 on page 105](#)).

### **Internal SGMII Management Registers**

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the SGMII PCS sublayer, including the status of both the SGMII Link and the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the SGMII auto negotiation function which occurs between AXI Ethernet and the external PHY device (typically a tri-speed BASE-T PHY).

These registers are accessed via the MII Management interface ([Using the Address Filters, page 56](#)). These registers are only valid when using the SGMII PHY interface.

**Table 82: Internal SGMII Management Registers**

Register Name	Register Address (REGAD)
SGMII Control Register (Register 0)	0
SGMII Status Register (Register 1)	1
SGMII PHY Identifier (Register 2 and 3)	2,3
SGMII Auto Negotiation Advertisement Register (Register 4)	4
SGMII Auto Negotiation Link Partner Ability Base Register (Register 5)	5
SGMII Auto Negotiation Expansion Register (Register 6)	6
SGMII Auto Negotiation Next Page Transmit Register (Register 7)	7
SGMII Auto Negotiation Next Page Receive Register (Register 8)	8
SGMII Extended Status Register (Register 15)	15
SGMII Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16

[Table 83](#) shows the Hard TEMAC Internal SGMII PCS Management Control Register bit definitions.

**Table 83: SGMII Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the GTX transceiver is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to signal full duplex mode.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to disable COL test.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 84 shows the Hard TEMAC Internal SGMII PCS Management Status Register bit definitions.

Table 84: SGMII Management Status Register (Register 1) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a 1 for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 85 shows the first Soft TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 85: SGMII Management PHY Identifier (Register 2) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 86 shows the second Soft TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 86: SGMII Management PHY Identifier (Register 3) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
4-9	MMN	Returns 0	000000	Manufacturer's Model Number. Always returns 0s.
0-3	Revision	Returns 0	0000	Revision Number. Always returns 0s.

Table 87 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Advertisement Register bit definitions.

Table 87: SGMII Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	All bits	Read	0x0001	SGMII defined value sent from the MAC to the PHY.

Table 88 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 88: SGMII Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	PHY Link Status	Read	1	This refers to the link status of the PHY with its Link Partner across the medium. 0 - Link Down 1 - Link Up
14	Acknowledge	Read	0	Used by Auto-negotiation function to indicate reception of a link partner's base or next page
13	Reserved	Returns 0	0	Always return zero.
12	Duplex Mode	Read	0	1 = Full Duplex 0 = Half Duplex
10-11	Speed	Read	00	00 - Reserved 01 - 1000 Mbps 10 - 100 Mbps 11 - 10 Mbps
1-9	Reserved	Returns 0s	000000000	Always return zeros.
0	Reserved	Returns 1	1	Always return one.

Table 89 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Expansion Register bit definitions.

Table 89: SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.

**Table 89: SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions (Cont'd)**

Bit(s)	Name	Core Access	Reset Value	Description
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 90 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Transmit Register bit definitions.

**Table 90: SGMII Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 91 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Receive Register bit definitions.

**Table 91: SGMII Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 92 shows the Hard TEMAC Internal SGMII PCS Management Extended Status Register bit definitions.

Table 92: SGMII Management Extended Status Register (Register 15) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 93 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Interrupt Control Register bit definitions.

Table 93: SGMII Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

## 1000BASE-X PCS/PMA

Please refer to [UG155](#) LogicCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII for an equivalent diagram of the clock management scheme when AXI Ethernet parameter C\_INCLUDE\_IO = "1". When the parameter C\_INCLUDE\_IO = "0", MGTCLK\_P connects directly to the Serial Transceiver. Therefore, the IBUFDS is not used.

### PCS/PMA

The Physical Coding Sublayer (PCS) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and 37 and performs the following:

- Encoding (and decoding) of GMII data octets to form a sequence of ordered sets
- 8B/10B encoding (and decoding) of the sequence ordered sets
- 1000BASE-X Auto-Negotiation for information exchange with the link partner

The Physical Medium Attachment (PMA) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and performs the following:

- Serialization (and de serialization) of code-groups for transmission (and reception) on the underlying serial PMD
- recovery of clock from the 8B/10B coded data supplied by the PMD

1000BASE-X PCS/PMA functionality is provided by connecting the Soft TEMAC silicon component to a GTP transceiver.

### **PMD**

The Physical Medium Dependent (PMD) sublayer is defined in IEEE 802.3 clause 38 for 1000BASE-LX and 1000BASE-SX (long and short wave laser). This type of PMD is provided by the external GBIC or SFP optical transceiver which should be connected directly to the ports of the GTX transceiver.

### **Spartan 6 Soft TEMAC 1000BASE-X Constraints**

Refer to [Answer Record 37174](#) for constraint examples. Refer to [UG625](#) for an overview of the various constraints used.

### **1000BASE-X Auto-Negotiation**

1000BASE-X auto negotiation is described in IEEE Std 802.3, clause 37. This function allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (the link partner on Ethernet), and detect corresponding operational modes advertised by the link partner.

The results of the auto negotiation can be read from the 1000BASE-X Management Auto negotiation Link Partner Ability Base Register ([Table 100](#)). The duplex mode and speed of the AXI Ethernet should then be set to match (see [TEMAC Receive Configuration Word 1 \(RCW1\) Registers - Offset 0x0000\\_0404, page 38](#), [TEMAC Transmit Configuration \(TC\) Registers - Offset 0x0000\\_0408, page 40](#), and [TEMAC Ethernet MAC Mode Configuration \(EMMC\) Registers - Offset 0x0000\\_0410, page 42](#)).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

1. By polling the auto negotiation complete bit of 1000BASE-X Management Status Register (Register 1, bit 5 [Table 71](#)).
2. By using the auto negotiation complete interrupt ([Interrupt Status Registers \(IS\) - Offset 0x0000\\_000C, page 22](#) and 1000BASE-X Management Auto Negotiation Interrupt Control Register [Table 105 on page 116](#).)

### **Loopback**

Unlike the hard TEMAC, there is only one possible loopback position:

- **Loopback in the Soft TEMAC silicon component.** When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the GTP transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the GTP transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet). The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.

Loopback can be enabled or disabled by writing to the 1000BASE-X Management Control Register bit 14 ([Table 95 on page 111](#)).

### **Internal 1000BASE-X PCS/PMA Management Registers**

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the 1000BASE-X PCS/PMA sublayer, including the status of the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the 1000BASE-X auto negotiation function which occurs between AXI Ethernet and its link partner, the Ethernet device connected at the far end of the PHY Link.

These registers are accessed via the MII Management interface ([Using the Address Filters, page 56](#)). These registers are only valid when using the 1000BASE-X PHY interface.

When using 1000BASE-X, AXI Ethernet is typically connected to an external optical transceiver device such as a GBIC or SFP transceiver.

**Table 94: Internal 1000BASE-X PCS/PMA Management Registers**

Register Name	Register Address (REGAD)
Control Register (Register 0)	0
Status Register (Register 1)	1
PHY Identifier (Register 2 and 3)	2,3
Auto Negotiation Advertisement Register (Register 4)	4
Auto Negotiation Link Partner Ability Base Register (Register 5)	5
Auto Negotiation Expansion Register (Register 6)	6
Auto Negotiation Next Page Transmit Register (Register 7)	7
Auto Negotiation Next Page Receive Register (Register 8)	8
Extended Status Register (Register 15)	15
Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 95 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Control Register bit definitions.

**Table 95: 1000BASE-X Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the GTX transceiver is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to signal full duplex mode.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to disable COL test.

Table 95: 1000BASE-X Management Control Register (Register 0) Bit Definitions (Cont'd)

Bit(s)	Name	Core Access	Reset Value	Description
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 96 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Status Register bit definitions.

Table 96: 1000BASE-X Management Status Register (Register 1) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a 1 for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 97 shows the first Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 97: 1000BASE-X Management PHY Identifier (Register 2) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 98 shows the second Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 98: 1000BASE-X Management PHY Identifier (Register 3) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 99 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Advertisement Register bit definitions.

Table 99: 1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - next page functionality is not advertised 1 - next page functionality is advertised
14	Reserved	Returns 0s	0	Always return zeros.
12 - 13	Remote Fault	Read/Write self clearing after auto negotiation	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read/write	0x3	00 - No pause 01 - Symmetric pause 10 - Asymmetric pause towards link partner 11 - both symmetric pause and asymmetric pause towards link partner
6	Half Duplex	Returns 0	0	Always return zeros because half duplex is not supported.
5	Full Duplex	Read/Write	1	0 - full duplex mode is not advertised 1 - full duplex mode is advertised
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 100 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Link Partner Ability Base Register bit definitions.

**Table 100: 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - next page functionality is not supported 1 - next page functionality is supported
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
12 - 13	Remote Fault	Read/	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read	0x	00 - no pause 01 - asymmetric pause supported 10 - symmetric pause supported 11 - both symmetric pause and asymmetric pause supported
6	Half Duplex	Read	0	0 - half duplex mode is not supported 1 - half duplex mode is supported
5	Full Duplex	Read/	0	0 - full duplex mode is not supported 1 - full duplex mode is supported
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 101 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Expansion Register bit definitions.

**Table 101: 1000BASE-X Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 102 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Transmit Register bit definitions.

**Table 102: 1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - last page 1 - additional next page(s) will follow

**Table 102: 1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions (Cont'd)**

Bit(s)	Name	Core Access	Reset Value	Description
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 - 10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 103 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Receive Register bit definitions.

**Table 103: 1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between subsequent pages.
0 - 10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 104 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Extended Status Register bit definitions.

**Table 104: 1000BASE-X Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 105 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Interrupt Control Register bit definitions.

**Table 105: 1000BASE-X Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

## Design Implementation

### Target Technology

The intended target technology are Spartan 6 and Virtex-6 FPGAs.

### Device Utilization and Performance Benchmarks

Because the AXI Ethernet is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are just estimates. As AXI Ethernet is combined with other pieces of the FPGA design, the utilization of the FPGA resources and the timing of AXI Ethernet design will vary from the results reported here. AXI Ethernet benchmarks for GMII systems are shown in Table 106 for a Virtex-6 FPGA. AXI Ethernet benchmarks for GMII systems are shown in Table 107 for a Spartan-6 FPGA with the exception of the last rows in which the SGMII and 1000Base-X PHY types were targeted.

Table 106: Virtex-6 FPGA Performance and Resource Utilization Benchmarks

Parameter Values									Device Resources						
C_(T,R)XMEM	C_(T,R)XCSUM	C_TXVLAN_*	C_RXVLAN_*	C_MCAST_EXTEND	C_STATS	C_AVB	C_TYPE	C_PHY_TYPE	Slices	Flip- Flops	BRAMs (RAMB36E1/ FIFO36E1)	BRAMs (RAMB18E1/ FIFO18E1)	LUTs	BUFGs	BUFRs
2048	0	0	0	0	0	0	1	1	1132	3173	4	0	3006	1	1
2048	0	0	0	0	0	0	2	1	885	2104	4	0	1880	1	1
16384	0	0	0	0	0	0	1	1	1225	3277	11	0	3188	1	1
16384	1	0	0	0	0	0	1	1	1305	3503	11	0	3434	1	1
32768	0	0	0	0	0	0	1	1	1479	3316	21	0	3235	1	1
32768	1	0	0	0	0	0	1	1	1588	3539	21	0	3552	1	1
16384	0	0	0	0	0	0	2	1	1064	2208	11	0	2117	1	1
16384	1	0	0	0	0	0	2	1	1018	2433	11	0	2446	1	1
32768	0	0	0	0	0	0	2	1	1009	2248	21	0	2237	1	1
32768	1	0	0	0	0	0	2	1	1240	2471	21	0	2578	1	1
32768	1	0	0	0	1	0	2	1	1591	3296	21	0	3310	1	1
32768	1	0	0	1	1	0	2	1	1466	3478	22	0	3478	1	1
32768	0	0	1	1	1	0	2	1	1544	3537	24	0	3406	1	1
32768	0	1	1	1	1	0	2	1	1735	3876	26	0	3750	1	1
32768	0	0	0	0	0	1	2	1	1591	3723	23	0	3417	2	1
32768	0	0	0	0	1	1	2	1	1994	4548	23	0	4120	2	1
32768	1	0	0	0	1	1	2	1	2045	4772	23	0	4498	2	1

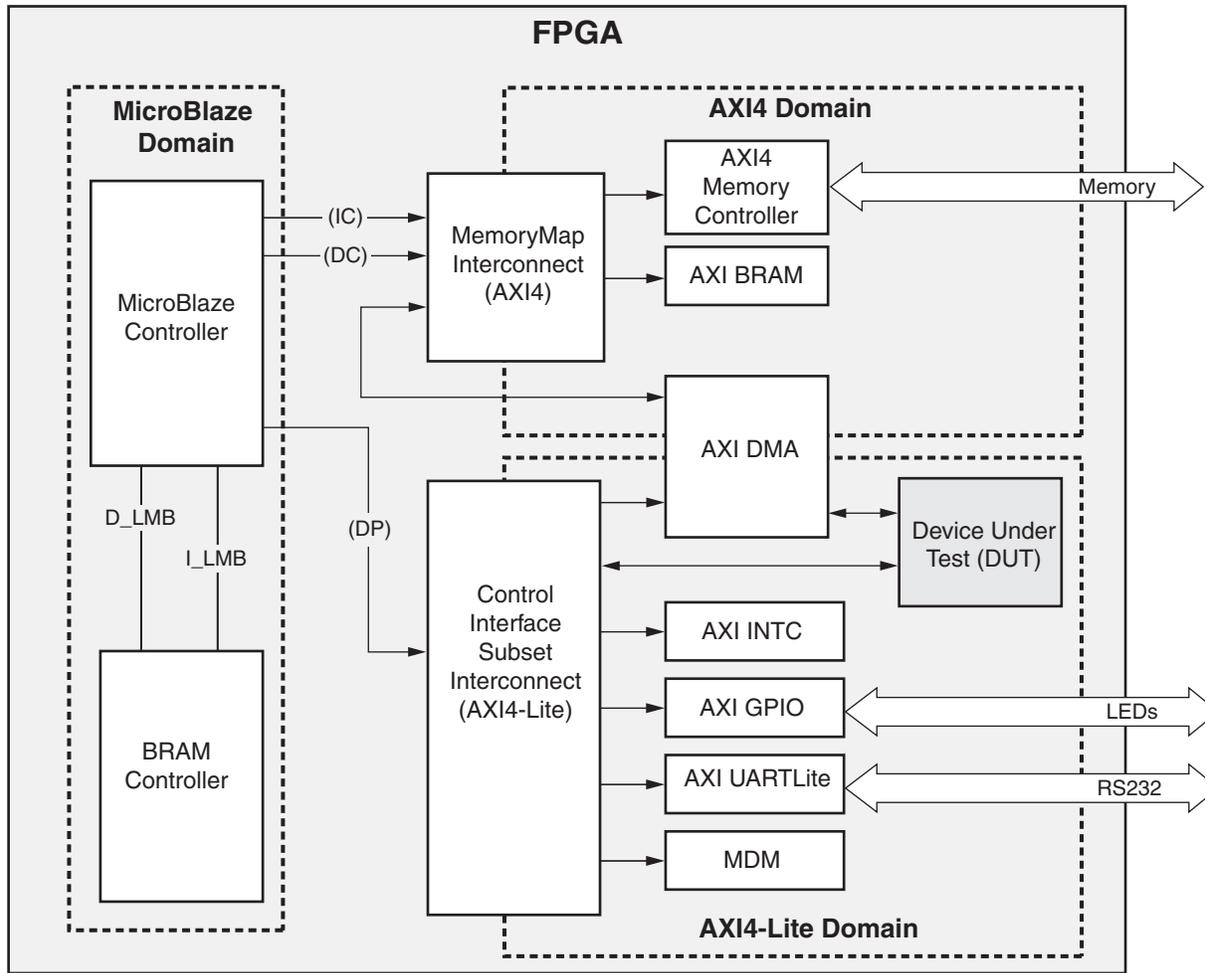
Table 107: Spartan-6 FPGA Performance and Resource Utilization Benchmarks

Parameter Values									Device Resources						
C_(T,R)XMEM	C_(T,R)XCSUM	C_TXVLAN_*	C_RXVLAN_*	C_MCAST_EXTEND	C_STATS	C_AVB	C_TYPE	C_PHY_TYPE	Slices	Flip- Flops	BRAMs (RAMB16BWER)	BRAMs (RAMB8BWER)	LUTs	BUFGs	BUFIOs
2048	0	0	0	0	0	0	1	1	1453	3181	4	0	3094	3	1
16384	0	0	0	0	0	0	1	1	1565	3265	21	0	3218	3	1
16384	1	0	0	0	0	0	1	1	1561	3490	21	0	3481	3	1
32768	0	0	0	0	0	0	1	1	1632	3308	41	0	3380	3	1
32768	1	0	0	0	0	0	1	1	1622	3532	41	0	3705	3	1
32768	1	0	0	0	1	0	1	1	1981	4359	41	0	4400	3	1
32768	1	0	0	1	1	0	1	1	2087	4538	43	0	4568	3	1
32768	0	0	1	1	1	0	1	1	2159	4599	46	1	4555	3	1
32768	0	1	1	1	1	0	1	1	2274	4940	49	2	4874	3	1
32768	0	0	0	0	0	1	1	1	2177	4779	44	0	4543	4	1
32768	0	0	0	0	1	1	1	1	2493	5604	44	0	5233	4	1
32768	1	0	0	0	1	1	1	1	2594	5828	44	0	5519	4	1
32768	1	0	0	0	1	1	1	4	2659	6436	44	1	6057	4	1
32768	1	0	0	0	1	1	1	5	2662	6276	44	0	5932	3	1

### System Performance

To measure the system performance ( $F_{MAX}$ ) of the AXI Ethernet core, it core was added to a Virtex-6 FPGA system and a Spartan-6 FPGA system as the Device Under Test (DUT) as shown in [Figure 66](#).

Because AXI Ethernet core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the core design will vary from the results reported here.



DS759\_6t

Figure 66: Virtex-6 and Spartan-6 FPGA System Configuration with the AXI Ethernet as the DUT

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target  $F_{MAX}$  numbers are shown in Table 108.

Table 108: System Performance

Target FPGA	Target $F_{MAX}$ (MHz)
xc6slx45t <sup>(1)</sup>	90
xc6vlx240t	150

**Notes:**

1. LUT utilization ~60%, BRAM utilization ~ 70%, I/O utilization ~80%

The target  $F_{MAX}$  is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

## Specification Exceptions

The AXI Ethernet design has no exceptions to the IEEE Std 802.3-2002 specification mandatory requirements.

## Reference Documents

Please note that the links to the documents below are updated over time and may not match the version that is used in AXI Ethernet. At the time this core was released, the version for each helper core is listed in parenthesis at the end of the helper core title.

1. [UG368](#) Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide
2. [UG366](#) Virtex-6 FPGA GTX Transceivers User Guide
3. [UG138](#) LogiCORE IP Tri-Mode Ethernet MAC User Guide (v4.4)
4. [UG386](#) Spartan-6 FPGA GTP Transceivers User Guide
5. [UG155](#) LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII (v10.4)
6. [UG170](#) LogiCORE IP Ethernet Statistics User Guide (v3.1)
7. [UG492](#) LogiCORE IP Ethernet AVB Endpoint (v2.2)
8. [UG625](#) Constraints Guide
9. [DS781](#) AXI\_DMA Data Sheet (v1\_00\_a)
10. [UG382](#) Spartan-6 FPGA Clocking Resources User Guide
11. [UG362](#) Virtex-6 FPGA Clocking Resources User Guide
12. ARM AMBA® AXI Protocol v2.0 Specification (ARM IHI 0022C)
13. ARM AMBA® 4 AXI4-Stream Protocol v1.0 Specification (ARM IHI 0051A)
14. ARM Control Interface Proposal (PR313-GENC-009384 0.5)
15. [Embedded Processing Peripheral IP Cores](#)
16. [Answer Record 37174](#)

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Ordering Information

This Xilinx LogiCORE IP module, AXI-Ethernet, is made up of several different helper modules which are licensed under different terms and conditions. A free evaluation version of all configurations is included with ISE Design Suite Embedded Edition software. Please use the Xilinx Platform Studio application (XPS) included with the Embedded Edition software to instantiate and use this core.

For full access or more information on a module, please refer to the product web page below and please contact your local Xilinx sales representative for pricing and availability of any Xilinx LogiCORE IP or software.

For more information, please visit the [AXI Ethernet](#) product web page.

For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your [local Xilinx sales representative](#).

## Revision History

Date	Version	Revision
9/21/10	1.0	Xilinx initial release.
12/14/10	1.1	Updated to v1.01a; removed references to Null Strobes and Null Transfers.

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