Quick Front-to-Back Overview Tutorial

PlanAhead Design Tool

UG673 (v14.5) April 10, 2013

This tutorial document was last validated using the following software version: ISE Design Suite 14.5

If using a later software version, there may be minor differences between the images and results shown in this document with what you will see in the Design Suite.

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Notice of Disclaimer

Revision History

Date	Version	Revision
04/10/2013	14.5	Validated with Release.

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Quick Front-to-Back Overview Tutorial

Introduction

This tutorial provides a quick introduction to some of the capabilities and benefits of using the Xilinx® PlanAhead™ design tool. The PlanAhead tool can be used during various stages of the design process for a variety of purposes.

Many of the PlanAhead tool analysis features are covered in more detail in other tutorials. Not every command or command option is represented here. This tutorial uses the features contained in the PlanAhead design tool product, which is bundled as a part of the ISE® Design Suite.

Tutorial Design Description

The small sample design used throughout this tutorial consists of a design called `bft`. There are several VHDL and Verilog source files in the bft design.

The design targets an xc7k70t device. A small design is used to allow the tutorial to be run with minimal hardware requirements and to enable timely completion of the tutorial, as well as to minimize the data size.

Software Requirements

The PlanAhead tool is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead tool is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)*.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller xc7k70t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Preparing the Tutorial Design Files

Copy the files from the ISE software installation area:

***<ISE_install_area>*/ISE_DS/PlanAhead/examples/PlanAhead_Tutorial.zip**

Extract the zip file contents into any write-accessible location which will be referred to in this tutorial as the extraction directory, or <*Extract_dir*>.

RECOMMENDED: *The tutorial sample design data is modified while performing this tutorial. A new copy of the original PlanAhead_Tutorial data should be extracted each time you run this tutorial.*

Lab 1: Front-to-Back Overview

Step 1: Creating a New Project

PlanAhead tool enables several types of projects to be created depending on where in the design flow the tool is being used. Register Transfer Level (RTL) sources can be used to create a project for development and analysis, synthesis, implementation and BIT file creation.

- On Windows, double-click the **Xilinx PlanAhead 14.4** Desktop icon, or select:

Start > All Programs > Xilinx Design Tools > ISE Design Suite 14.4 > PlanAhead > PlanAhead[1]

- On Linux, change the directory to `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data`, and type **planAhead**.

The PlanAhead Getting Started page opens with links to create new projects, open existing or example projects, and view the documentation.

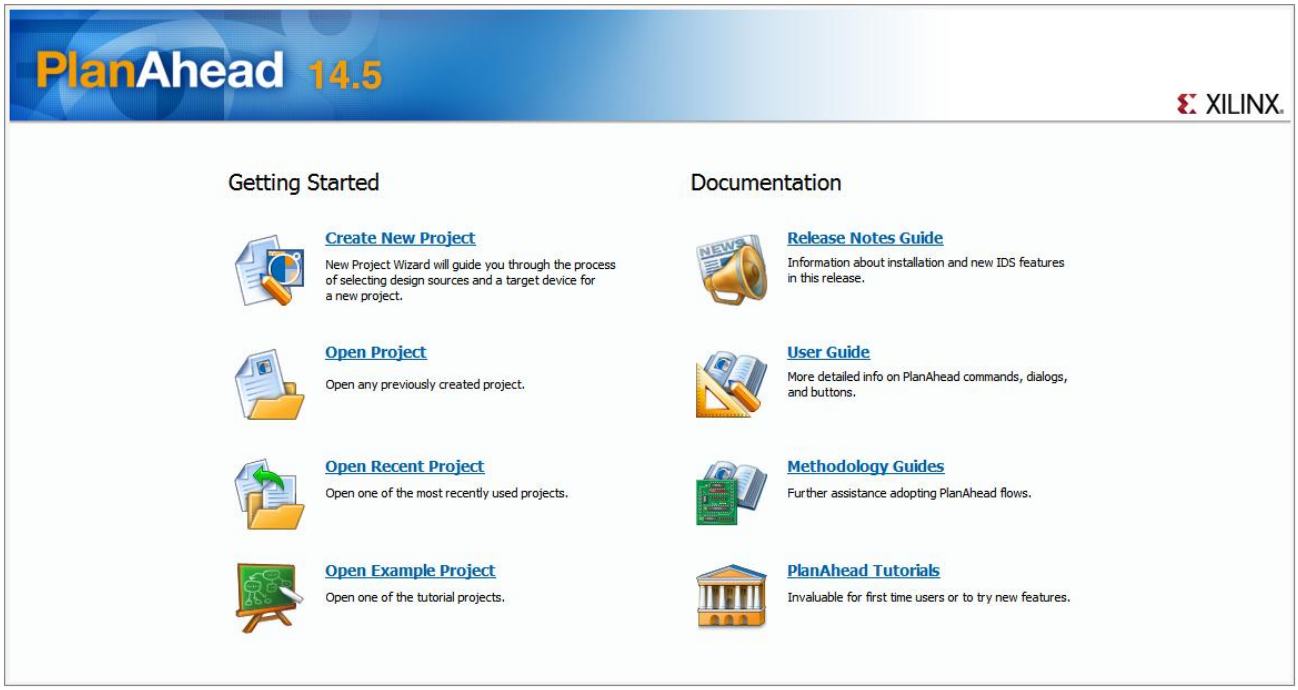

Figure 1: Getting Started Page

[1] Your installation may not be called Xilinx Design Tools on the Start menu.

Creating a new RTL Project

This step uses RTL Source Files from the Tutorial directory:

<*Extract_Dir*>/PlanAhead_Tutorial/Sources/hdl

1. Select the **Create New Project** link on the Getting Started page.

   The Create a New PlanAhead Project confirmation dialog box opens.

2. Click **Next**.

   The Project Name page opens.

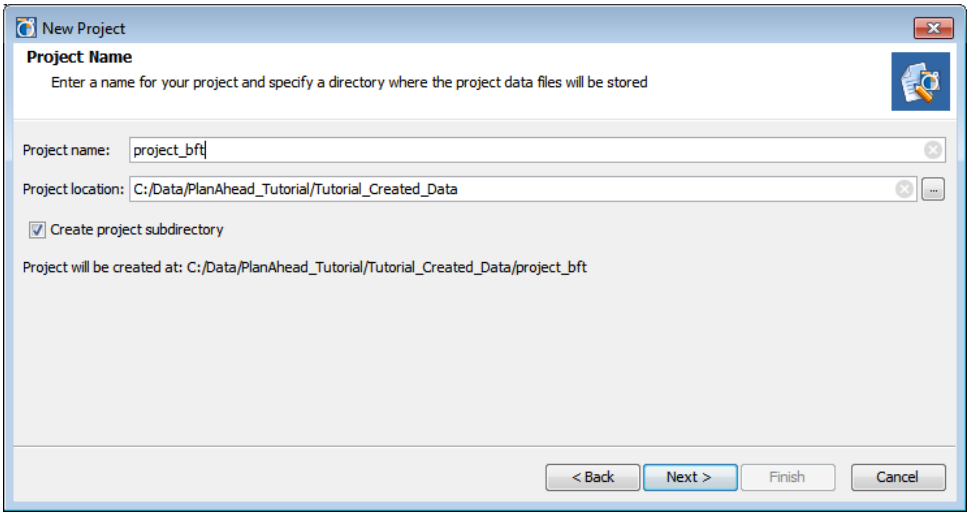

Figure 2: New Project Name and Location Page

3. Set the Project location to:
   `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data`.
4. Enter the Project name: **project_bft**, then click **Next**.

   The Design Source page opens.

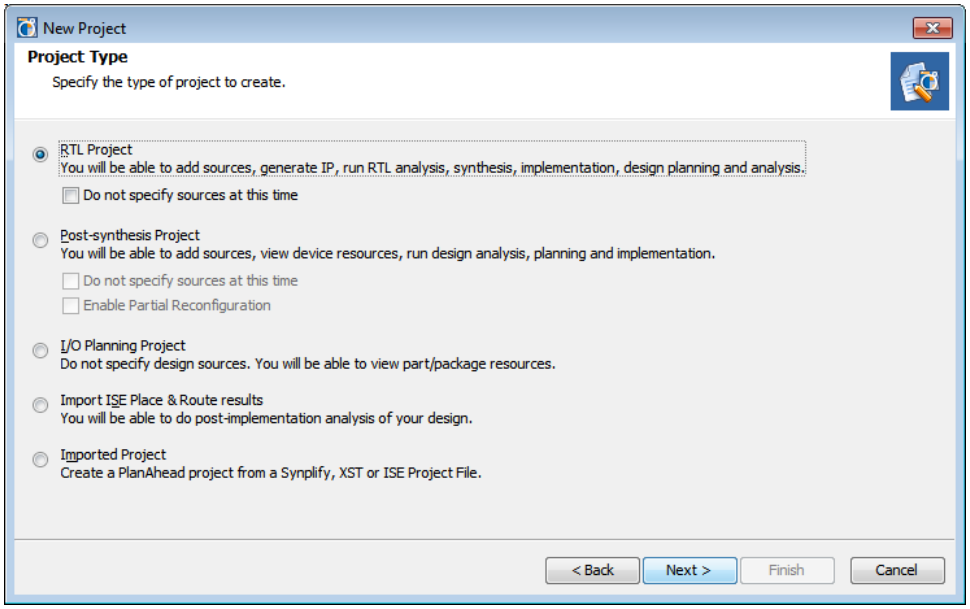

Figure 3: New Project Design Sources

5. Click the **RTL Project** option, and then click **Next**.

   The Add Sources page opens.

Adding Source Files

1. Click the **Add Files** button and browse to the following directory:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl`
2. Press the **Ctrl** key to select **async_fifo.v**, **bft.vhdl**, **bft_tb.v**, and **FifoBuffer.v**, and click **OK**.
3. Set the simulation test bench file `bft_tb.v` as a Simulation only source file.
4. Click on the **Synthesis and Simulation** entry in the HDL Source for field for `bft_tb.v` and select **Simulation only**.
5. Click the **Add Directories** button, and browse to select the following directory:

`<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl/bftLib`.

6. Set the VHDL Library for all of the sources in the bftLib directory.
7. Click on the **work** entry in the Library field for bftLib, and type **bftLib**.
8. If needed, click these two checkboxes to select **Copy Sources into Project**, and **Add Sources from Subdirectories**.
9. Verify that the page looks like the following figure.

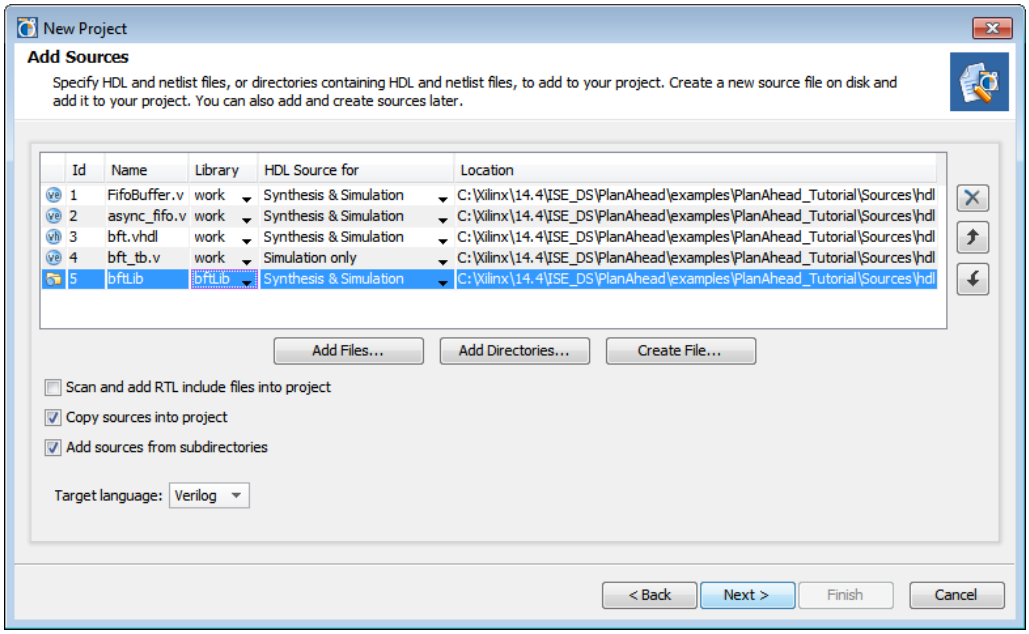

Figure 4: New Project: Selecting Sources to Add to the Project

10. Click **Next**.

    The Add Existing IP page opens. You can select existing IP (Intellectual Property) from CORE Generator™ software `.xco` project files. However, this tutorial does not include importing IP into the project.

11. Click **Next.**

    The Constraints Files page opens.

Adding a Constraint File

1. Click the **Add Files** button, browse to select the following file:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/bft_full.ucf`

2. Click **OK**.

   The `bft_full.ucf` file appears in the Add Constraints dialog box.

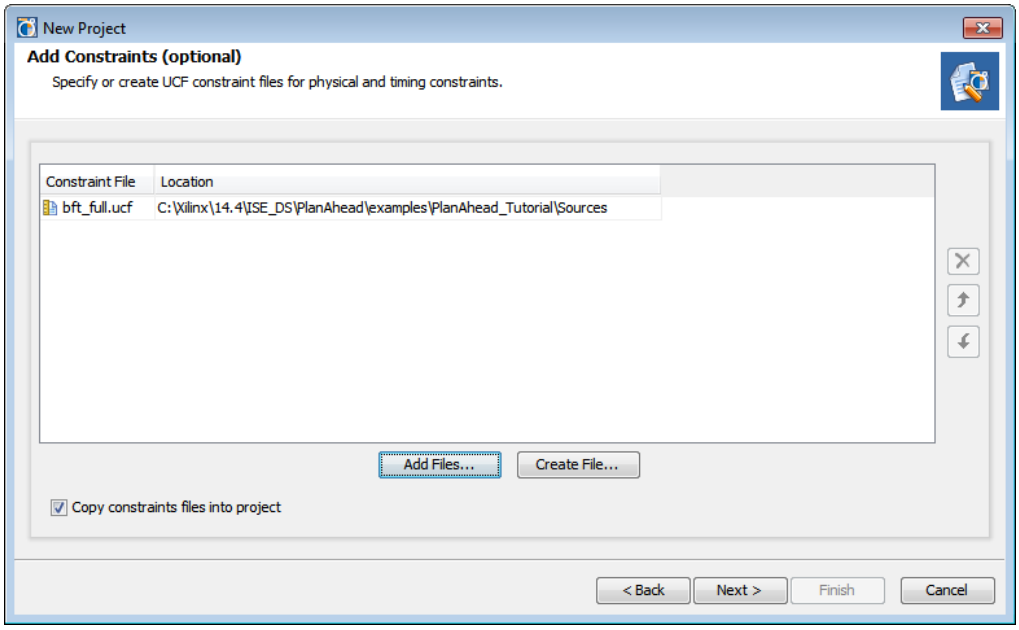

Figure 5: New Project: Adding Constraint Files

3. Make sure the **Copy constraints into project** checkbox is enabled.
4. Click **Next**.

   The Default Part page opens.

Selecting a Default Part

1. In the Filter section, click the Family pull-down menu and select **Kintex-7**.

   Notice the list is filtered to only show Kintex®-7 devices.
2. In the Search field, type **70t**.

   Notice the 70t devices listed.
3. Select the **xc7k70tfbg484-2** device, and click **Next**.

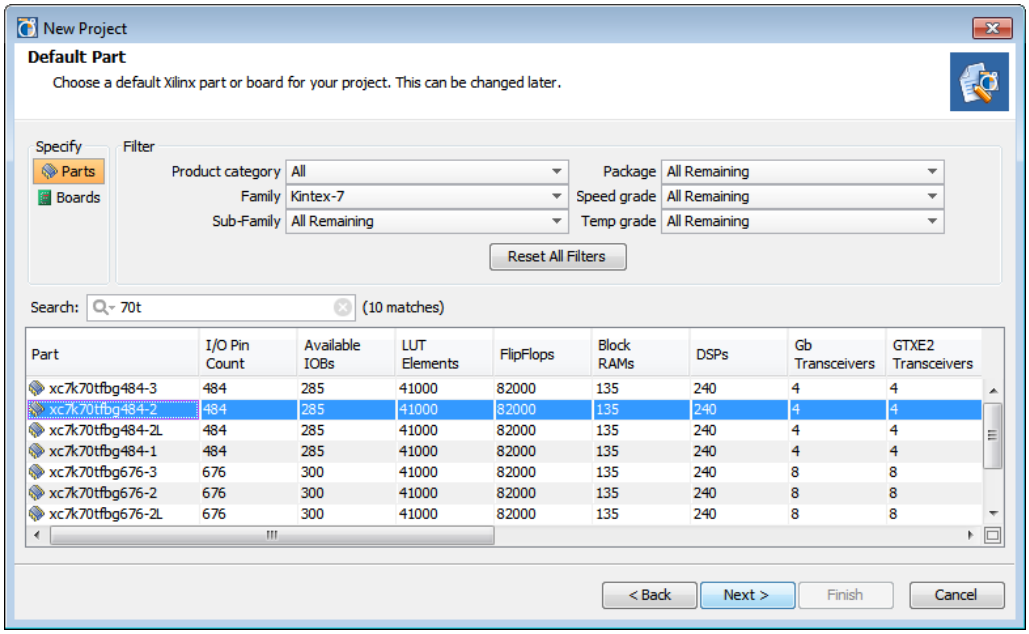

Figure 6: New Project: Selecting a Family and Default Part

4. Review the New Project Summary page, and click **Finish.**

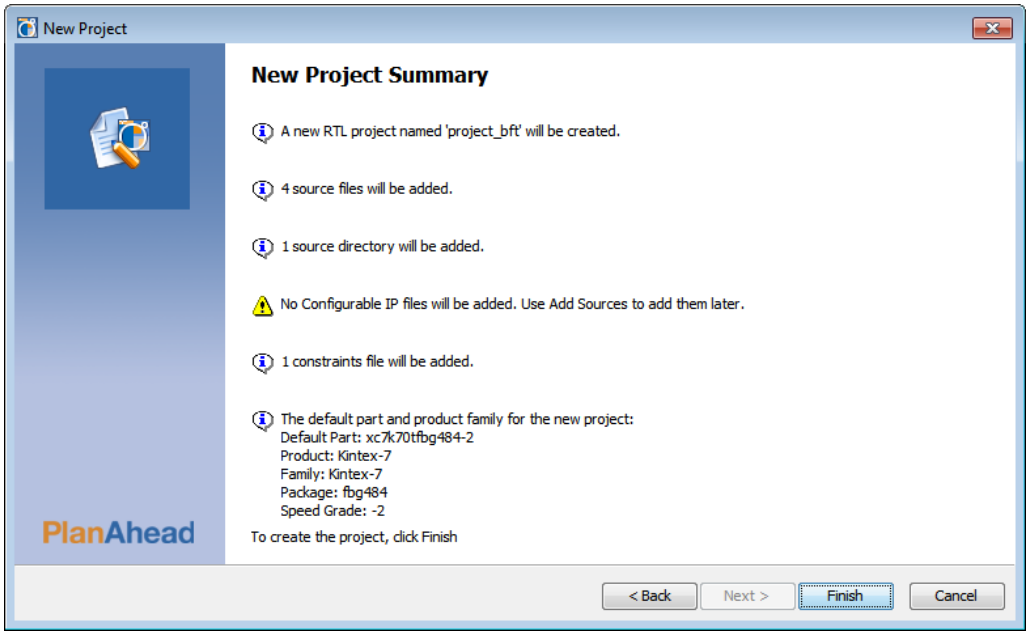

Figure 7: New Project Summary

The PlanAhead environment opens. The Flow Navigator is located on the left edge. It will be used throughout the rest of the tutorial to explore and implement the design.

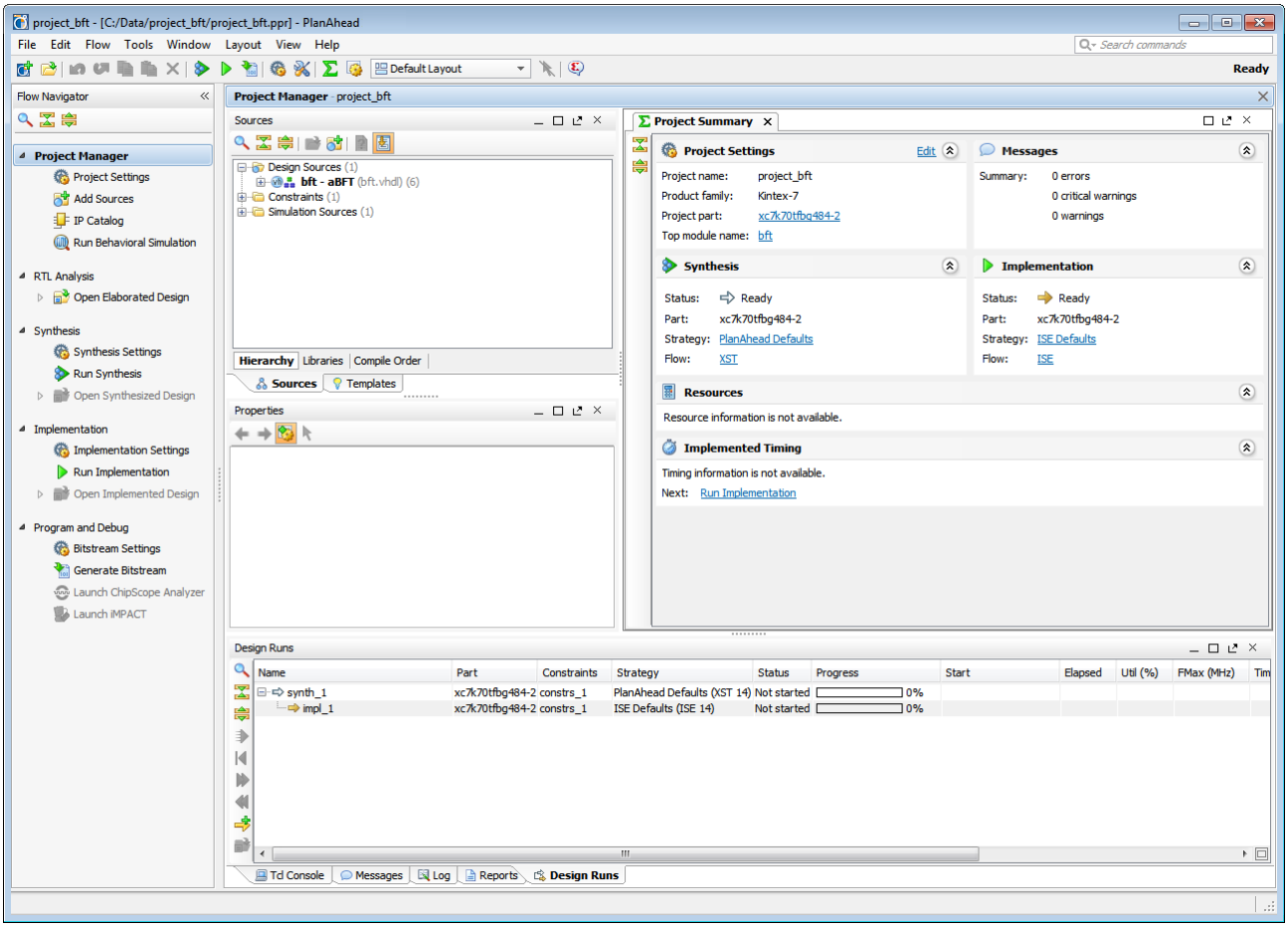

Figure 8: PlanAhead Environment

Step 2: Using the Sources View and the Text Editor

The PlanAhead tool allows different file types to be added as design sources including Verilog, VHDL, NGC format cores, UCF/NCF constraint files, and specific simulation sources. The files display by Hierarchy, Library or Compile Order in the Sources view. A text editor is supplied to create or develop RTL sources. Third party text editors can also be configured.

Exploring the Sources View and Project Summary

1. Look at the information presented in the Project Summary. This window is updated as the design progresses through the design flow.
2. In the Sources view, **click** on the '**+**' icon to expand the `bft` module.

   You can see the various RTL source files that you added when you created the project. Remember, you added RTL files and the `bftLib` directory, and its sub-directories.
3. In the Sources view, **click** on the '**+**' icon to expand the Constraints folder.

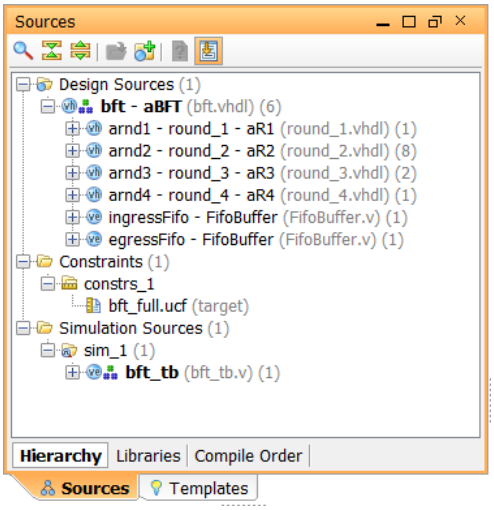

Figure 9: Viewing Sources

In the Sources view the Design Sources folder helps keep track of VHDL and Verilog source files. Notice the Hierarchy tab is displayed by default, showing the design hierarchy. The Filter Sources by Missing Files or Instantiations button is disabled, which means the displayed hierarchy is complete. If this were enabled, you could use it to resolve any missing source files in your design.

The Source types are broken out into separate folders for Design Sources, Constraints, Simulation Sources, IP, etc. In the Libraries tab, sources are grouped by file type, while the

Compile Order tab shows the file order used for synthesis. Any IP in the project would be shown in a separate IP tab in the Sources view.

Opening the Text Editor

1. Select one of the VHDL sources in the Sources view.
2. Right-click to review the commands available in the Sources view popup menu.
3. Select **Open File**, and use the scroll bar to browse the text in the Text Editor.

TIP: *Alternatively, you can double-click on source files in the Sources view to open them in the Text Editor.*

4. With the cursor in the Text Editor, right-click and select **Find in Files**.

   The Find in Files dialog box opens with various search options.

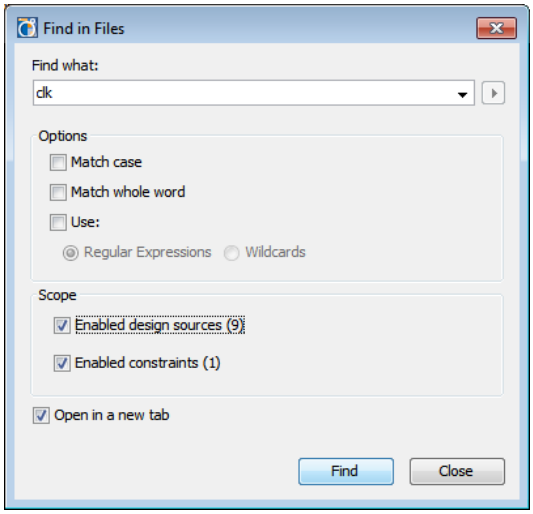

Figure 10: Using the Find in Files Command

5. Type **clk**, and click **Find**.

   The Find in Files view displays in the messaging area at the bottom of the PlanAhead environment.

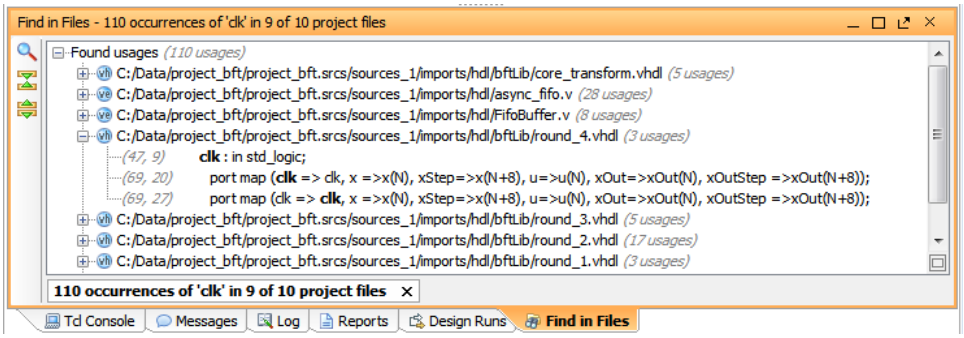

Figure 11: Viewing the Find in Files Results

6. In the Find in Files view, expand and select one of the occurrences of `clk` and notice that the source file is opened in the Text Editor, and the specific occurrence is highlighted.
7. Close the **Find in Files** view.
8. Close each of the open RTL file tabs in the Text Editor.

The PlanAhead tool also includes an RTL analysis and IP customizing environment. This environment is covered in the *RTL Design and IP Generation Tutorial: PlanAhead Design Tool* (*UG675*).

When you click the **Open Elaborated Design** button under RTL Analysis in the Flow Navigator, the RTL design is elaborated, enabling various views of the design including an RTL Netlist, Schematic view, Hierarchy view, and estimated resource statistics. The different views have a "cross-select" feature, which helps you to debug and optimize the RTL design. There are also several RTL Design Rule Checks (DRCs) to check for areas to improve performance or power.

The Xilinx IP Catalog provides access to the Xilinx CORE Generator™ tool to generate IP. You can sort and search the Catalog in a variety of ways. IP can be customized, generated, and instantiated.

Step 3: Simulating the Design

The PlanAhead tool is integrated with the Xilinx ISim logic simulation environment. The PlanAhead tool enables you to add and manage synthesis sources in the project. You can configure simulation options and create and manage various simulation source sets. You can launch behavioral simulation prior to synthesis using RTL sources and launch timing simulation post-implementation.

The Behavioral Simulation command configures and launches a single ISim run, which is the basic flow used in this tutorial. It can be accessed in the Flow Navigator view on the left side of the PlanAhead environment, shown in the following figure.

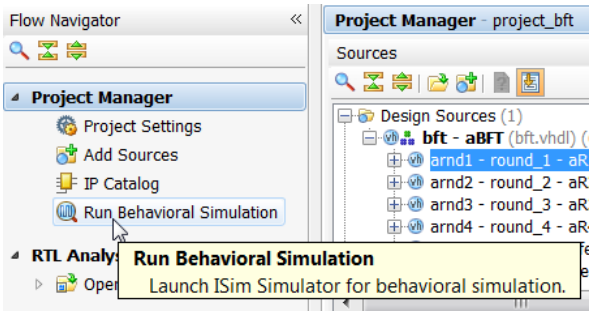

Figure 12: Launching Behavioral Simulation

1. Select Project Settings from the top of the Flow Navigator.

   Notice the simulation related options in the General Options dialog such as Language Options.

2. Select the **Simulation** icon on the left to view Simulation specific options.

3. Toggle the **Target simulator** field to notice the choices of QuestaSim/ModelSim or ISim Simulator.

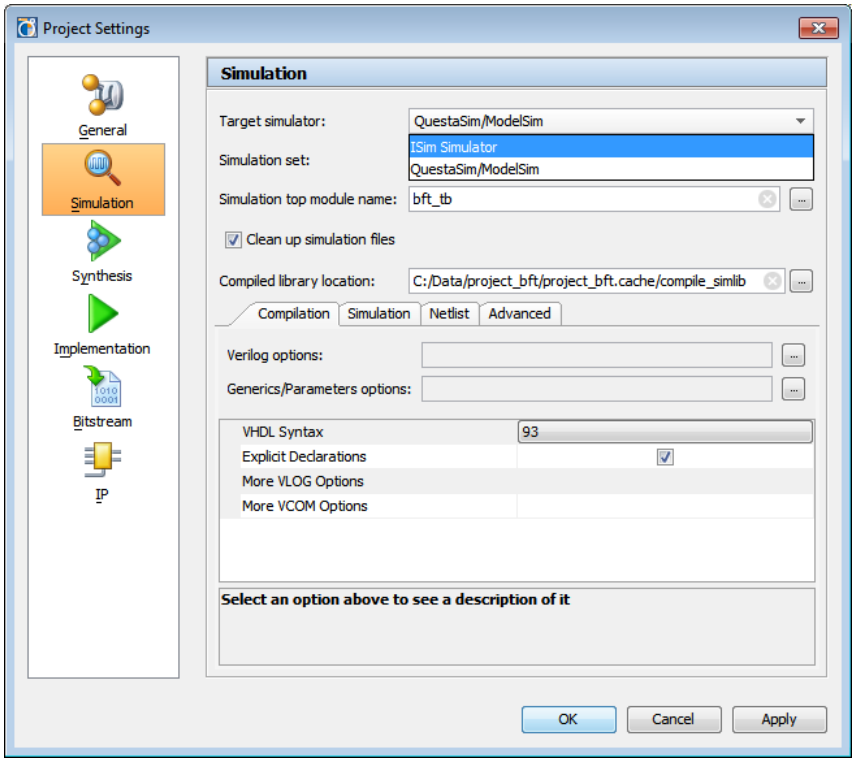

Figure 13: Launching Behavioral Simulation

4. Select ISim Simulator.

5. Examine the various options of the Project Settings dialog box and click **Cancel**.
6. In the Flow Navigator, select **Run Behavioral Simulation**.

   The Launch Behavioral Simulation dialog box opens.

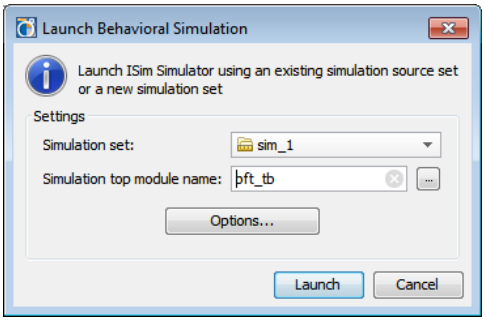

Figure 14: Launch Behavioral Simulation

7. If bft_tb is not specified as the **Simulation Top Module Name**, click the browse button ... , and select **bft_tb**, and click **OK**.
8. Click the **Options** button.

   The **Simulation Options** dialog box opens.

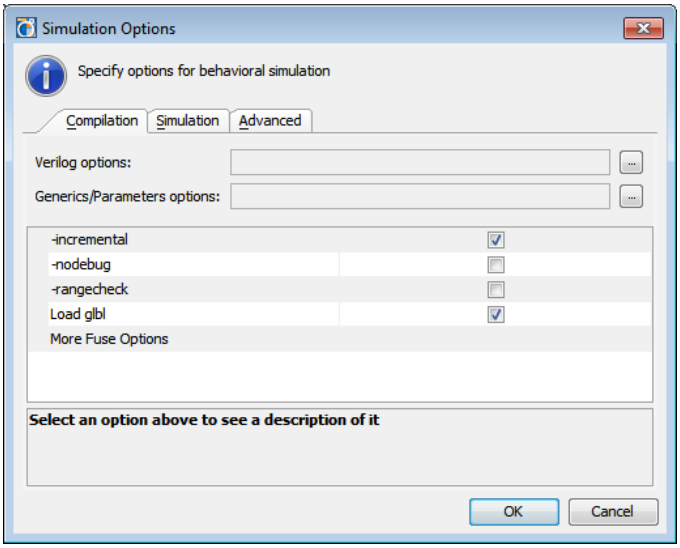

Figure 15: Simulation Options

   Notice the various options on the **Compilation** tab.

9. Click the **Simulation** tab and the **Advanced** tab, and examine the various options.
10. Click **Cancel**.

11. Click **Launch** to invoke the ISE Simulator (ISim) simulation environment.

    The ISim simulation environment opens.

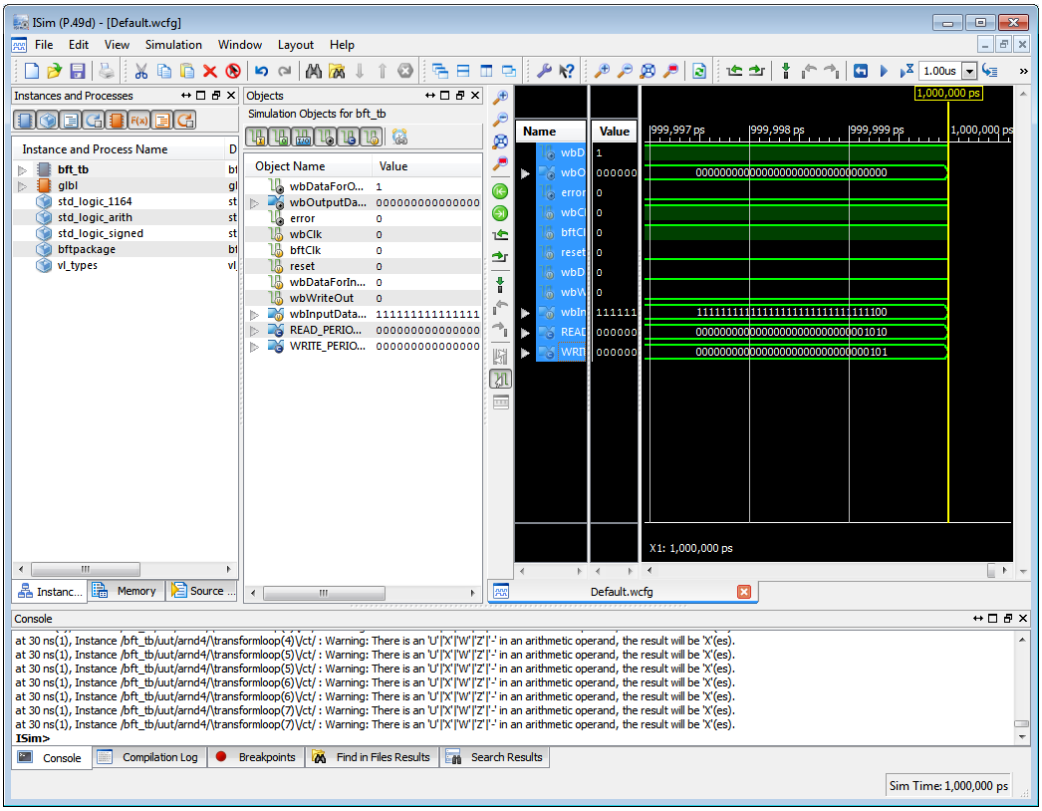

Figure 16: ISim Simulation Environment

Editing RTL source files in the ISim environment results in the PlanAhead source files being updated as well. The two tools are referencing the same source files. Refer to the *ISim In-Depth Tutorial (UG682)*, for information about using ISim.

12. In ISim, select **File > Exit** and click the **Yes** button if prompted to close ISim.

Step 4: Synthesizing the Design

The PlanAhead tool enables one or more synthesis runs to be configured, launched, and monitored, either sequentially or simultaneously.

The Synthesize command configures and launches a single run which is the basic flow used in this tutorial. It can be accessed in the Flow Navigator view on the left side of the PlanAhead Environment.

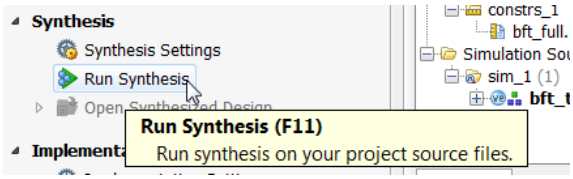

Figure 17: Flow Navigator - Synthesize Drop Down Menu

The Flow Navigator launches all major design compilation processes including synthesis, implementation, and generate bitstream. Optionally, it also lets you open the Elaborated RTL Design, the Synthesized Design, and the Implemented Design results to enable design analysis and constraints assignment at each phase of the design process.

Exploring Synthesis Options

1. In the Flow Navigator, select **Synthesis Settings**.

   The Synthesis Project Settings dialog box opens.

2. Review the available options.
3. Click the **Strategy** drop-down menu and review the available Synthesis Strategies
4. Click **Cancel**.

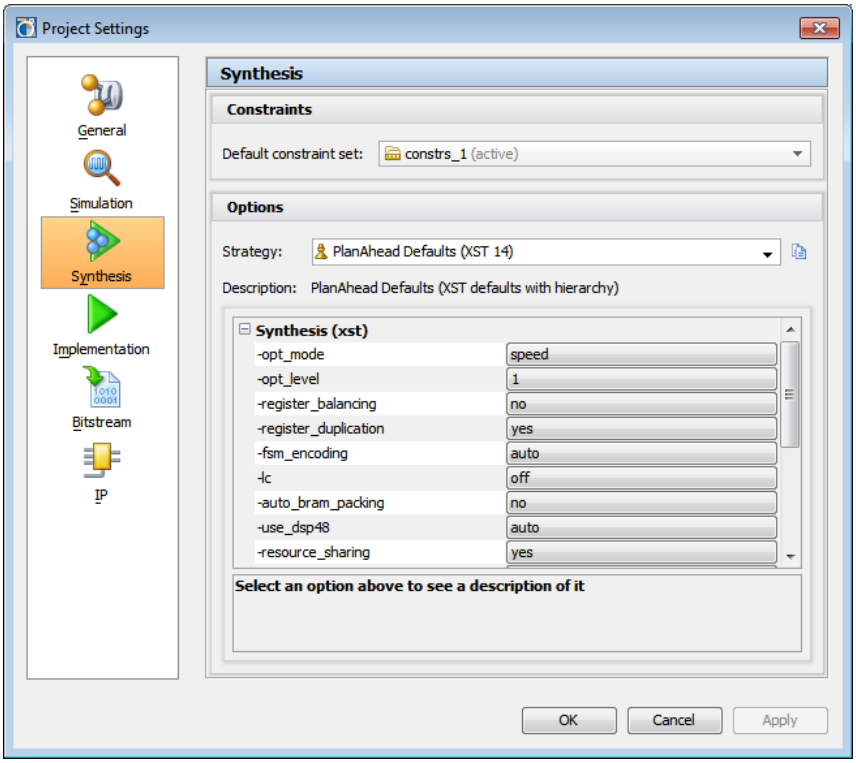

Figure 18: Synthesis Settings

Running Synthesis

1. In the Flow Navigator click **Run Synthesis** to launch the run.

   Notice the Status bar in the upper right corner displays Running XST, which indicates that synthesis is now running. Clicking the Cancel button halts the synthesis run and removes run data.

   The Log view displays the output messages from the ISE commands, and the Messages view displays a filtered list of Warnings and Errors. Clicking on the Synthesis messages in the Messages view opens the RTL file and displays the corresponding line of RTL code that the message is referencing.

TIP: *Right-clicking on Synthesis in the Flow Navigator displays a menu of additional commands and launch options.*

2. When the synthesis run completes, select **Open Synthesized Design** in the **Synthesis Completed** dialog box and click **OK**.
3. If prompted, click **Yes** to close the RTL Design.

The PlanAhead Synthesized Design environment displays with the synthesized netlist, target part, and active constraint set applied.

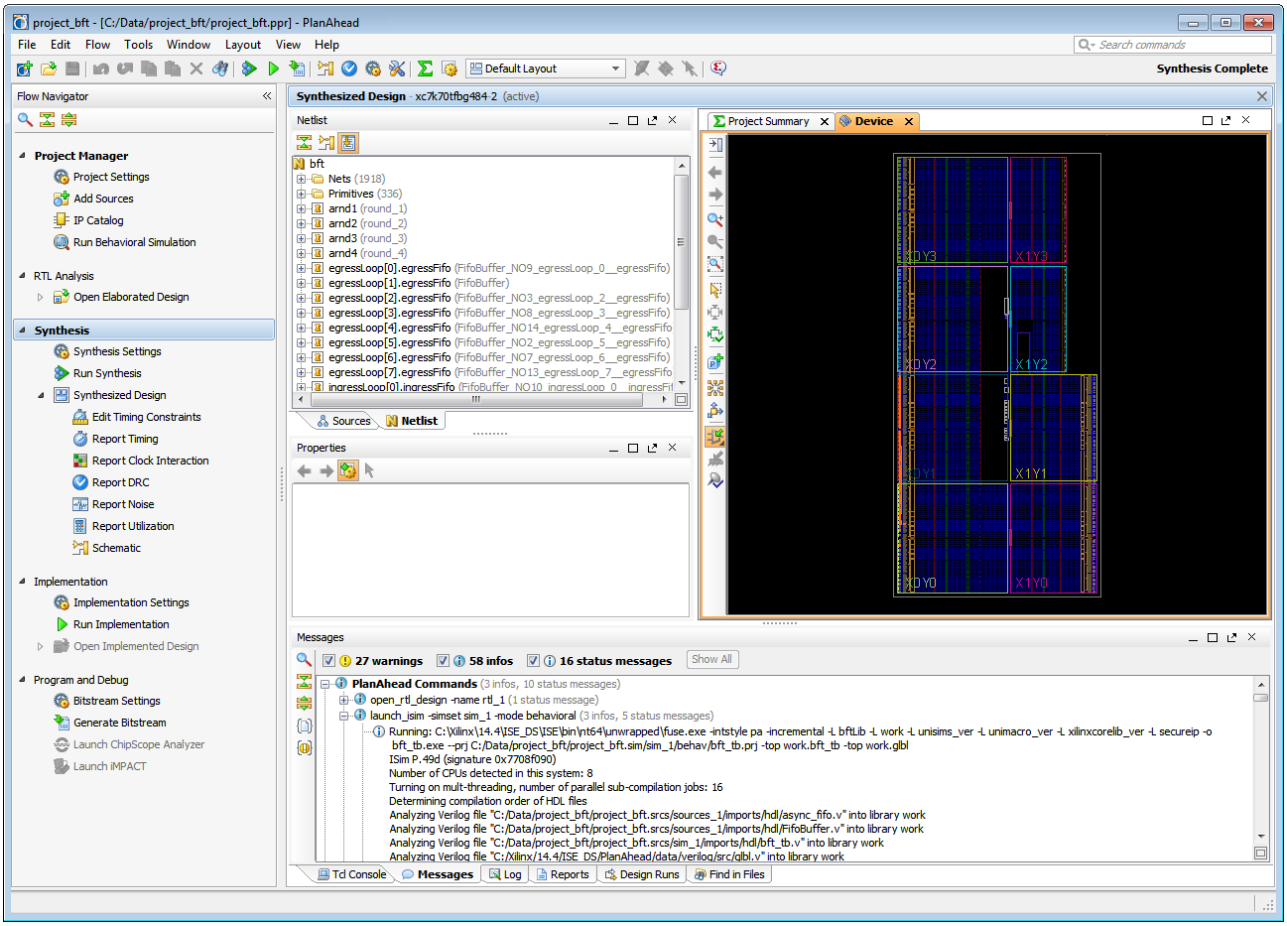

Figure 19: Opening the Synthesized Design

TIP: *Right-clicking on Synthesis in the Flow Navigator and selecting the New Synthesized Design command enables additional Synthesized Designs to be opened simultaneously with different netlists, constraints, or target devices.*

Viewing the Synthesis Report

1. Click the **Reports** view tab at the bottom of the PlanAhead environment.

   If there is no view tab available, select **Window > Reports**.

2. Double-click the **XST Report** to view the XST report in the Workspace.
3. To examine the XST report scroll, through the report.

4. Close the XST Report by clicking on the **X** in the view tab.

   The PlanAhead tool also includes a ChipScope™ debug core insertion environment. This environment is covered in the PlanAhead Software Tutorial: Debugging with ChipScope (*UG677*). You can use the PlanAhead features to explore and select logic signals to debug. The debug cores can be configured, implemented, and automatically added into the top level design netlist. The cores are also maintained through design netlist iterations.

   The PlanAhead tool provides a powerful design analysis and floorplanning environment to explore and experiment with the design. This environment is covered in the Design Analysis and Floorplanning Tutorial: PlanAhead Design Tool (*UG676*).

   Notice the available commands in the Flow Navigator under Synthesized Design.

5. Select **Tools** from the PlanAhead main menu and examine the available commands.
6. Select **I/O Planning** from the View Layout pull-down menu in the toolbar at the top of the PlanAhead environment.

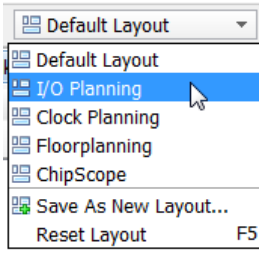

Figure 20: Opening the I/O Planning View Layout

   There are several different layouts of the tool views available to help you perform different design tasks. For example, the I/O Planning layout provides views to enable I/O pin exploration and constraint assignment. The Design Analysis layout provides views to analyze the logic in the design and apply constraints. You can also create and display custom layouts. The last layout selected will be used by default the next time that design is opened.

   Note: The I/O planning environment is covered in the I/O Pin Planning Tutorial: PlanAhead Design Tool (*UG674*).

7. Examine the various views and information presented, for example the Package view in the workspace and the I/O Ports view.
8. Select **Default Layout** from the same pull-down menu in the toolbar.

You can close the Synthesized Design environment after your analysis and constraint definition completes. This helps preserve system memory and avoids having multiple editing environments open simultaneously. For the purposes of this tutorial, it is left open. You can Click the Close button in the view banner or select Close from the Synthesis pull-down menu in the Flow Navigator to close the Synthesized Design.

Step 5: Implementing the Design

The PlanAhead tool provides the flexibility for experimenting with implementation options. You can apply multiple implementation Strategies to multiple runs to find the best performing results.

Exploring Implementation Options

1. In the Flow Navigator, select **Implementation Settings**.

   The Implementation Project Settings open.

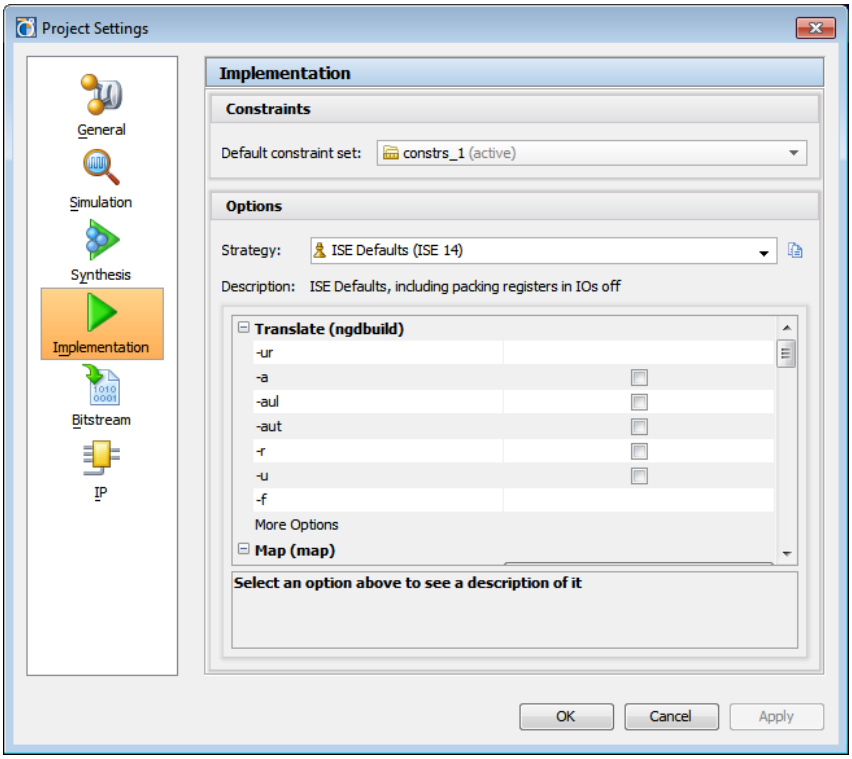

Figure 21: Implementation Settings

   Notice the ability to configure the Constraint Set to be applied to the run.

2. Examine the Implementation Options
3. Click the **Strategy** drop-down menu and review the available Implementation Strategies and click **Cancel**.

Launching Implementation

1. In the Flow Navigator, click **Run Implementation** to launch the run.

   Notice the Status in the upper right corner displays Running NGDBuild, indicating that ISE implementation is now in progress.

   The Log view displays the output of the ISE commands, and the Messages view displays a filtered list of Warnings and Errors.

   The implementation run is processed in the background, so that you can continue with other design tasks in necessary. While the run is implementing, you could click any of the post-synthesis analysis features such as timing, power, and utilization reporting in the Flow Navigator.

2. After the Run completes, select the **Open Implemented Design** option in the Implementation Completed dialog box, and click **OK.**

3. Click **Yes** to close the Synthesized Design before opening the Implemented Design.

Step 6: Analyzing the Results

The PlanAhead tool enables placement and timing results to be imported quickly for analysis from any of the completed runs. The PlanAhead tool imports placement and displays it in the form of "unfixed" LOC placement constraints. The TRACE timing results display in the Timing view.

For more information about Design Analysis and Floorplanning, see Design Analysis and Floorplanning Tutorial: PlanAhead Design Tool (*UG676*).

The PlanAhead environment displays the loaded implemented design, seen in Figure 23.

Clicking the Open Implemented Design button in the Flow Navigator also opens the Implemented Design environment. There are options in the pull-down menu for opening Implemented Designs with different run results.

Notice the placement is imported into the Device view and the TRACE timing results are displayed in the Timing view. Your results might differ from those shown in Figure 23.

1. Click the **Reports** view tab at the bottom of the PlanAhead environment.

   If there is no Reports view available, select **Window > Reports**.

2. Double-click on the **MRP Report** and examine scrolling through the report.

3. Close the MRP Report by clicking the **X** button in the Workspace view tab.

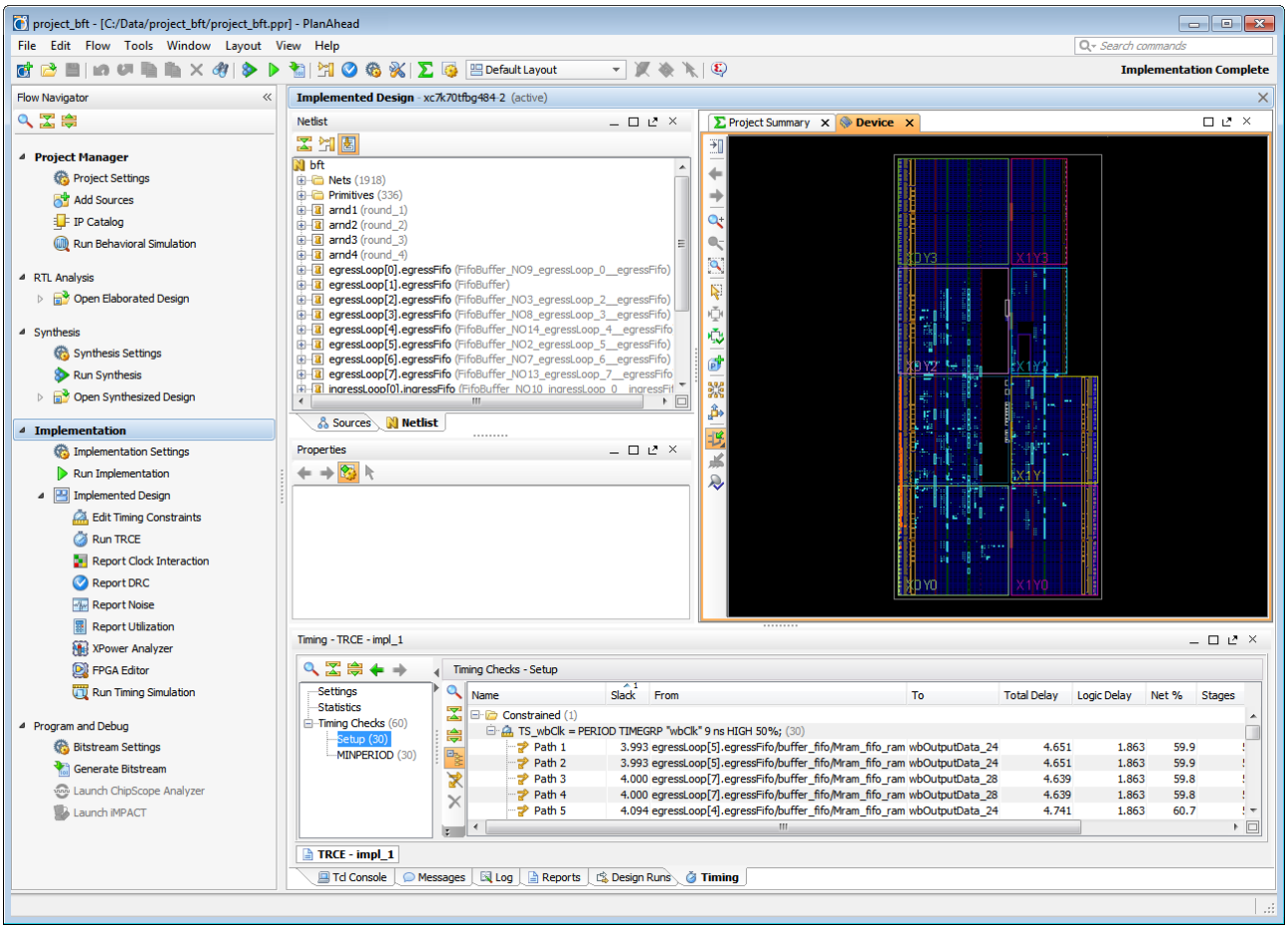

Figure 22: Opening the Implementation Results

4. In the Device view, click the **Hide/Show I/O Nets** button to turn on the I/O connectivity.
5. In the Device view, click the **Hide/Show I/O Nets** button to turn off the I/O connectivity.
6. Click the Timing view tab and, select the top timing path.

   The path is highlighted in the Device view and the logic objects on the path are selected in other views.

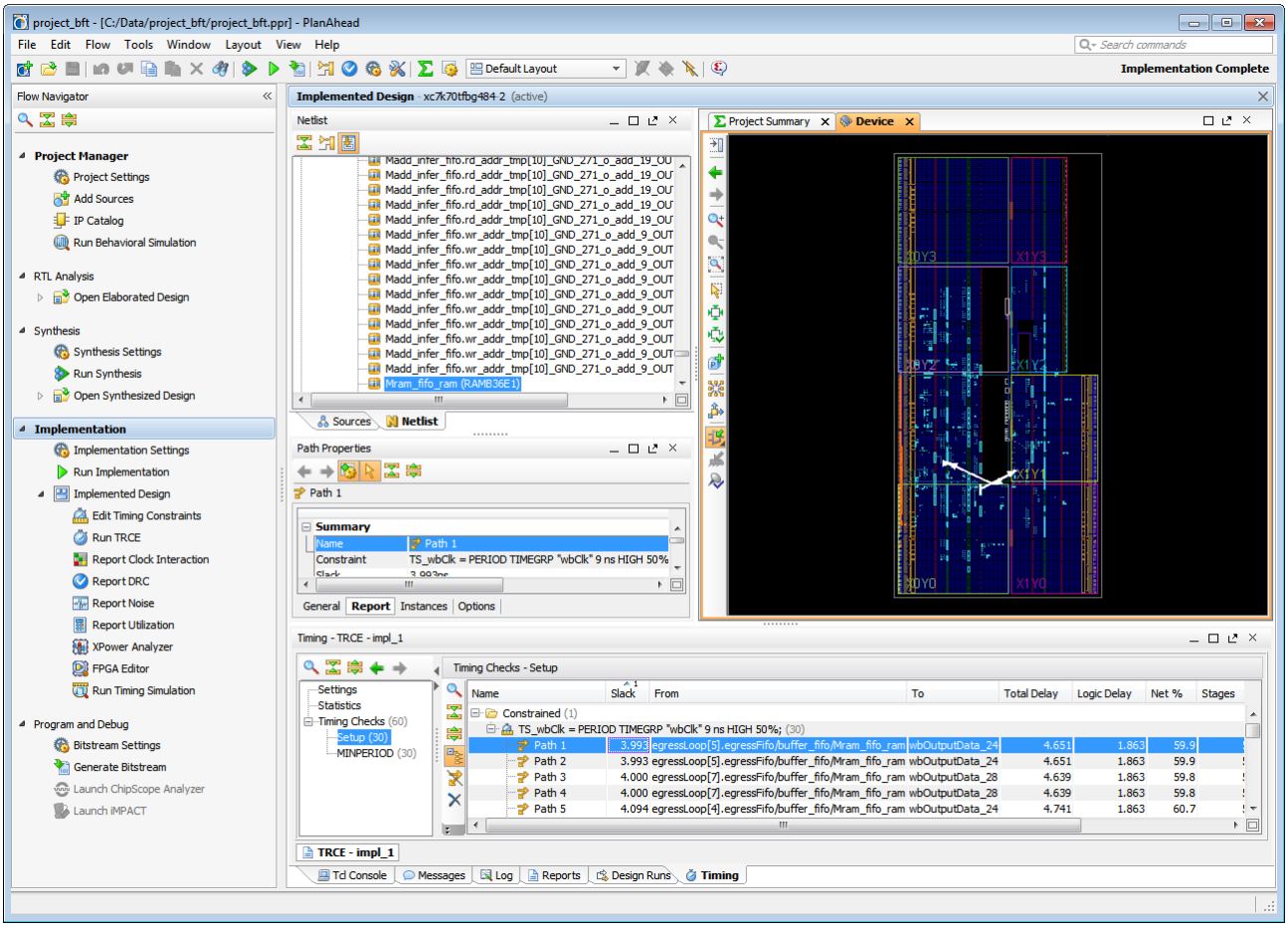

Figure 23: Highlighting Timing Paths

7. In the Path Properties view banner, click the **Maximize** button .

7. The Path Properties view displays in full screen.

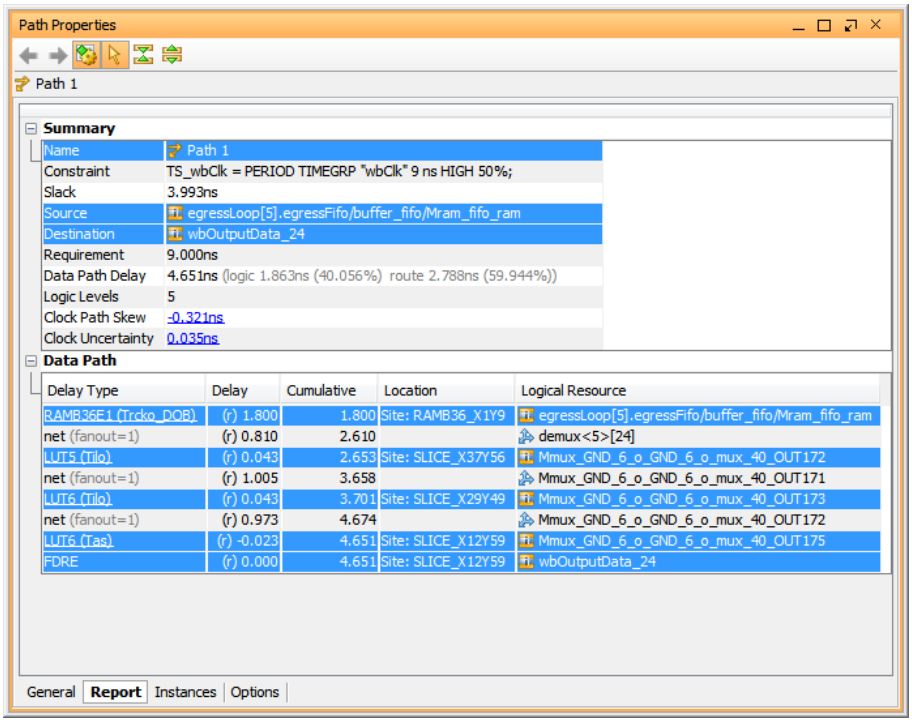

Figure 24: Viewing Path Properties

Notice the Path Properties report looks very similar to the TRACE report. Selecting any of the Logical Resources or Locations (e.g. SLICE_X36Y79) selects the logic object or site for viewing in Device or other view window.

8. Click the **Restore** button  in the Path Properties view banner to bring the view back to the original location.
9. In the Timing view, make sure the first path is still selected and click the **Schematic** button from the view toolbar  or select the command from the popup menu.

   The Schematic view opens.

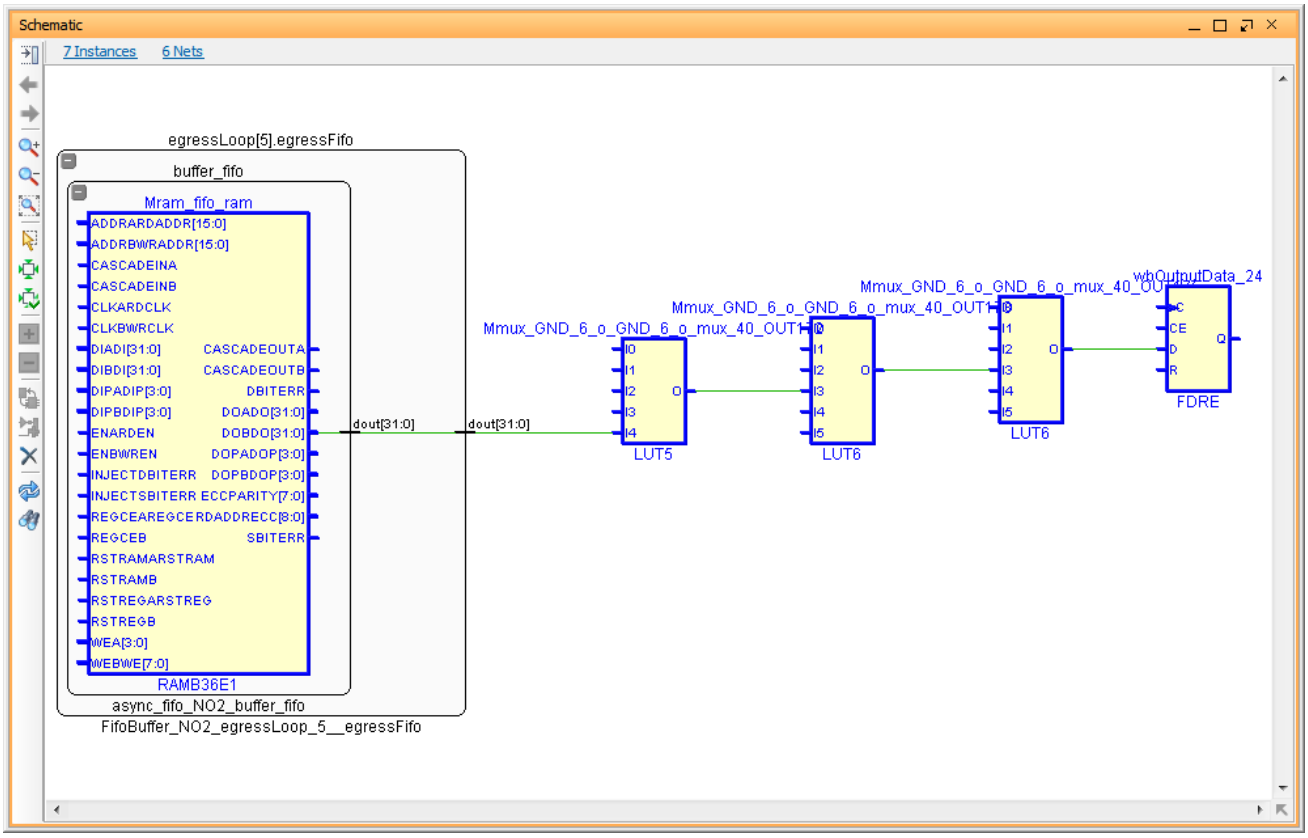

Figure 25: Viewing Timing Paths in the Schematic

Notice that the schematic displays the logic objects on the selected paths as well as the logical hierarchy. This helps identify logic modules for floorplanning. It also displays links to find the Nets and Instances displayed in the current view.

TIP: *The PlanAhead tool also includes a design analysis and floorplanning environment. This environment is covered in the Design Analysis and Floorplanning Tutorial: PlanAhead Design Tool (UG676). You can use the analysis features to explore the design or the implementation results. You can apply constraints aimed at better and more consistent results.*

10. **Close** the Schematic view.
11. Experiment with the various analysis features under Implemented Design in the Flow Navigator.

Step 7: Creating the Bitstream File

1. Click Bitstream Settings in the Flow Navigator.

   The Bitgen Project Settings open.

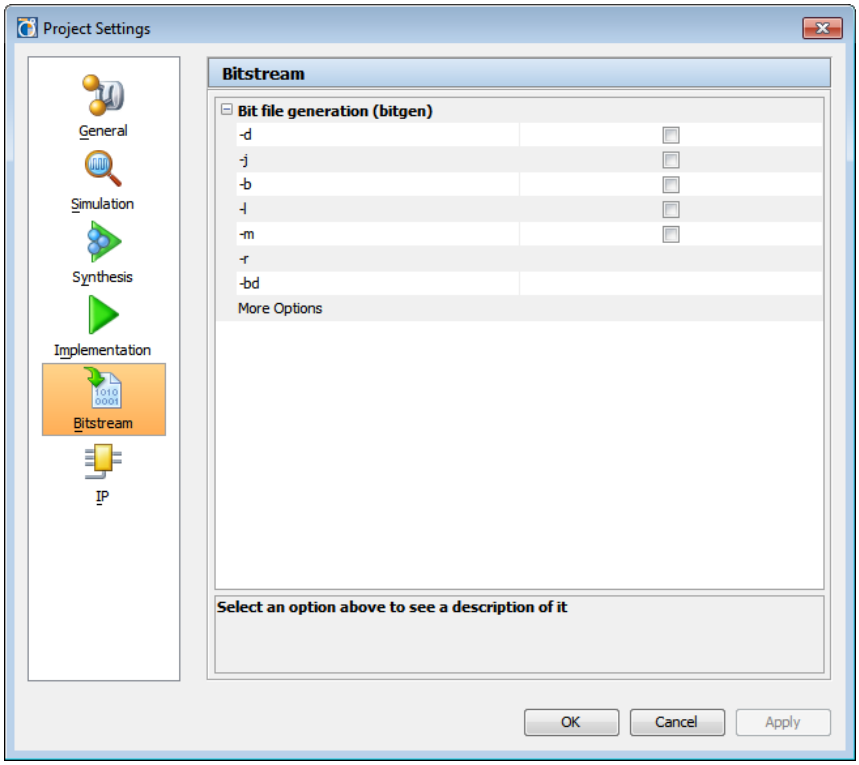

Figure 26: Bitstream Settings

2. Select **Cancel**.
3. Click **Generate Bitstream** in the Flow Navigator.

   The Running Bitgen progress bar opens. When the Bitstream is generated, a dialog box opens to inform you that the bitstream was successfully generated.

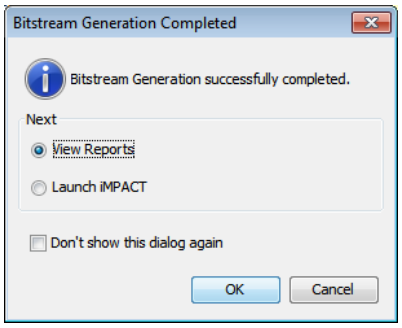

Figure 27: Bitstream Generated

4. Click the **OK** button to dismiss the dialog box and open the Reports view.
5. In the Flow Navigator, notice that you can launch ChipScope Analyzer and the iMPACT programming tool after a bitstream file is generated.

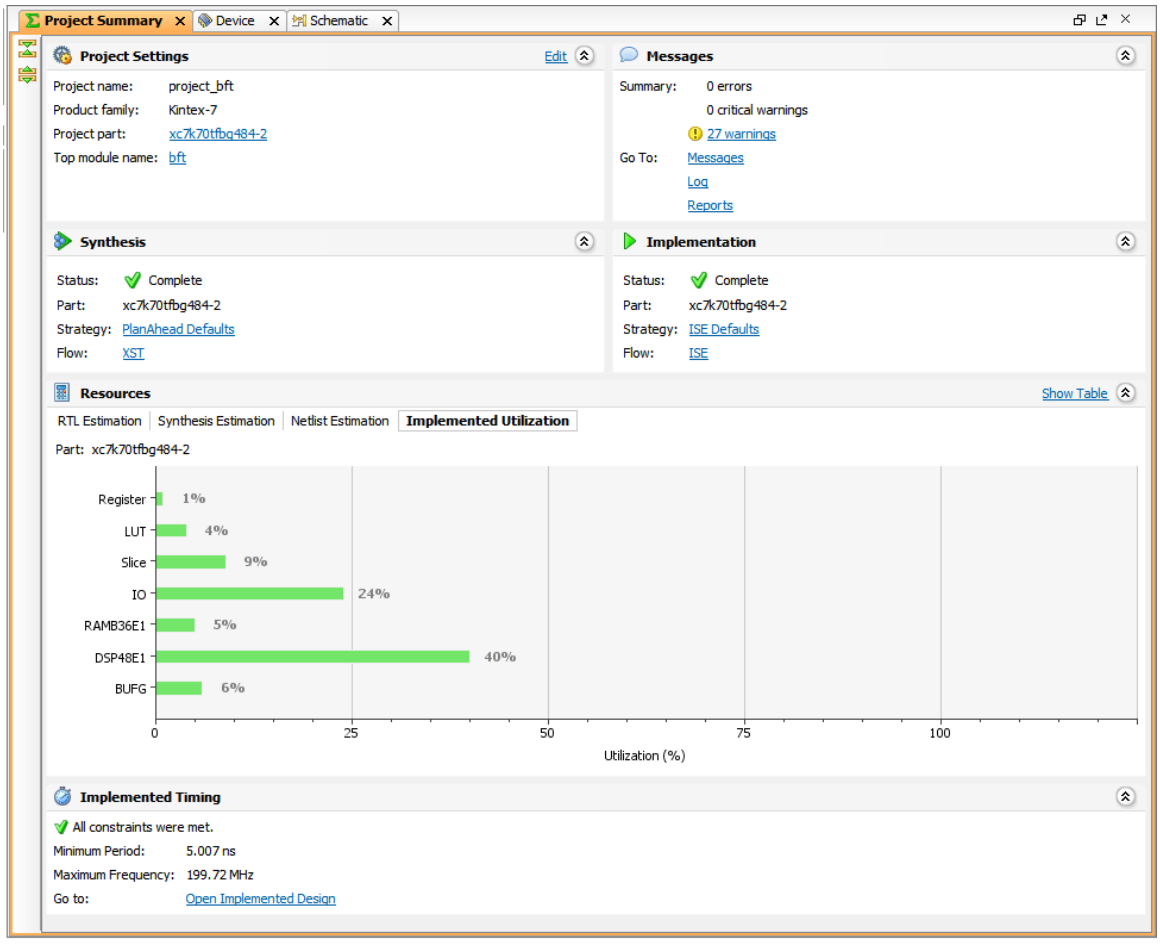

Figure 28: Project Summary of Implemented Design

Reviewing the Project Summary for the Implemented Design

1. Select the **Project Summary** tab, and review the information presented.
2. Close the PlanAhead tool by selecting **File > Exit**, click **Yes** to save, and **OK**.

Conclusion

In this tutorial, you:

- Used a small PlanAhead RTL project to step quickly through the basic PlanAhead design flow, starting by creating an RTL project, and exploring RTL sources in the Text Editor.
- Reviewed the simulation options and launched ISim.
- Reviewed the various synthesis run options, ran synthesis.
- Imported the results by opening the synthesized design.
- Explored implementation options
- Ran implementation.
- Monitored run results and viewed command report files.
- Imported run results, and analyzed a timing path.
- Created a bitstream file.