

# Kria SOM Carrier Card

## *Design Guide*

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## Introduction

The purpose of this design guide is to support hardware, system, and firmware engineers implementing a product using either an AMD Kria™ K26 SOM or K24 SOM. The guide outlines electrical, mechanical, firmware, and power-on configuration design considerations that must be addressed as part of designing an AMD SOM compatible carrier card. The document is not intended to be self-contained, meaning that there are references to other AMD product documentation to help the reader find more detailed technical information available in corresponding technical reference manuals, software design guides, and thermal design guides. The Kria K26 and K24 are designed to be mechanical and electrically compatible to allow scalability between the two SOMs.

# Electrical Design Considerations

This chapter describes the electrical interface details needed to design your carrier card to mate with the AMD Kria™ SOMs. The electrical interface design guidelines include the SOM connector details and signal names, signal routing guidelines, and power supply design.

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## SOM Connector Overview



**TIP:** Connector pinout information is available in the *Electrical Specifications* sections of the following data sheets:

- [Kria K26 SOM Data Sheet \(DS987\)](#)
- [Kria K24 SOM Data Sheet \(DS985\)](#)

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The connectors provide support for following interfaces.

- Control and status signals
- Multiplexed I/O (MIO) bank
- PS-GTR high-speed serial transceiver signals
- High-performance I/O (HPIO) bank signals
- High-density I/O (HDIO) bank signals
- GTH high-speed serial transceiver signals (K26 only)
- Power system

**Note:** The [ADM6-60-01.5-L-4-2-A](#) connector is referenced throughout this document. However, the Samtec REF-226081 is an alternative connector. Contact your Samtec distributor for more information.

### K26 SOM

The K26 SOM uses two 240-pin connectors to provide electrical connectivity between the SOM and the carrier card. These two connectors are referred to as SOM240\_1 and SOM240\_2. The SOM240\_1 and SOM240\_2 connector pinouts are available in the *Electrical Specifications* section of the [Kria K26 SOM Data Sheet \(DS987\)](#).

The SOM240\_1 and SOM240\_2 connectors use the Samtec 0.635 mm AcceleRate HD high-density 4-row, 60 position connector set. The part number for the socket ([ADF6-60-03.5-L-4-2-A](#)) is used on the bottom side of the SOM. The part number for the terminal ([ADM6-60-01.5-L-4-2-A](#)) is for use on the carrier card.

## K24 SOM

The K24 SOM uses one 240-pin connector and one 40-pin connector to provide electrical connectivity between the SOM and the carrier card. These two connectors are referred to as SOM240\_1 and SOM40. The SOM240\_1 connector is backward compatible with the SOM240\_1 connector on the K26 SOM. The SOM SOM240\_1 and SOM40 connector pinouts are available in the *Electrical Specifications* section of the *Kria K24 SOM Data Sheet* ([DS985](#)).

The SOM240\_1 connector uses the Samtec 0.635 mm AcceleRate (R) HD high-density 4-row, 60 position connector set. The part number for the socket ([ADF6-60-03.5-L-4-2-A](#)) is used on the bottom side of the SOM. The part number for the terminal ([ADM6-60-01.5-L-4-2-A](#)) is for use on the carrier card. The SOM40 connector uses the Samtec 0.635 mm AcceleRate (R) HD high-density 4-row, 10 position connector set. The part number for the socket ([ADF6-10-03.5-L-4-2-A](#)) is used on the bottom side of the SOM. The part number for the terminal ([ADM6-10-01.5-L-4-2-A](#)) is for use on the carrier card.

## Scalability Across Kria SOMs

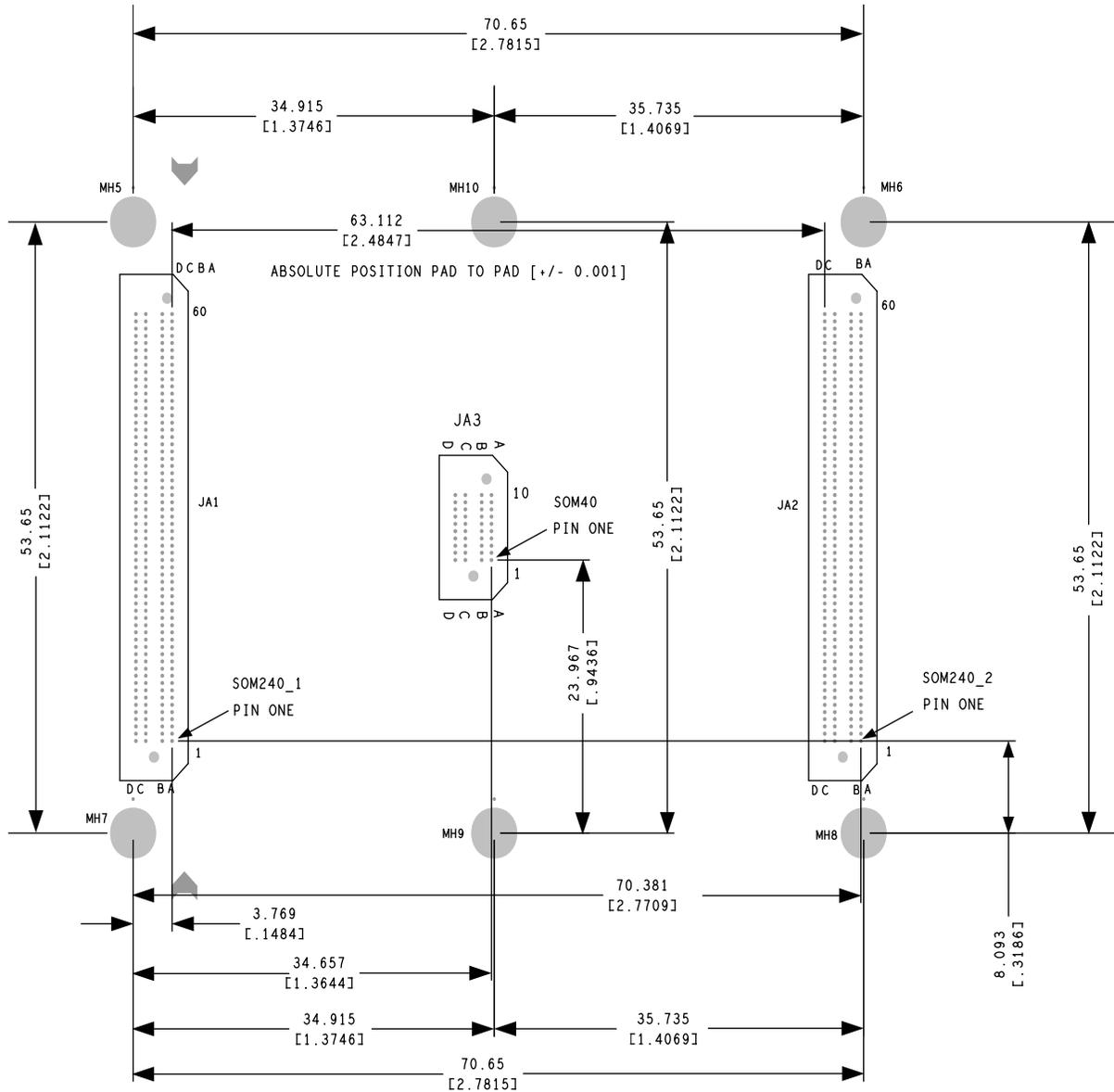
Kria SOMs are designed to support user scalability between the both the K26 and K24 SOMs. This is achieved by having a shared physical connector and corresponding electrical pinout for a common set of physical I/O, power rails, and interface capabilities on the SOM240\_1 connector. The scalability between the additional I/O of K26 vs. K24 is accomplished through the secondary connectors SOM40 on K24 and SOM240\_2 on K26. A given carrier card can accommodate both K24 and K26 by using the mechanical keep outs and connector alignments outlined in the following image and by planning for their extended I/O to be mapped to the extended I/O connectors of the corresponding SOM.

- **som\_240\_1:** Common connector to both K26 and K24
  - Control and status signals
  - MIO signals
  - PS-GTR
  - Subset of HPIO
  - Subset of HDIO
  - SOM power
- **som\_240\_2:** K26 only
  - Additional HPIO
  - Additional HDIO
  - GTH transceiver

- som\_40: K24 only
  - Additional HPIO
  - Additional HDIO

A DXF of the mechanical connector overlay file is available at [Kria SOM Carrier Connector Compatibility Overlay \(XTP785\)](#).

Figure 1: Kria SOM Connector Overlay



X28741-101523

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## Supported I/O Standards

Kria SOMs support all I/O standards supported by the respective bank that a signal is connected to with the exception of I/O standards that require a reference voltage ( $V_{REF}$ ). For more information, refer to the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

During power-up and configuration, internal pull-up resistors are disabled and each SelectIO™ pin is set to 3-state.

The K26 SOM is built with the XCK26-SFVC784-2LV device; which has a -2 speed grade and is an LV device (operates at  $V_{CCINT} = 0.72V$ ).

The K24 SOM is built with the XCK24-UBVA530-2LV device; which has a -2 speed grade and is an LV device (operates at  $V_{CCINT} = 0.72V$ ).

Consult the corresponding I/O speed tables in the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* ([DS925](#)) for the switching characteristics. I-grade SOM devices can differ from the standard MPSoC. Exceptions overriding the standard definition are listed in each SOM data sheet. Refer to the K26I SOM I-grade specification in the *Kria K26 SOM Data Sheet* ([DS987](#)) or the K24I SOM industrial grade specification in the *Kria K24 SOM Data Sheet* ([DS985](#)).

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## Signal Routing Guidelines

This section provides signal routing guidelines and required PCB layout constraints for all interfaces provided on the SOM.

**Note:** Consult the *UltraScale Architecture PCB Design User Guide* ([UG583](#)) for detailed information.

### MIO Signals

- Route all MIO signals MIO[77:26] as single-ended 50Ω traces.
- The maximum data rate supported on MIO signals is 250 Mb/s.
- Implement length matching as required by the interface used on individual MIO signal groups defined by the application MIO configuration.
- All MIO signals must be 1.8V compatible.

## HDIO Signals

- Route all HDIO signals as single-ended 50 $\Omega$  traces.
- The maximum data rate supported on HDIO signals is 250 Mb/s. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925)* for more information on HDIO signals.
- Implement length matching as required by the application PL-based interface mapped to the HDIO signal groups.

## HPIO Signals

HPIO signals can be implemented as high-speed differential signaling such as MIPI interfaces or other application specific interfaces.

- HPIO P/N pairs should be routed as standard 50 $\Omega$  single-ended traces.
- The maximum data rate supported on HPIO signals is 2.5 Gb/s. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925)* for more information on HPIO signals.
- Implement length matching as required by the interface used on individual HPIO signal groups.
- Match P and N signals within an HPIO differential pair to within  $\pm 0.5$  mils of each other.
- If using MIPI differential signals, length match the MIPI interface HPIO signal groups (pair to pair) within  $\pm 50$  mils.
- MIPI differential signals to all other signal spacing should be 2.5 times the distance between signal to nearest GND plane.
- Match other application-specific HPIO use cases per the HPIO signal group interface requirement.

## PS-GTR Transceivers

PS-GTR transceivers support a maximum transfer rate of 6 Gb/s over each lane.

- To minimize the impedance discontinuity at the SOM connector interface, route the PS-GTR signals using a 90 $\Omega$  differential impedance.
- Match P and N differential signals to within  $\pm 0.5$  mils of each other.
- Route PS-GTR signals in internal routing layers as a stripline structure.
- Route PS-GTR signals with a maximum of two via transitions. Ensure adequate ground return vias are placed next to the signal vias to minimize crosstalk.
- Route PS-GTR signals to have a maximum via stub length of less than 50 mils. It is a good design practice to minimize the stub length to avoid reflections.

- PS-GTR differential signals to all other signal spacing should be four times the distance between the signal to the nearest GND plane.
- For design flexibility, no transceiver capacitors are added to the data lanes on the PS-GTR transceivers.
- For more information on proper decoupling and interface standards, see the *PCB Guidelines for the PS Interface in the Zynq UltraScale+ MPSoC* chapter in the *UltraScale Architecture PCB Design User Guide* ([UG583](#)).

## GTH Transceivers (K26 SOM only)

Refer to the *Vivado Device Model* section of the *Kria K26 SOM Data Sheet* ([DS987](#)) for the GTH transceiver maximum transfer rate.

- To minimize the impedance discontinuity at the SOM connector interface, route the GTH signals using a 90 $\Omega$  differential impedance.
- Match P and N differential signals to within  $\pm 0.5$  mils of each other.
- Route GTH signals in internal routing layers as a stripline structure.
- Route GTH signals with a maximum of two via transitions. Ensure adequate ground return vias are placed next to the signal vias to minimize crosstalk.
- Route GTH signals to have a maximum via stub length of less than 24 mils. It is a good design practice to minimize the stub length to avoid reflections.
- GTH differential signals to all other signal spacing should be five times the distance between the signal to the nearest GND plane.
- For design flexibility, no transceiver capacitors are added to the data lanes on the GTH transceivers.
- For more information on proper decoupling and interface standards, see the *PCB Design Checklist* chapter in the *UltraScale Architecture GTH Transceivers User Guide* ([UG576](#)).

## Transceiver Reference Clocks

Both the PS-GTR and PL-GTH transceivers differential clock signals (REFCLKs) must meet following signal integrity requirements.

- The target differential impedance of 100 $\Omega$ .
- Match P and N differential signals to within  $\pm 0.5$  mils of each other.
- REFCLK to all other signal spacing should be five times the distance between the signal to the nearest GND plane.

The Kria K26 SOM includes 0.01  $\mu$ F AC coupling capacitors on the MGTREFCLKs to minimize noise and reduce power consumption.

## I/O Constraints Definition

### *SOM I/O Timing Model*

The MPSoC package delay and SOM trace length information are defined by the board-to-board connector pin name and associated MPSoC pin function net name. See the trace delay file for the SOM:

- *Kria K26 SOM Trace Delay File* ([XTP688](#))
- *Kria K24 SOM Trace Delay File* ([XTP779](#))

When creating an I/O timing model, you should include the AMD Zynq™ UltraScale+™ MPSoC package and SOM PCB signal delays for all MIO, HDIO, and HPIO related interfaces. As the carrier card designer, you must include the trace length definitions associated with your implementation.

The Vivado device model captures the MPSoC-related timing model information. When designing a carrier card, you need to include the physical trace length of the MPSoC to board-to-board connector on the SOM along with the board-to-board connector to peripheral device on your carrier card.



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**TIP:** The SOM device and package delay is available in the AMD Vivado™ tools.

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### *SOM I/O Drive Strength Definition*

For up to eight inches of trace length on the carrier card, the recommendation is to use a 4 mA drive strength and a slow slew rate for all MIO and HDIO signals. When trace lengths on the carrier card are longer than eight inches, signal integrity simulations might be necessary to select the correct drive strength and proper termination.



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**RECOMMENDED:** For MIO signals that are local to the SOM on MIO bank 500 and part of MIO bank 501, the recommendation is to use a 4 mA drive strength and slow slew rate.

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For I/O modeling, including drive strength settings, the Zynq UltraScale+ MPSoC [IBIS models](#) can be downloaded from the AMD website.

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## SOM Configuration and Control Signals

This section outlines the configuration and control signals associated with the Zynq UltraScale+ MPSoC on the SOM.

### Power-on Reset (PS\_POR\_B) Signal

This is the Zynq UltraScale+ MPSoC power-on reset signal. In AMD documentation this signal is also described as PS\_POR\_B. The PS\_POR\_B signal is an active-Low signal that must be asserted during the SOM power-up sequence. On the SOM, the PS\_POR\_B signal is connected to the PS\_POR\_L SOM240 connector signal.

### System Reset (PS\_SRST\_B) Signal

This system reset is primarily used for debug activities and is functionally equivalent to POR\_B except for clearing a subset of PS power-on and error registers. See the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)) for more information.

### BOOT\_MODE Signals

The BOOT\_MODE pins define the physical device that the Zynq UltraScale+ MPSoC uses to read the boot firmware. The boot firmware is prepackaged as a `boot.bin`, which is a consolidated boot firmware binary constructed using the AMD Bootgen tool outlined in the *Bootgen User Guide* ([UG1283](#)).

**Note:** AMD documentation uses PS\_MODE and BOOT\_MODE interchangeably.

The SOM includes two non-volatile storage devices: QSPI and eMMC. The BOOT\_MODE strapping defines the primary boot device. Alternative boot devices can be designed on your carrier card via MIO banks 501 and 502. The BOOT\_MODE memory device selection resistor strapping is defined in the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)).

### JTAG Port Interfaces

The JTAG interface uses a serial configuration mode, popular for prototyping and board test. The four-pin JTAG interface consisting of pins TMS, TDO, TDI, and TCK is included for debug purposes and recommended to be accessible through the carrier card, regardless of boot mode selected. For more information, see the JTAG Interface section in *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)).

### PS\_ERROR\_OUT Signal, PS\_ERROR\_STATUS Commands

PS\_ERROR\_OUT is asserted when there is an accidental loss of power, a hardware error, or an exception in the PMU. For secure scenarios where device status is disabled from external visibility, there are PMU control registers to mask PS\_ERROR\_OUT. PS\_ERROR\_OUT is sourced from a 1.8V power domain. For more information, see the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)).

PS\_ERROR\_STATUS indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status. For secure scenarios where device status is disabled from external visibility, there are PMU control registers to mask PS\_ERROR\_STATUS. PS\_ERROR\_STATUS is sourced from a 1.8V power domain. For more information, see the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)).

### Power Management Unit (PMU)

The PMU processor of the Zynq UltraScale+ MPSoC has access to a subset of the I/O in bank 501 that should be given special consideration during the implementation of power-down and power control functionality in the SOM and carrier card design. The PMU application can be customized by the carrier card designer. However, the AMD PMU reference implementation uses the following pin mappings:

- MIO31 is a SOM/CC pin that can be mapped to a PMU GPI pin. PMU GPI pin can be used to implement functionality like a *HW Requested Shutdown*.
- MIO32 is a PMU GPO reserved signal.
- MIO33 is the PMU output signal reserved for PL power control. This *SW Controlled Power Down for PL* is only available on the K24.
- MIO34 is the PMU output signal reserved for LPD/FPD (PS) power control, this *SW Controlled Power Down* is implemented for both the K26 and K24 SOMs.
- MIO35 is a SOM/CC pin that can be mapped to a PMU GPO pin. A PMU GPO pin can be used for PMU based functionality, like external POR\_B control or external watchdog monitor.

### Sideband Signals

The sideband signals consist of power, processor, and configuration signals.  $V_{CCO}$  for sideband signals is 1.80V.

- **JTAG:** The JTAG signals JTAG\_TCK\_C2M, JTAG\_TMS\_C2M, JTAG\_TDI\_C2M, and JTAG\_TDO\_M2C connect to the SOM Zynq UltraScale+ MPSoC JTAG port.
- **PS\_REF\_CLK:** The PS\_REF\_CLK input is connected to a 33.33 MHz oscillator.
- **PS\_PAD\_I/O:** The PS RTC inputs are connected to a 32.768 kHz crystal.
- **I2C:** The I2C signals I2C\_SCK and I2C\_SDA connect to an I2C master on MIO bank 500 of the SOM Zynq UltraScale+ MPSoC. The I2C I/O standard is 1.8V.
- **PS\_MODE[3:0]:** The connector PS\_MODE[3:0] pins connect to the SOM Zynq UltraScale+ MPSoC PS\_MODE pins. All mode pins are pulled High to 1.8V through a resistor on the SOM. The carrier card boot mode is required to set the PS\_MODE pins to a valid boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)). To configure a PS\_MODE pin to a logic 1, the pin must be left floating, to configure a logic 0, the PS\_MODE pin must be connected to GND with a 0Ω resistor.

- **PS\_POR\_L:** During power up, a voltage monitor keeps PS\_POR\_L asserted (Low) until all SOM power rails are stabilized. Afterward, PS\_POR\_L is released and the boot process starts. A carrier card can use PS\_POR\_L to reset any on-board devices. The carrier card can also force PS\_POR\_L Low to extend the reset during power on. At any time, the carrier card can use PS\_POR\_L to reset the system or extend the boot process. A proper shutdown sequence is recommended before resetting the system. The PS\_POR\_L signal drives the PS\_POR\_B signal on Zynq UltraScale+ MPSoC. This signal is pulled up to 1.8V through a 4.70 K $\Omega$  resistor on the SOM.
- **PS\_SRST\_C2M\_L:** The PS\_SRST\_C2M\_L pin connects to PS\_SRST\_B signal on the SOM Zynq UltraScale+ MPSoC. PS\_SRST\_B input signal to the Zynq UltraScale+ MPSoC is the system reset signal, and it is commonly used during debug. PS\_SRST\_C2M\_L is pulled High to 1.8V on the SOM.

## Power Management Signals

- **PWROFF\_C2M\_L:**
  - PWROFF\_C2M\_L is an active-Low signal to power down the SOM and pulled High to the +5V SOM input power rail.
  - When PWROFF\_C2M\_L is asserted, the SOM power regulators perform a full-power shutdown of the device following the correct regulator power-down sequence. This signal does not alert application software to the power shutdown.
  - Upon deassertion of PWROFF\_C2M\_L, the SOM power regulators initiate a power-on sequence.

**Note:** Asserting PWROFF\_C2M\_L does not perform a software shutdown or notify the system of the shutdown. The power regulators start to power down instantly. Use the MIO31\_PMU\_GPI pin and PMU functionality to initiate a software shutdown.

- **PWRGD\_LPD\_M2C:** PWRGD\_LPD\_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PS low-power domain (LPD) rails. PWRGD\_LPD\_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor LPD status.
- **PWRGD\_FPD\_M2C:** PWRGD\_FPD\_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PS full-power domain (FPD) rails. PWRGD\_FPD\_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor FPD status.

**Note:** The K26 SOM does not have split rails for LPD and FPD. PWRGD\_LPD\_M2C and PWRGD\_FPD\_M2C are tied together on the SOM.

- **PWRGD\_PL\_M2C:** PWRGD\_PL\_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PL power rails. PWRGD\_PL\_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor PL power status.

- **VCCOEN\_PS\_M2C:** VCCOEN\_PS\_M2C is an active-High push-pull output signal from the SOM power system to enable the PS  $V_{CCO}$  rails that are supplied by the carrier card. VCCOEV\_PS\_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal as an indication to turn power on for all PS peripherals.
- **VCCOEN\_PL\_M2C:** VCCOEN\_PL\_M2C is an active-High push-pull output signal from the SOM power system to enable the PL  $V_{CCO}$  rails that are supplied by the carrier card. VCCOEN\_PL\_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal as an indication to turn power on for all PL peripherals.

## SOM MIO Design Considerations

The Zynq UltraScale+ MPSoC on the SOM has a set of integrated, built-in interface IPs. These interface IPs are made available to external pins through multiplexed I/O (MIO) selection, which can be selected and customized for a carrier card design. The MIO interface configuration is set as part of the Vivado design project through the Vivado processor configuration wizard (PCW).

The design of the SOM carrier card must give special consideration to the MIO pins to ensure that the desired MIO peripherals are mappable to the physical pins defined by the electrical design of the carrier card. The SOM fixes the mapping of MIO bank 500 for SOM based peripherals and a subset of bank 501 for SOM power management signals. The remaining MIO pins are configurable for flexibility in the carrier card design. The full MIO peripheral IP mapping to physical pin mapping is defined in the *MIO Interfaces* table in *Zynq UltraScale+ Device Technical Reference Manual (UG1085)*. MIO mapping must comply with the Zynq UltraScale+ MPSoC design constraints and requirements.

### MIO Bank 500

The SOM fixed MIO configurations for bank 500 are outlined in the following table. This MIO configuration is defined by the physical SOM design and cannot be modified by carrier-card designers. It defines the MIO configuration for the SOM peripherals: QSPI, TPM SPI, LEDs, eMCC, and I2C configuration bus.

MIO #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Peripheral	QSPI						SPI1	GPIO0		SPI1			GPIO0	eMMC (SD0)										GPIO0	I2C1	
Pin Fct	sclk_out	miso_mo1	mo2	mo3	mosi_mi0	n_ss_out	sclk_out	LED_DS35	LED_DS36	n_ss_out	miso	mosi	FW_Upd	data[0]	data[1]	data[2]	data[3]	data[4]	data[5]	data[6]	data[7]	cmd_out	clk_out	eMMC_Rst	scl	sda

### MIO Bank 500 – Extensible I2C Bus

This MIO configuration must be considered fixed and pre-populated in the corresponding SOM Vivado board files. In SOM bank 500, predefined configuration of the PS I2C interface is made available to the carrier card via the I2C\_SCK and I2C\_SDA signals on the som\_240\_1 connector. If the carrier card does not need to extend this I2C bus, the carrier card should leave them as no connects. If the carrier card design extends this bus, they need to ensure they do not introduce an address conflict with the I2C devices on the SOM. The I2C devices are defined in the corresponding table of the *Kria K26 SOM Data Sheet (DS987)* and *Kria K24 SOM Data Sheet (DS985)*.

## MIO Bank 501 – PMU MIO Considerations

The Zynq UltraScale+ MPSoC platform management unit (PMU) processor has access to a subset of the MIO in bank 501 that are also available to the clock-capable I/O and should be given special consideration for the implementation of power-down and power control functionality of the SOM and carrier card design. The SOM power management reserved pins MIO32–34 and are identified in green. The K26 SOM only implements MIO34. The K24 SOM implements both MIO33 and MIO34.

There are also two pins related to optional PMU features made available in the SOM PMU reference implementation. They implement an external shutdown request and can control an external platform watchdog function. These MIO501 optional feature pins are shown in orange.

There are two PMU accessible pins that require special consideration in your CC design as they can be directly accessed by the PMU auxiliary processor.

- MIO31: PMU input pin
- MIO35: PMU output pin

These pins can also be mapped to the APU GPIO controllers if not used in any special PMU-based functionality.

## MIO Bank 501 – UART

**RECOMMENDED:** *The carrier card design should include a UART for board bring-up and initial debug. The AMD Kria boot firmware and PetaLinux BSP default the UART interface to MIO36 and MIO37. It is recommended that carrier card designs use this same mapping to be able to use the AMD provided software references.*

The orange color coding in the following table point out special design consideration pins inclusive of the UART.

MIO #	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
Peripheral						PMU_GPI	PMU_GPO	PMU_GPO	PMU_GPO	PMU_GPO	UART1															
Pin Fct						SHUTDOWN	FPD_Pwr_En	PL_Pwr_EN	PS_Pwr_En	WD_OUT	txd	rxd														

## MIO Bank 502

MIO bank 502 has no pin reservations relative to the carrier card design, beyond those defined in *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#)).

## SOM Power

Your carrier card should provide:

- The SOM main power supply (+5V power rail).
- The  $V_{CCO}$  power rails for the programmable logic (PL) HPIO and HDIO banks on the SOM.
- Optionally, the carrier card can supply an external battery power to the  $V_{CC\_BATT}$  pin for real-time clock (RTC) battery backup power.

## SOM Connector Power Pins

The following data sheets contain the power rail requirements for the connector power pins on each SOM.

- *Kria K26 SOM Data Sheet* ([DS987](#))
- *Kria K24 SOM Data Sheet* ([DS985](#))

For the selected I/O type, the supply voltage tolerance at the SOM connector must be within +3%/-2%. For example:

- If an HPIO bank is configured for the LVDS (1.8V) standard, the  $V_{CCO}$  at the SOM connector pin must be within 1.764V-1.854V.
- If an HDIO bank is configured for the LVDS\_25 standard, the  $V_{CCO}$  at the SOM connector pin must be within 2.450V-2.575V.

## Power Management

The SOM is based on a custom MPSoC. Designing the SOM power follows the same design practices. Signaling is provided to help with this, and it is recommended that you split the power system on your carrier card into three power domains:

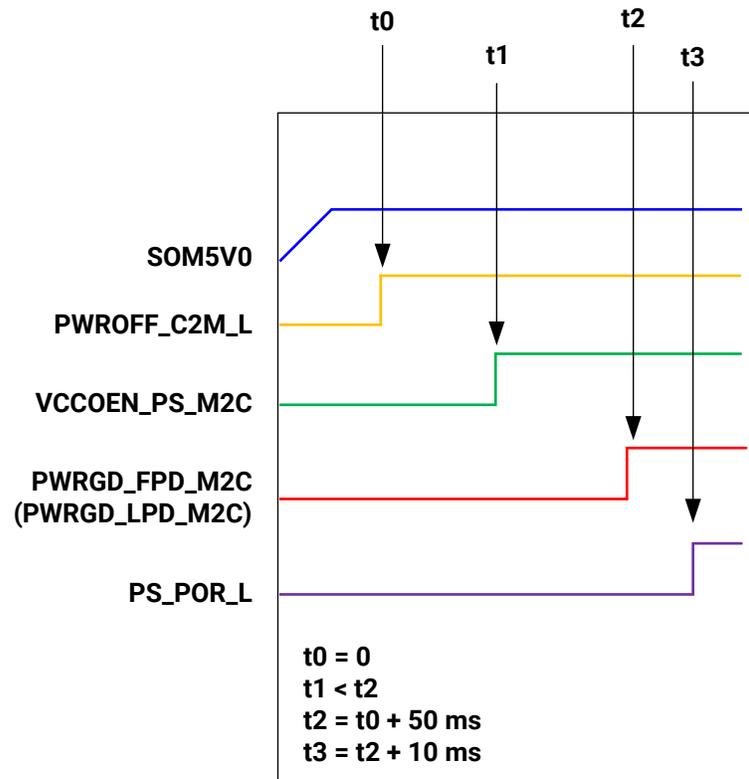
- **Always On Power Domain:** The +5 V main power and auxiliary power support infrastructure components such as the power management and telemetry circuits, reset circuits, and clocking circuits.
- **PS Power Domain:** The power rails that support the peripherals connected to the PS MIO and PS-GTR signals.
- **PL Power Domain:** The power rails that support the peripherals connected to the PL HDIO and HPIO signals and the  $V_{CCO}$  rails.

## Power Sequencing

The carrier card power management circuit for your application is required to implement a defined sequence to ensure proper initialization of the SOM. Your carrier card supplies the +5V SOM power rail ( $V_{CC\_SOM}$ ). The following diagrams outline the interactions between the carrier card and the SOM at power up, and must be followed for proper operation of the SOM.

### PS Power Up Behavior

Figure 2: PS Power Up Sequence Diagram



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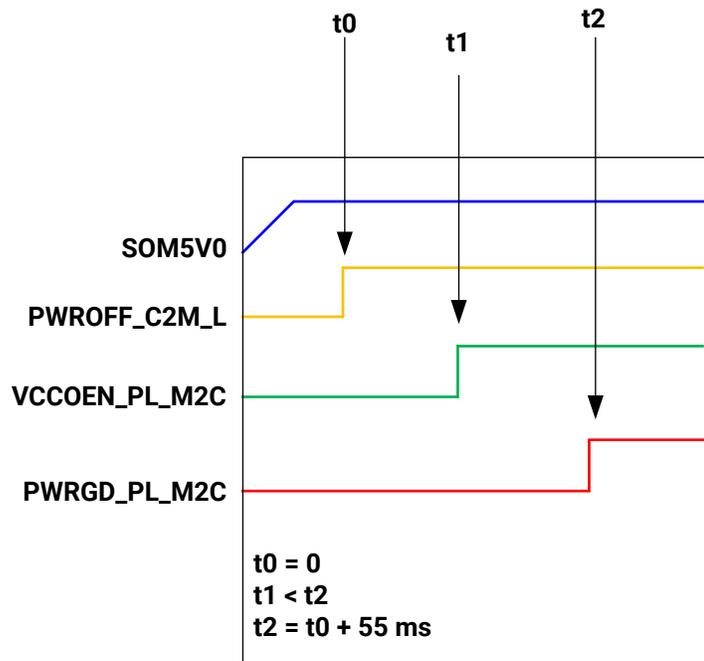
1. Carrier-provided SOM5V0 is initialized and stabilized.
2. Carrier deasserts PWROFF\_C2M\_L ( $t_0$ ).
3. SOM PS core and I/O power initialized in the correct sequence (parallel to PL sequence).
4. SOM PS power is stabilized.
  - a. Sequencer asserts VCCOEN\_PS\_M2C ( $t_1$ ).
  - b. PS power stabilization occurs within 50 ms.
  - c. Carrier enables all supplies related to PS MIO peripherals.

**Note:**  $V_{CCOEN\_PS\_M2C}$  is required to be asserted by the power sequencer prior to allowing the power-on sequence to continue, that is the release of PS\_POR\_L.

5. SOM full-power domain (FPD) and low-power domain (LPD) sequencing is initialized.
6. SOM FPD and LPD power is stabilized.
  - a. Sequencer asserts PWRGD\_FPD\_M2C and PWRGD\_LPD\_M2C ( $t_2$ ).
  - b. PWRGD\_FPD\_M2C and PWRGD\_LPD\_M2C are tied together on the K26 SOM.
  - c. Asserts 50 ms after PWROFF\_C2M\_L is deasserted.
7. SOM releases PS reset.
  - a. Sequencer releases PS\_POR\_L1 ( $t_3$ ).
  - b. This occurs 10 ms after PWRGD\_FPD\_M2C and PWRGD\_LPD\_M2C asserts.
  - c. Carrier can now control the SOM power on reset (POR\_B) signaling to hold off boot for carrier related delays, or coordination.
8. Carrier assertion of PS\_POR\_L starts a hardware reset of the MPSoC. This leaves the power supplies fully sequenced and available for immediate use by the SOM upon PS\_POR\_L release, without needing to sequence the MPSoC a second time.

## PL Power Up Behavior

Figure 3: PL Power Up Sequence Diagram



X29305-041924

1. Carrier-provided SOM5V0 is initialized and stabilized
2. Carrier deasserts PWROFF\_C2M\_L (t0)
3. All SOM PL power initialized in the correct sequence. Parallel to PS sequence.
4. SOM PL core and VCU power stabilized:
  - a. Sequencer asserts VCCOEN\_PL\_M2C (t1)
  - b. PL power stabilization occurs within 55 ms
  - c. Carrier enables all VCCO supplies related to PL peripherals
5. All remaining SOM power stabilized:
  - a. Sequencer asserts PWRGD\_PL\_M2C (t2)
  - b. Asserts 55 ms after PWROFF\_C2M\_L deassertion

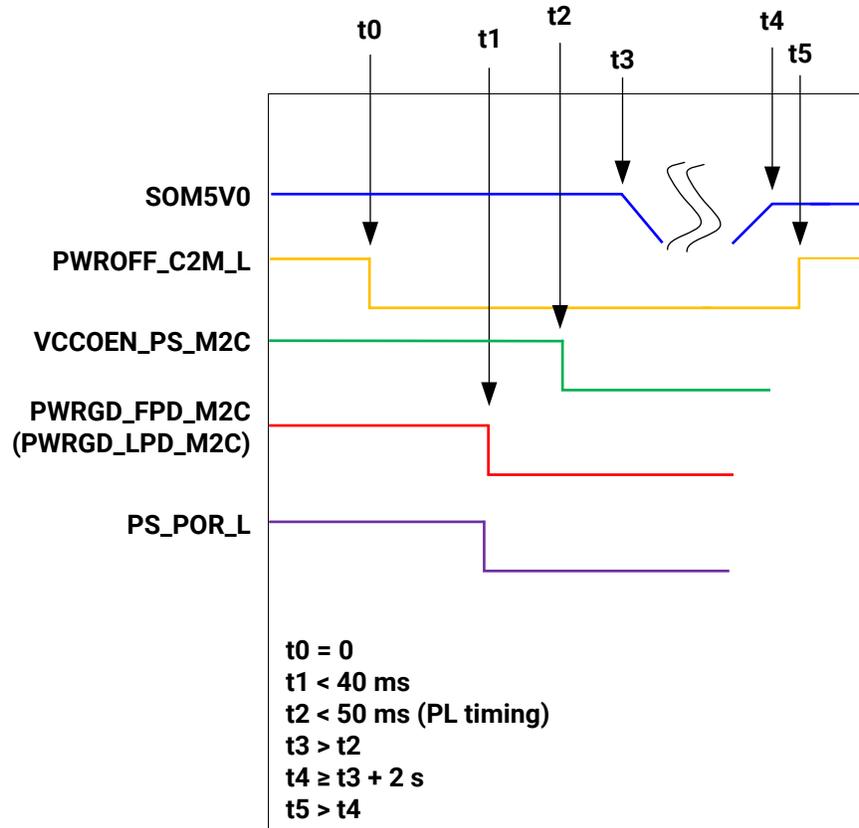
### ***SOM Power Off Sequence***

AMD recommends implementing an intentional shutdown sequence to allow software running on the platform to cleanly shutdown file systems and interface transactions. Both software and hardware requested shutdown features noted for the platform management unit (PMU) are available. Both require you to account for these and enable them in their production MPSoC-PMU firmware configuration.

When no consideration is given to the PS, nor operating system, asserting PWROFF\_C2M\_L can be used to immediately begin a power down at the power supply level. The following sequence assumes that the SOM 5.0 V power supply is sustained during the power down sequence. With that assumption, the power sequencer devices should remove the power rails in the correct order without waiting for the operating system to cleanly shutdown.

## PS Power Down

Figure 4: PS Power Down Sequence Diagram

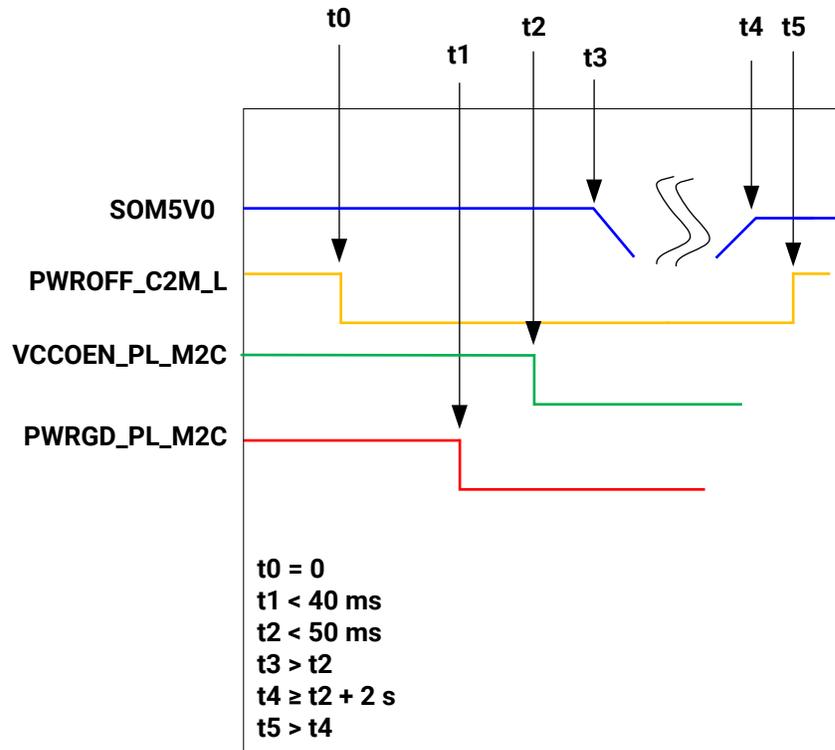


X29304-041924

- Carrier asserts PWROFF\_C2M\_L ( $t_0$ ). Power sequencers immediately begin rolling back all power solutions.
- Upon first power supply not meeting the required stabilization requirements, all status signals and request signaling from the SOM are deasserted ( $t_1$ ).
- At VCCOEN\_PS\_M2C ( $t_2$ ) deassertion carrier turn off power to  $V_{CCO}$  supplies.
- Carrier remove SOM5V0 ( $t_3$ )
  - SOM5V0 does not have to be removed, however, the discharge of related power supplies and power up rules must be observed before PWROFF\_C2M\_L ( $t_5$ ) can be deasserted.
  - ( $t_4$ ) is observed to be the same point as ( $t_0$ ) in the power-up sequence.
- Rails discharge for up to 2 seconds ( $t_5$ ).

## PL Power Down

Figure 5: PL Power Down Sequence Diagram



X29306-041924

- Carrier asserts PWROFF\_C2M\_L (t0). Power sequencers immediately begin rolling back all power solutions.
- Upon first power supply not meeting the required stabilization requirements, all status signals and request signaling from the SOM is deasserted (t1)
- At VCCOEN\_PL\_M2C (t2) deassertion carrier turns off power to the V<sub>CCO</sub> supplies.
- Carrier remove SOM5V0 (t3).
  - SOM5V0 does not have to be removed. However, the discharge of related power supplies and power up rules must be observed before PWROFF\_C2M\_L (t5) can be deasserted.
  - (t4) is observed to be the same point as (t0) in the power up sequence.
- Rails discharge for up to 2 seconds (t5).

**★ IMPORTANT!** It is a good design practice to delay the re-release of PWROFF\_C2M\_L for more than 2 seconds. This is because full discharge of the SOM rails depends on many factors including device temperature, temperature grade, and the performance/power draw of the software and firmware being run on the SOM at the time of PWROFF\_C2M\_L assertion. Failure to provide enough time for the system to discharge rails can provide a locked state for the power sequencer. Rails powering up under the incorrect order can cause the sequencer to halt power-up sequence for SOM protection. The only resolution to this locked state is a complete power down of all rails, including the main SOM 5.0 V input.

## Power Telemetry

**✔ RECOMMENDED:** Your carrier card should employ a current sensing device to monitor the input current on the  $V_{CC\_SOM}$  supply rail that is powering the SOM. AMD carrier cards add this current sensing device to the PS I2C bus to minimize I/O.

## Voltage Rail Monitoring

A subset of the SOM rails can be monitored using the system monitor (SYSMON) available on the Zynq UltraScale+ MPSoC. For more information on the SYSMON, see *UltraScale Architecture System Monitor User Guide (UG580)*.

Table 3: Voltage Rail Domains

Domain	SYSMON on Zynq UltraScale+ MPSoC	Power Rail on SOM
+5V Input	$V_P/V_N$	$V_{IN\_5V0}$
PS	$V_{CC\_PSINTLP}$ $V_{CC\_PSINTFP}$	$V_{CC\_PS\_0V85}$ (0.85V)
PS	$V_{CC\_PSAUX}$	$V_{CC\_PS\_1V80}$ (1.8V)
PL	$V_{CCINT}$	$V_{CC\_PL\_0V72}$ (0.72V)
PL	$V_{CCAUX}$	$V_{CC\_PL\_1V80}$ (1.8V)
PL	$V_{CCBRAM}$	$V_{CC\_PL\_0V85}$ (0.85V)

The Zynq UltraScale+ MPSoC SYSMON is supported for Linux applications by the AMD analog mixed signal (AMS) driver, available in the AMD [ADC](#) GitHub. The SYSMON is supported for bare-metal applications by the [SYSMONPSU](#) driver.

## SOM Power Integrity

The K26 SOM and K24 SOM are equipped with adequate decoupling capacitors on all PS and PL voltage rails to support a defined set of transient step loads. The programmable logic (PL) and processing system (PS) designs must not exceed the specified maximum current limit and the corresponding step loads as listed in the following tables.

**Table 4: PL Design Limits for K26 SOM**

Voltage Rail	Voltage (V)	Maximum Current (A)	Step Load (% of Maximum Current)
V <sub>CCINT</sub>	0.72	6.5	50
V <sub>CCINT_VCU</sub>	0.9	3.5	50

**Table 5: PS Design Limits for K26 SOM**

Voltage Rail	Voltage (V)	Maximum Current (A)	Step Load (% of Maximum Current)
V <sub>CC_PSINTLP</sub> and V <sub>CC_PSINTFP</sub>	0.85	3.5	25
V <sub>CCO_PSIO</sub>	1.8	0.300	100

**Table 6: PL Design Limits for K24 SOM**

Voltage Rail	Voltage (V)	Maximum Current (A)	Step Load (% of Maximum Current)
V <sub>CCINT</sub>	0.72	3.13	100
V <sub>CCINT_IO</sub>	0.85	0.08	40

**Table 7: PS Design Limits for K24 SOM**

Voltage Rail	Voltage (V)	Maximum Current (A)	Step Load (% of Maximum Current)
V <sub>CC_PSINTLP</sub> and V <sub>CC_PSINTFP</sub>	0.85	2.27	25
V <sub>CCO_PSIO</sub>	1.8	0.29	100

## SOM Power Estimation

AMD has created the Power Design Manager (PDM) tool (download at [www.amd.com/power](http://www.amd.com/power)) for power estimation. The PDM tool supports SOM developers to get power estimation based on their applications.

The following thermal guides provide documentation to support the integration of the SOM into your application system thermal and mechanical solutions including thermal modeling and detailed design specifications.

- *Kria K26 SOM Thermal Design Guide* ([UG1090](#))
- *Kria K24 SOM Thermal Design Guide* ([UG1094](#))

# Mechanical Design Considerations

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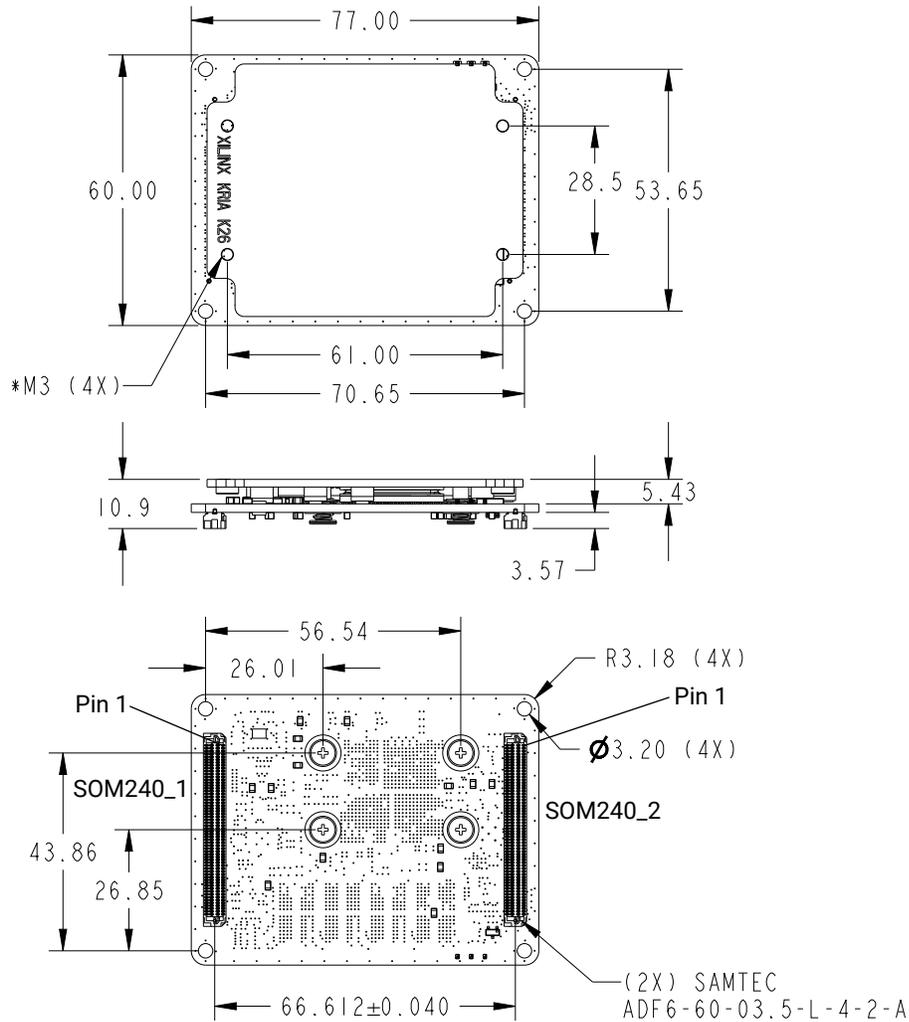
## K26 SOM Mechanical Dimensions

The following table and figures define the mechanical specifications of the K26 SOM. The following mechanical drawing provides the detailed dimensions of the SOM.

*Table 8: K26 SOM Mechanical Specifications*

Parameter	Specification
SOM length	77 mm
SOM width	60 mm
SOM height (without a thermal solution)	10.9 mm
Mass	58 grams

Figure 6: K26 SOM Dimensions



Notes:

1. All dimensions in mm.
2. Mass: 58G.
3. Mounting holes (\*) are reserved for customer's cooling installation.
4. Tolerance unless otherwise specified: ±0.13.

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The K26 SOM 3D CAD files are available for your platform or carrier design reference. These files are design aides in your cooling mechanical design, system assembly interference and clearance reviews, and board-to-board (B2B) connector placement alignment checks.

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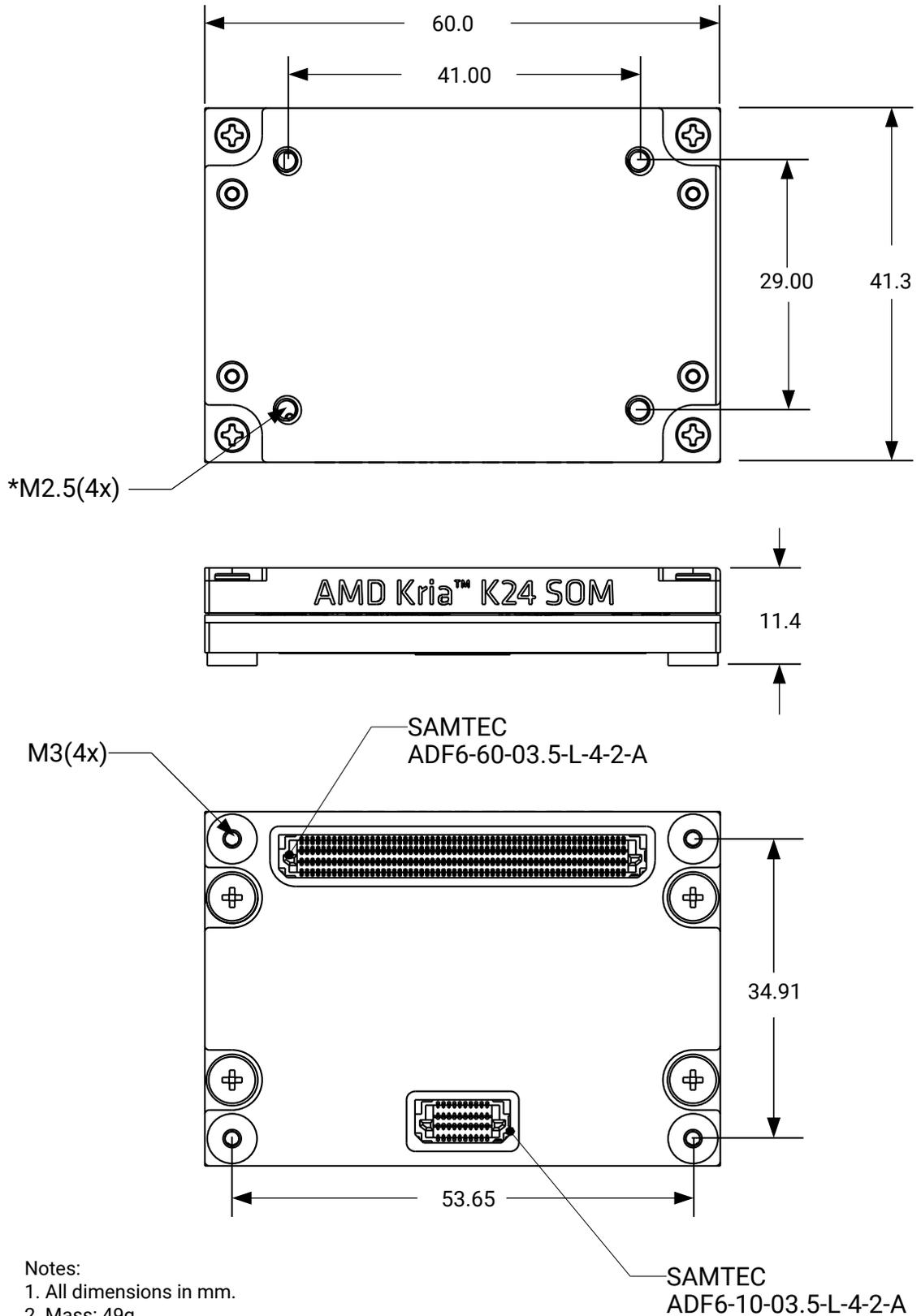
## K24 SOM Mechanical Dimensions

The following table and figures define the mechanical specifications of the K24 SOM. The following mechanical drawing provides the detailed dimensions of the SOM.

*Table 9: K24 SOM Mechanical Specifications*

Parameter	Specification
SOM length	60 mm
SOM width	41.3 mm
SOM height (without a thermal solution)	11.4 mm
Mass	49 grams

Figure 7: K24 SOM Dimensions



- Notes:
1. All dimensions in mm.
  2. Mass: 49g.
  3. \*M3(4x) holes are reserved for customer's cooling installation.
  4. Tolerance unless specified otherwise:  $\pm 0.13$  mm.

SAMTEC  
ADF6-10-03.5-L-4-2-A

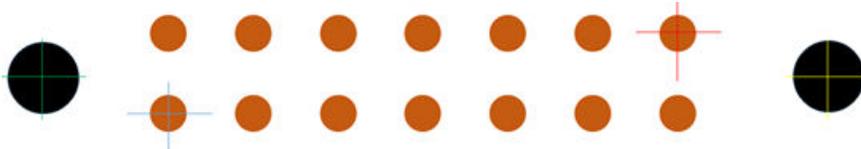
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The K24 SOM 3D CAD files are available for your platform or carrier design reference. These files are design aides in your cooling mechanical design, system assembly interference and clearance reviews, and board-to-board (B2B) connector placement alignment checks.

## PCB Fabrication and Assembly House Requirements

The following are requirements for the fabrication of the PC board assembly.

- Carrier card PCB pad-to-pad tolerance should be  $< \pm 25 \mu\text{m}$ .

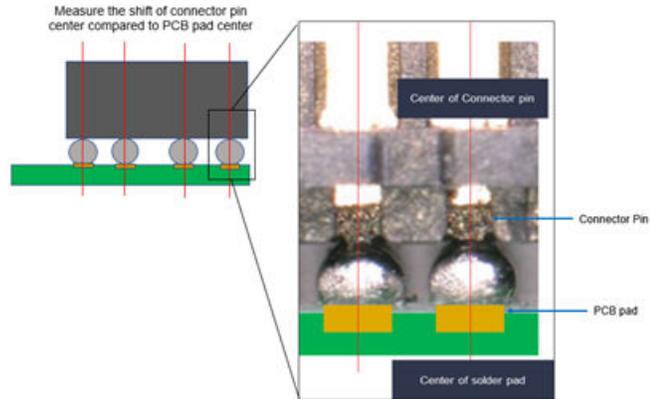


The blue to red cross (surface pad to surface pad) tolerance with respect to the Gerber pad location should be less than  $\pm 1\text{mil}$  ( $25 \mu\text{m}$ ).

- Carrier card assembly house placement capability should be  $< \pm 26 \mu\text{m}$ .
- RMS value of the PCB pad-to-pad and component placement tolerance, based on the capabilities listed above should be  $< \pm 36 \mu\text{m}$ .
- Samtec recommends a tolerance of  $\pm 0.04 \text{ mm}$  in the distance between the connectors.
- The combination of all these requirements must be controlled to less than  $\pm 40 \mu\text{m}$ .

The evaluation of Samtec connector placement is conducted by shifting the placement of the connector from 0% (PCB pad center aligned with connector pin center) to 15% (pin center offset by 15% of PCB pad width). The shifted connectors are capable of self-aligning after a reflow soldering process. The following image shows that even though placement of the connector shifted by 15% of the pad width, the connector solder ball was still able to self-align to the center of pad.

Figure 8: Connector Pin/Pad Placement



**Note:** PCB fab and assembly contractors must be able to produce carrier cards to the specifications listed in the [PCB Fabrication and Assembly House Requirements](#) section. In addition, the connectors that are shifted by 15% of the pad width must be capable of self-aligning after a reflow soldering process.

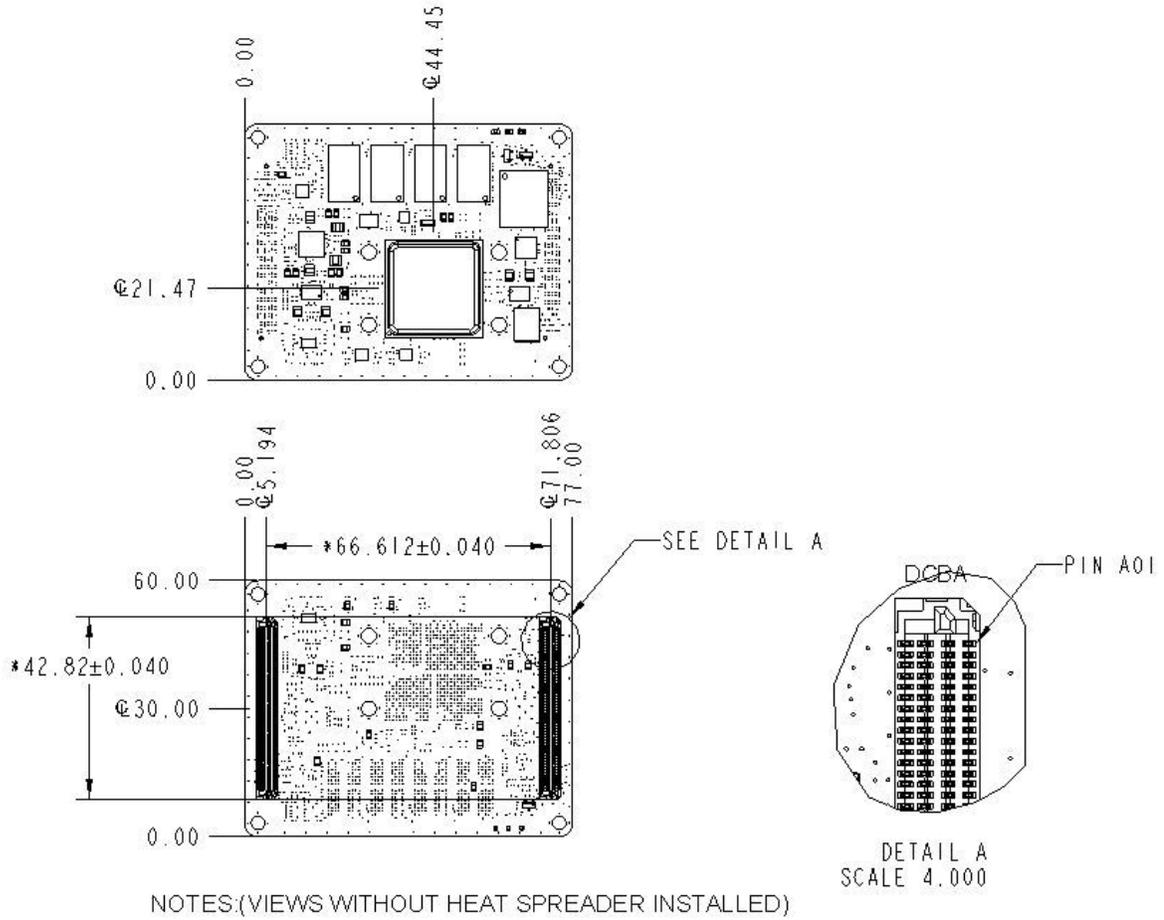
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## K26 SOM to Carrier Card Samtec Connector Placement Guidelines

Both the commercial (C) grade and industrial (I) grade SOMs have two Samtec 0.635 mm AcceleRate® HD high-density, 4-row, 60-position connectors. The Samtec part number is ADF6-60-03.5-L-4-2-A. The connectors are placed on the bottom side of the carrier card centered between the mounting holes shown in [Figure 6: K26 SOM Dimensions](#).

Board-to-board (B2B) mating connectors must be precisely placed on the PCB, particularly for multi-pair connector applications. Tight control is required during the board layout design and the manufacturing process for product reliability and a decent yield rate. To avoid over-stressing the mechanical design of the connectors and creating functional damage during system assembly, the next figure includes the recommended maximum position tolerance of the connector. Auto-placement machine accuracy and the tolerance of the connector pin solder pad position contributes to this recommendation.

Figure 9: K26 SOM Samtec Connector Position Tolerance



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## K24 SOM to Carrier Card Samtec Connector Placement Guidelines

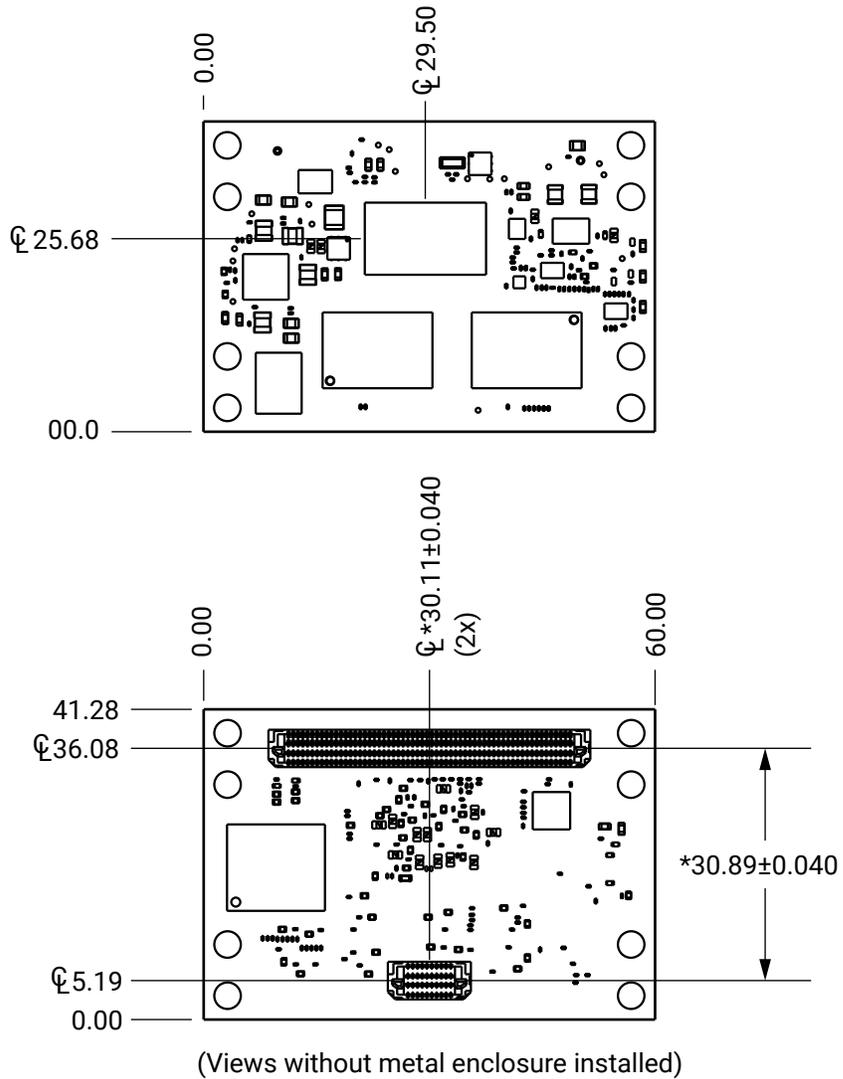
Both the commercial (C) grade and industrial (I) grade K24 SOMs have two Samtec 0.635 mm AcceleRate® HD high-density connectors.

- The SOM240\_1 connector uses the Samtec 0.635 mm AcceleRate HD high-density 4-row, 60 position connector set. The part number for the socket (ADF6-60-03.5-L-4-2-A) is used on the bottom side of the SOM. The part number for the terminal (ADM6-60-01.5-L-4-2-A) is for use on the carrier card.
- The SOM40 connector uses the Samtec 0.635 mm AcceleRate HD high-density 4-row, 10 position connector set. The part number for the socket (ADF6-10-03.5-L-4-2-A) is used on the bottom side of the SOM. The part number for the terminal (ADM6-10-01.5-L-4-2-A) is for use on the carrier card.

The connectors are placed on the bottom side of the carrier card centered between the mounting holes shown in [Figure 7: K24 SOM Dimensions](#).

Board-to-board (B2B) mating connectors must be precisely placed on the PCB, particularly for multi-pair connector applications. Tight control is required during the board layout design and the manufacturing process for product reliability and a decent yield rate. To avoid over-stressing the mechanical design of the connectors and creating functional damage during system assembly, the next figure includes the recommended maximum position tolerance of the connector. Auto-placement machine accuracy and the tolerance of the connector pin solder pad position contributes to this recommendation.

Figure 10: K24 SOM Samtec Connector Position Tolerance



Notes:

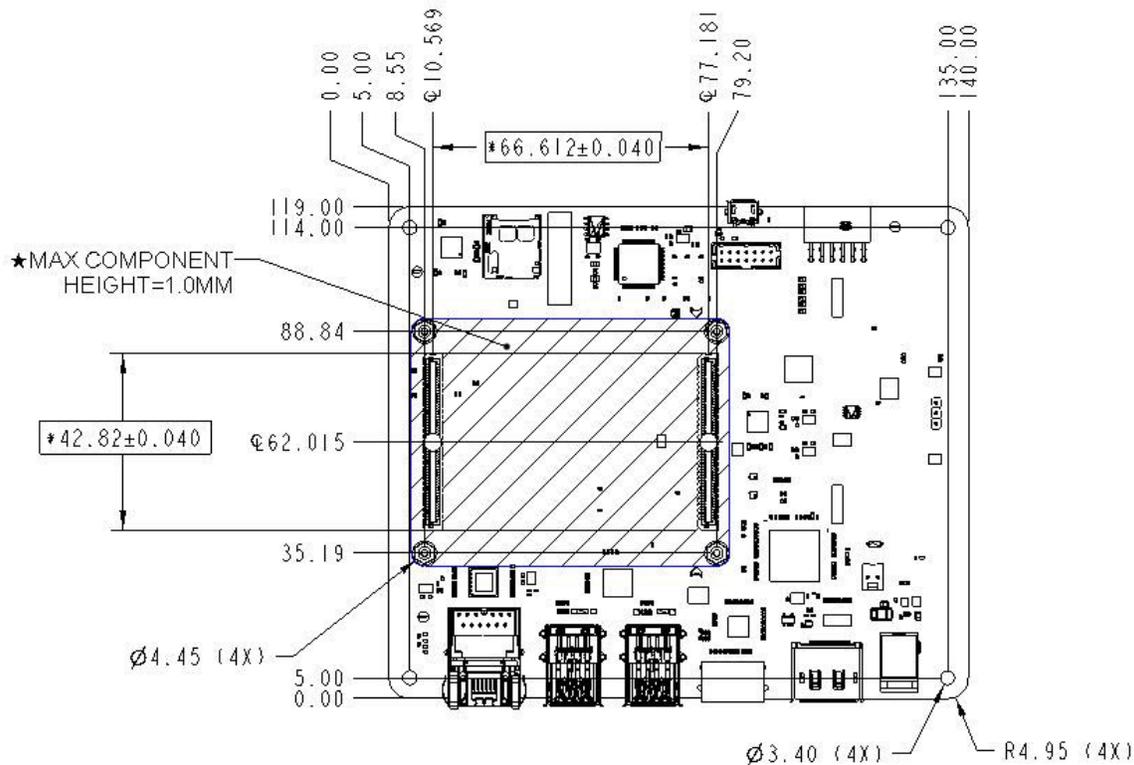
1. All dimensions are in mm.
2.  $\phi$  Centerline of SoC, connectors.
3. \* B2B connector placement machine X,Y accuracy: 0.026 mm/3-sigma.
4. \* B2B connector footprint solder pad tolerance: 0.025 mm.
5. Tolerance unless specified otherwise:  $\pm 0.13$  mm.

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# Carrier Card Board to Board Connector Placement Guideline for K26 SOM

Corresponding to the Samtec 0.635 mm AcceleRate HD connectors (ADF6-60-03.5-L-4-2-A) on the SOM, the mating connectors (ADM6-60-01.5-L-4-2-A) are placed on your carrier card. See the note about the Samtec [REF-226081](#) alternative mating connector. The two SOM mating connectors must be placed and positioned using a tightly controlled design and manufacture processing. The following figure shows the keep-out area and connector position tolerance information used on an example carrier card design. The keep out area defined maximum component height is 1.0 mm.

Figure 11: Carrier Card Board to Board Connector Placement Tolerances

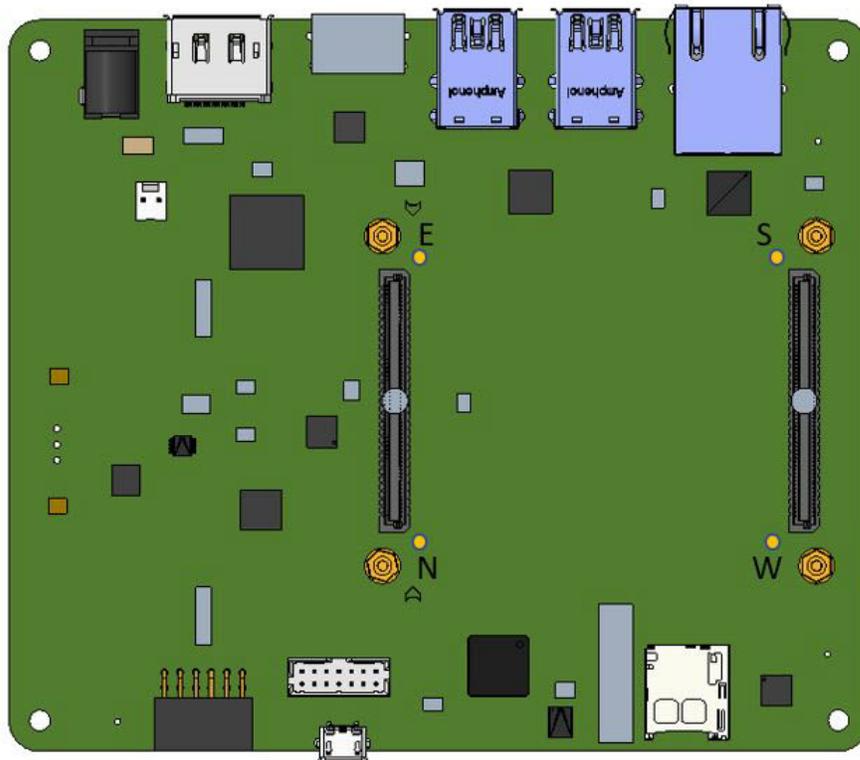


NOTES:

1. ALL DIMENSION IN MM.
2.  $\phi$ -CENTERLINE OF CONNECTOR.
3. \* B2B CONNECTOR PLACEMENT MACHINE X,Y ACCURACY:  $\pm 0.026\text{MM}/3\text{-SIGMA}$ .
4. \* B2B CONNECTOR FOOTPRINT SOLDER PAD TOLERANCE:  $\pm 0.025\text{MM}$ .
5. ★DETAIL COMPONENT KEEPOUT INFO REFER TO PCB LAYOUT DESIGN GUIDELINE.
6. TOLERANCE UNLESS OTHERWISE SPECIFIED:  $\pm 0.13$ .

During board-to-board insertion and removal, the installation process should work within the following recommended strain limits. The following figure shows the recommended locations (E-W, N-S) for a strain measurement on a carrier card. Diagonal strain should not exceed 500 micro-strain during mating. Strain rate duration taken to reach maximum 500 micro-strain should not be less than four seconds. Based on experimental data, the maximum strain of 428 micro-strain reached in 3.63 seconds duration and was validated through dye and pry, where the sample passed.

Figure 12: Recommended Locations for Strain Measurement on a Carrier Card



## Board to Board Connector Distance Tolerance Control for K26 SOM

The distance between the mating Samtec [ADM6-60-01.5-L-4-2-A](#) connectors on the carrier card must match the distance between the [ADF6-60-03.5-L-4-2-A](#) connectors on the SOM.

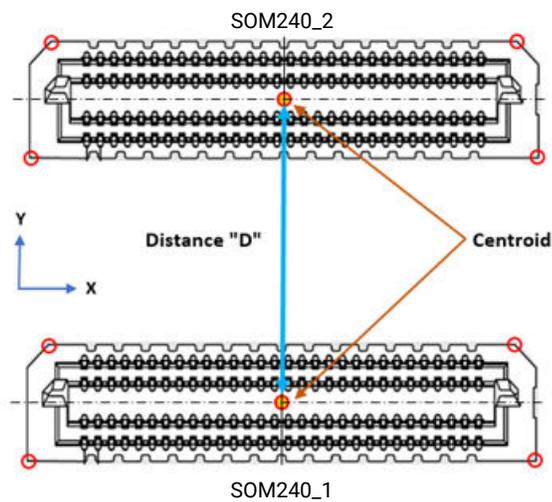
See the note about the Samtec [REF-226081](#) alternative mating connector.

The final connector position is dictated by auto-placement machine accuracy and PCB pad position tolerance. The way the distance is measured between connectors is crucial to ensure seamless board-to-board mating, without applying mechanical stress.

To determine the centroid of the connector, use the four corners of the connector edges marked with red circles as shown in the following figure. By using a high-accuracy optical measurement instrument, measure the distance  $D$ . Distance  $D$  should be 66.612 mm (nominal). The allowable distance  $D$  and tolerance is  $66.612 \pm 0.04$  mm center to center. The following table shows the recommended optical measurement instrument specifications.

Name	OGP Smartscope
Model	CNC670
Accuracy	$\pm 5 \mu\text{m}$

Figure 13: Connector Distance Measurement

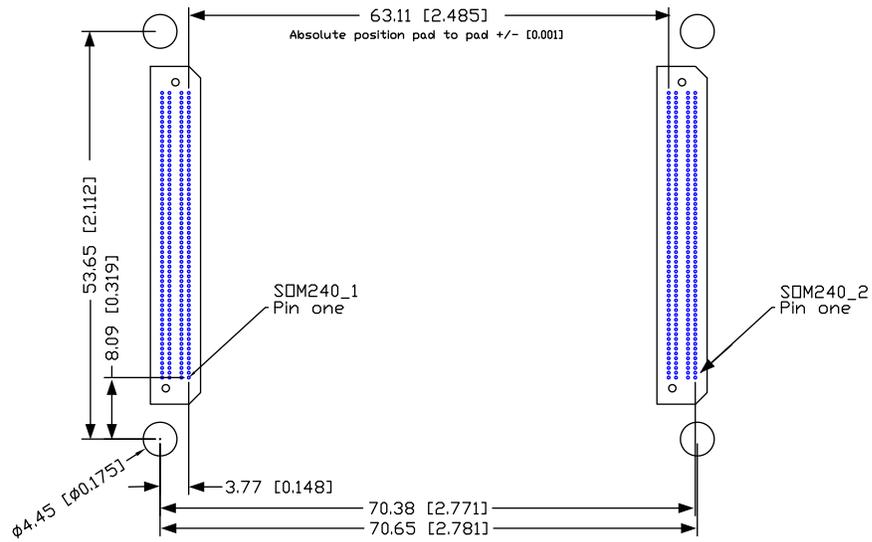


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## Board to Board Connector PCB Layout for K26 SOM

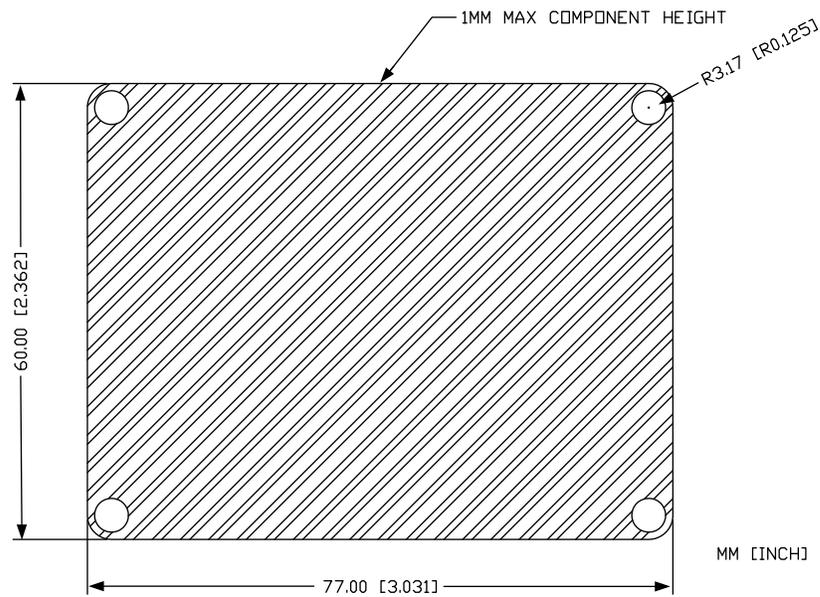
The following figure shows the top view of the carrier card SOM connector locations and mechanical standoff relative placement.

Figure 14: SOM240 Connector Pad Requirements on K26 Carrier Card (Top View)



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Figure 15: K26 Keep Out Requirements on K26 Carrier Cards (Top View)



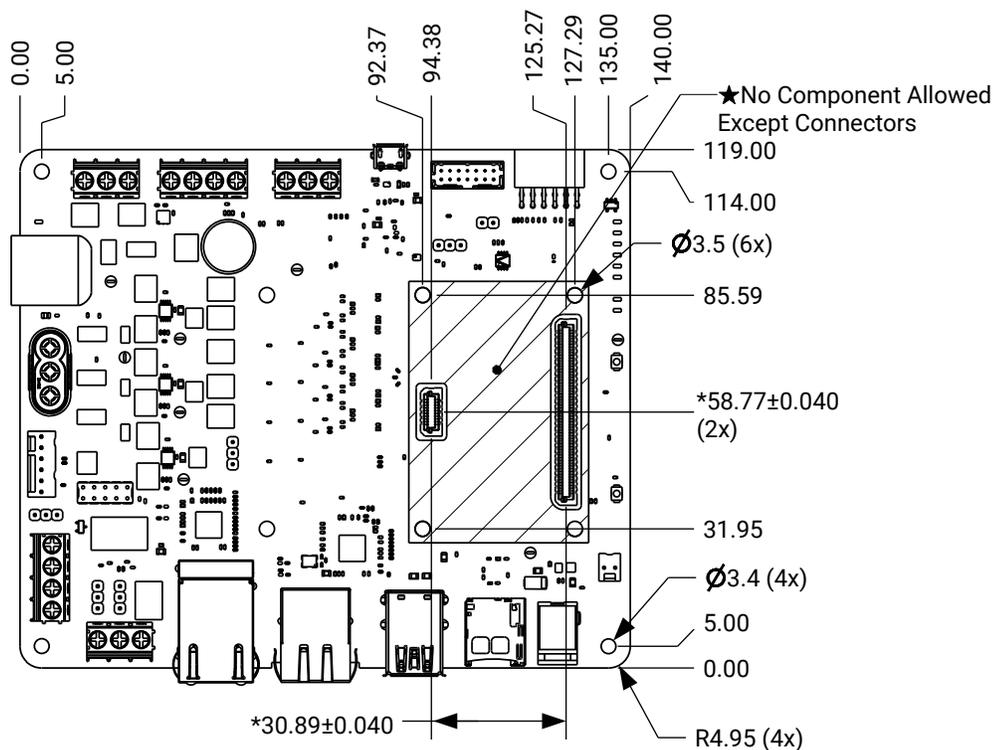
MM [INCH]

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# Carrier Card Board to Board Connector Placement Guideline for K24 SOM

Corresponding to the Samtec 0.635 mm AcceleRate HD connectors (ADF6-10-03.5-L-4-2-A) on the SOM, the mating connectors (ADM6-60-01.5-L-4-2-A and ADM6-10-01.5-L-4-2-A) are placed on your carrier card. See the note about the Samtec [REF-226081](#) alternative mating connector. The two SOM mating connectors must be placed and positioned using a tightly controlled design and manufacture processing. The following figure shows the keep-out area and connector position tolerance information used on an example carrier card design.

Figure 16: Carrier Card Board to Board Connector Placement Tolerances for K24 SOM



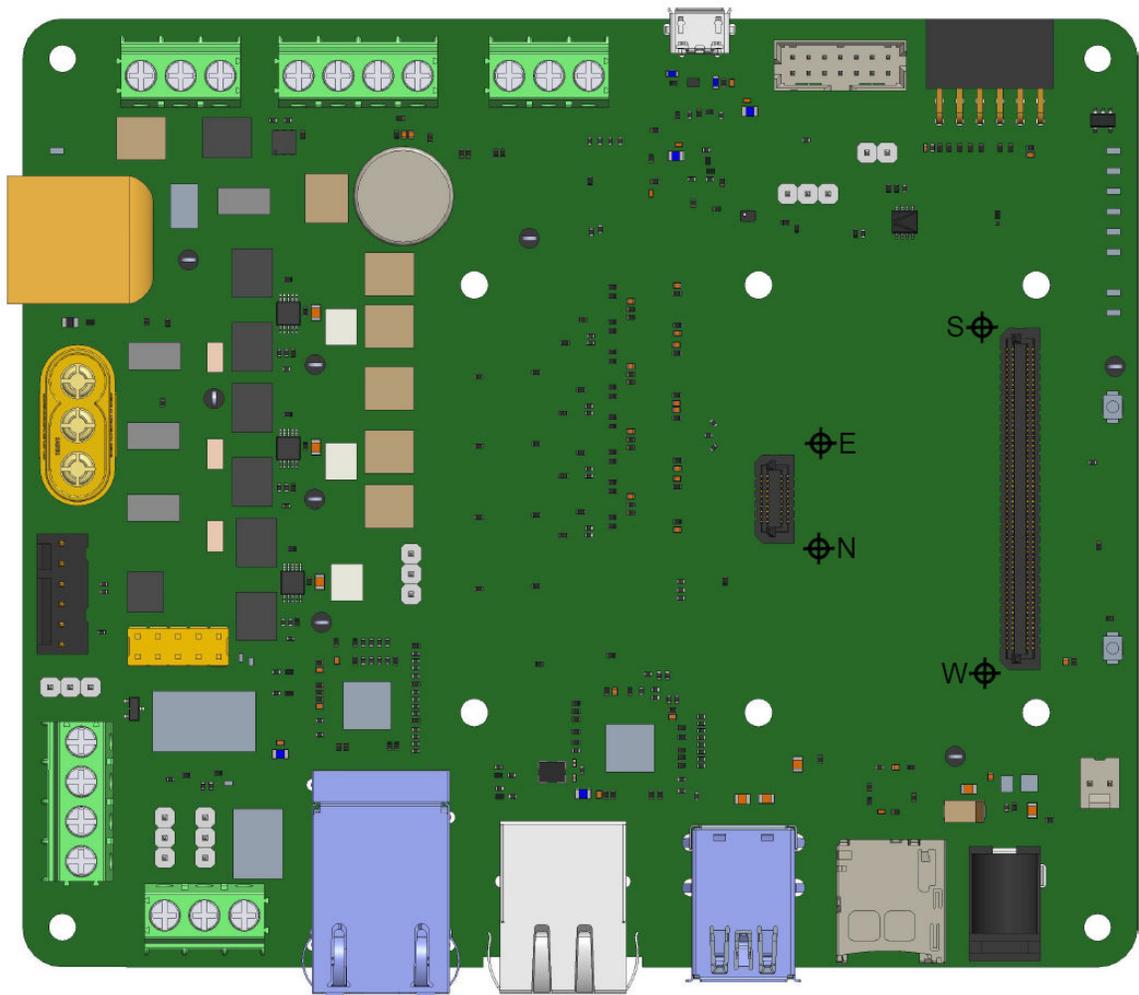
Notes:

1. All dimensions in mm.
2. Centerline of SoC, connectors.
3. \*B2B connector placement machine X,Y accuracy: 0.026 mm/3-sigma.
4. \* B2B connector footprint solder pad tolerance: 0.025 mm.
5. Component keep-out information, refer to PCB layout design guideline.
6. Tolerance unless specified otherwise:  $\pm 0.13$ .

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During board-to-board insertion and removal, the installation process should work within the following recommended strain limits. The following figure shows the recommended locations (E-W, N-S) for a strain measurement on a carrier card. Diagonal strain should not exceed 500 micro-strain during mating. Strain rate duration taken to reach maximum 500 micro-strain should not be less than four seconds. Based on experimental data, the maximum strain of 222 micro-strain reached in 4.42 seconds duration and was validated through dye and pry, where the sample passed.

**Figure 17: Recommended Locations for Strain Measurement on a Carrier Card for a K24 SOM**



## Board to Board Connector Distance Tolerance Control for K24 SOM

The distance between the mating Samtec [ADM6-60-01.5-L-4-2-A](#) and [ADM6-10-01.5-L-4-2-A](#) connectors on the carrier card must match the distance between the [ADF6-60-03.5-L-4-2-A](#) and [ADF6-10-03.5-L-4-2-A](#) connectors on the SOM.

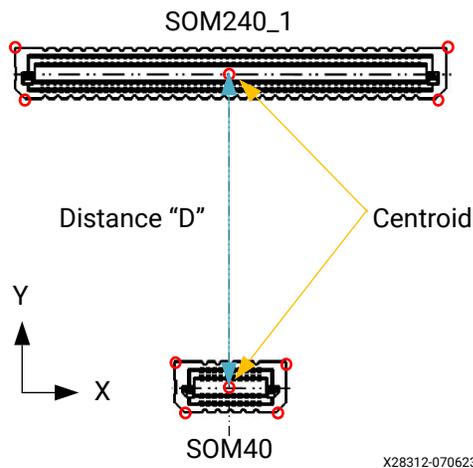
See the note about the Samtec [REF-226081](#) alternative mating connector.

The final connector position is dictated by auto-placement machine accuracy and PCB pad position tolerance. The way the distance is measured between connectors is crucial to ensure seamless board-to-board mating, without applying mechanical stress.

To determine the centroid of the connector, use the four corners of the connector edges marked with red circles as shown in the following figure. By using a high-accuracy optical measurement instrument, measure the distance  $D$ . Distance  $D$  should be 30.89 mm (nominal). The allowable distance  $D$  and tolerance is  $30.89 \pm 0.04$  mm center to center. The following table shows the recommended optical measurement instrument specifications.

Name	OGP Smartscope
Model	CNC670
Accuracy	$\pm 5 \mu\text{m}$

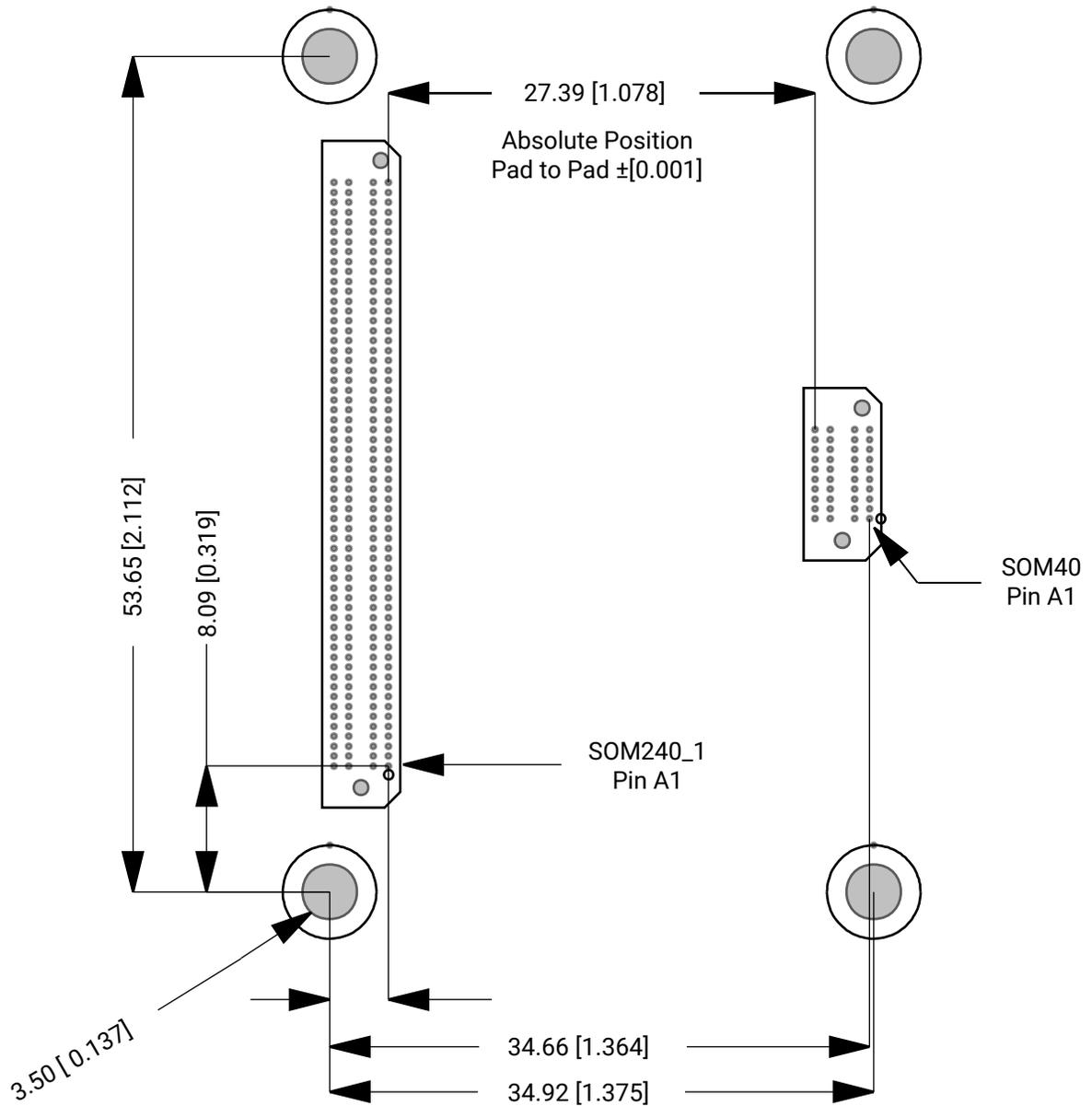
Figure 18: K24 SOM Connector Distance Measurement



## Board to Board Connector PCB Layout for K24 SOM

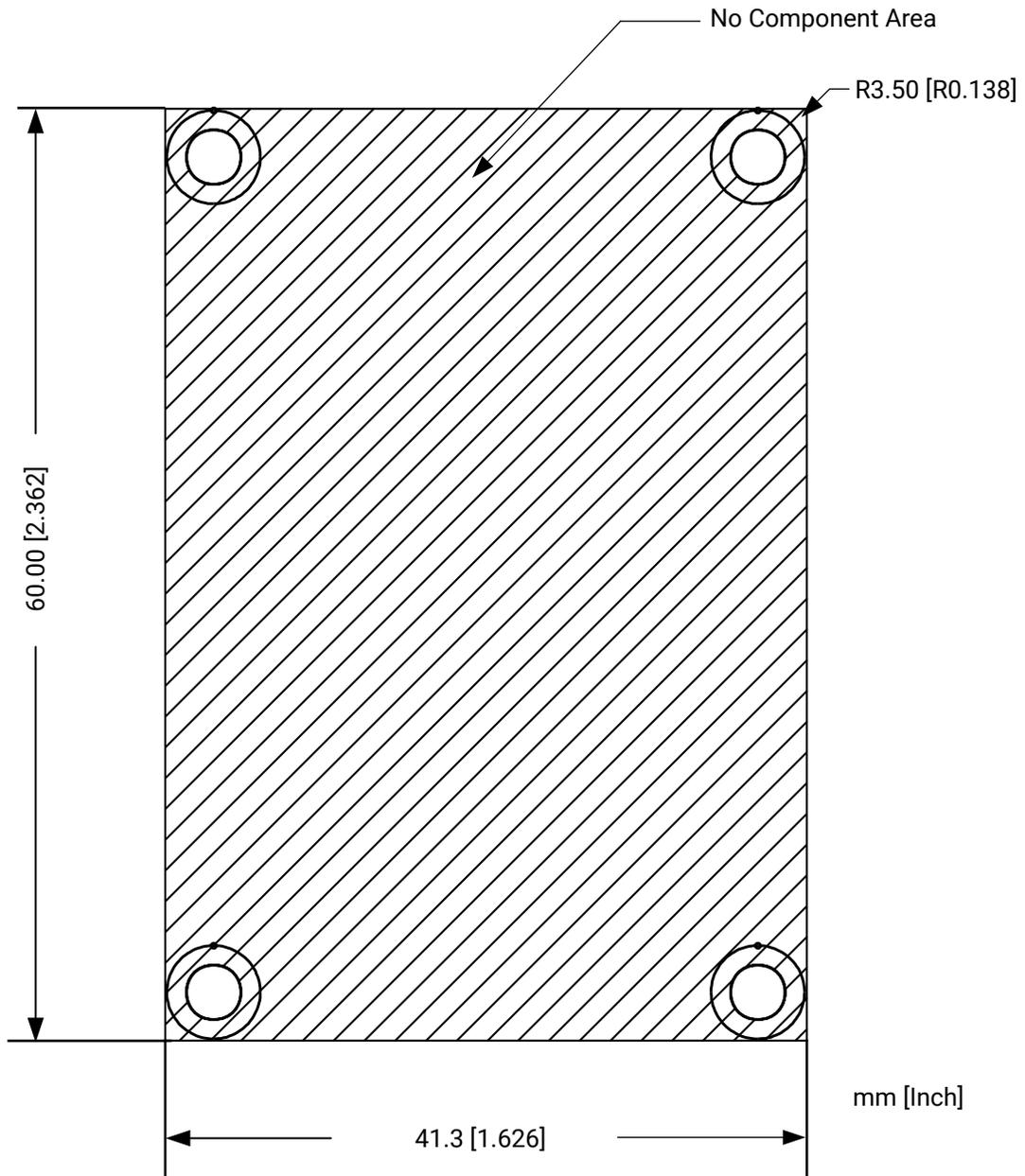
The following figure shows the top view of the carrier card SOM connector locations and mechanical standoff relative placement.

Figure 19: K24 SOM Connector Pad and Standoff Placement



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Figure 20: K24 SOM Connector Pad and Standoff Placement Dimensions



X28315-092023

# Board to Board Connector Stencil Design

To ensure that at time zero no crack has occurred, solder paste is applied to PCB metal pads using screen printing. The volume of the printed solder paste is determined by the stencil aperture and its thickness. In most cases, the thickness of a stencil must be matched to the needs of all components on the PCB. Stencil apertures should be a circular shape. A laser cutting (mostly made from stainless steel) with nickel blanking is preferred to ensure that both uniform and high-solder paste is transferred to the PCB. The recommended stencil design dimensions are listed in the following table and shown in the image.

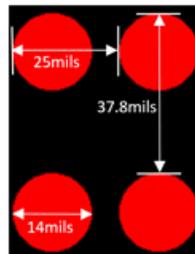
Table 12: Board to Board Connector Recommended Stencil Design

Aperture Shape	Pitch	Diameter	Stencil Thickness
Round	25 mils and 37.8 mils	14 mils	5 mils

Figure 21: Board to Board Connector Recommended Stencil Design



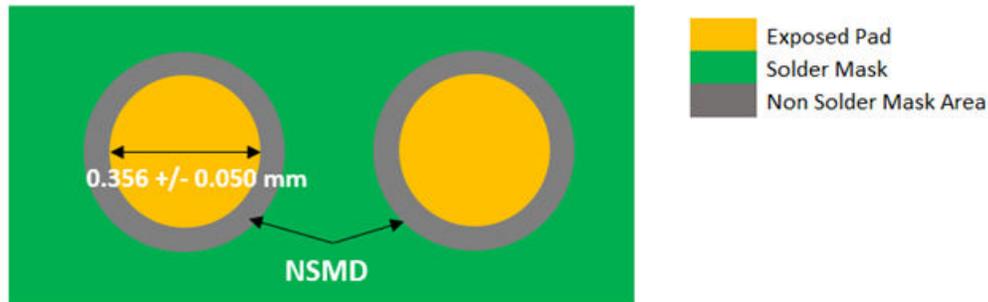
● Stencil aperture



## Footprint Details

PCB pad design should be in a circular shape with diameter of  $0.356 \pm 0.050$  mm ( $14.0 \pm 2.0$  mils). Non-solder mask defined (NSMD) pad design as shown in the following figure is recommended for better reliability performance.

Figure 22: Recommended PCB Layout for Board to Board Connector



## Recommended Pb-free Reflow Soldering Profile

AMD does not support soldering SnAgCu BGA connectors with Sn/Pb solder paste during the soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of  $220^{\circ}\text{C}$ . At this temperature range, the SnAgCu BGA solder balls cannot properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take a few factors into account:

- Solder paste flux used
- Size of the board
- Density of the components on the board
- Ratio of large and small, lighter components (the mixture)

Profiles should be established for all new board designs using thermocouples placed at multiple locations on the component. In addition, if there is a mixture of devices on the board, the profile should be checked at various board locations to ensure that the minimum reflow temperature is reached on the larger components, and at the same time the temperature does not exceed the threshold that might damage the smaller, heat sensitive components.

The following tables and figures provide the recommended guidelines for Pb-free solder PCB assembly reflow. In general, a gradual-linear ramp into a spike is proven, by various sources, to be the optimal reflow profile for Pb-free solder. This profile results in a better wetting yield and less thermal shock than the conventional ramp-soak-spike profile. It is a known fact that SnAgCu (SAC) alloy reaches its full liquidus at a temperature of 235°C. In the reflow profiling, the coldest solder joints need to be identified and to ensure that they reach a minimum peak temperature of 235°C for at least 10 seconds. Reflowing at high-peak temperatures of 260°C or above can damage the heat sensitive components and cause board warpage. Refer to the latest IPC/JEDEC J-STD-020 standard for allowable peak temperature on the components. The allowable component peak temperature is determined by the component size. The following table lists the reflow soldering temperature profile information. In any case, use as low of a peak temperature reflow profile as possible. The following image shows an example of the reflow temperature profile.

**Table 13: Recommended Reflow Soldering Temperature Profile**

Profile Feature	Convection, IR/Convection
Preheat ramp-up rate 30°–150°C	3°C/s maximum
Preheat temperature soak time 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–120 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak temperature (lead/ball)	235°C–245°C typical (depends on solder paste, board size, component mixture)
Ramp-down rate	4°C/s maximum

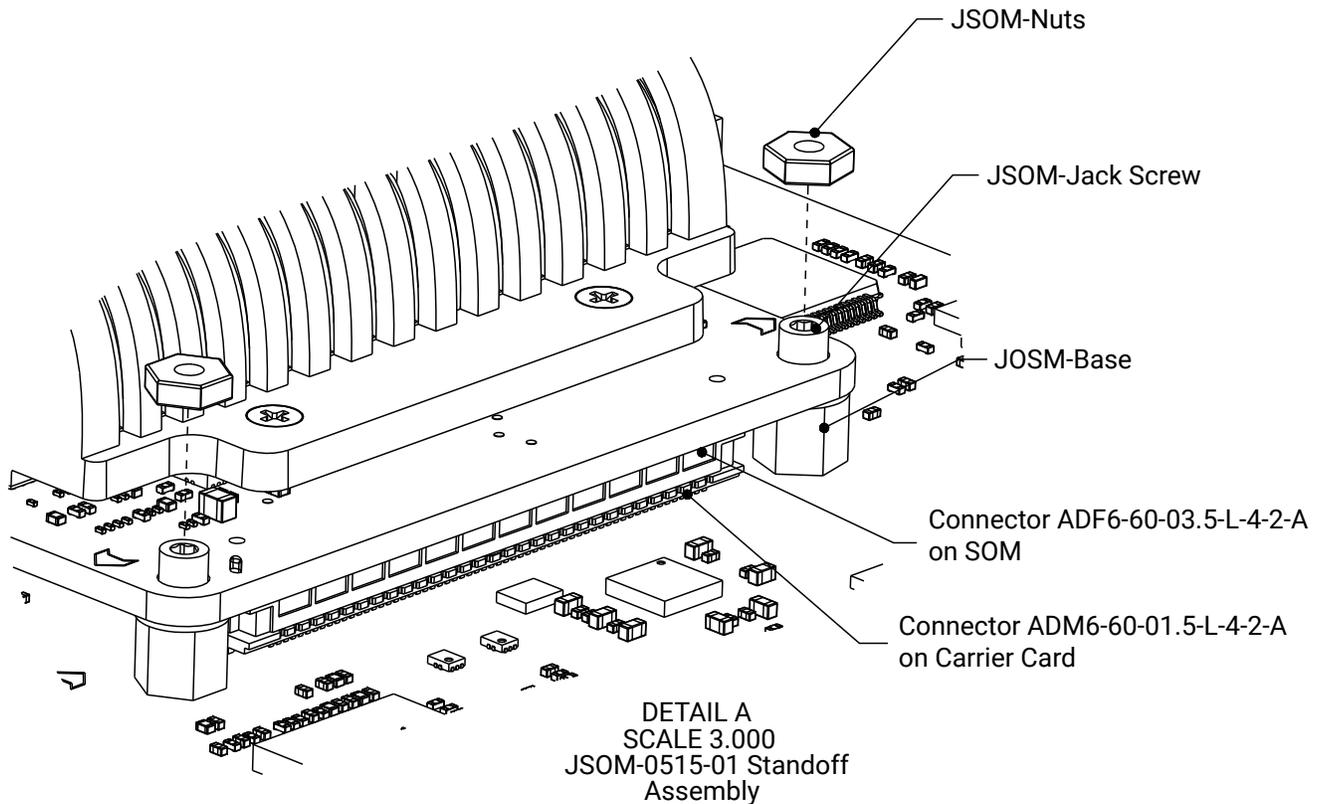
**Figure 23: Recommended Reflow Soldering Temperature Profile**



# Board to Board Assembly Guidelines (K26 SOM)

Samtec jack screw standoff, part number JSOM-0515-01, is recommended by Samtec to be used as mechanical support in its board-to-board (B2B) connector assembly. This JSOM type standoff protects connectors from over mechanical stresses during mating and de-mating assembly.

Figure 24: K26 SOM B2B Assembly with Samtec JSOM Standoffs

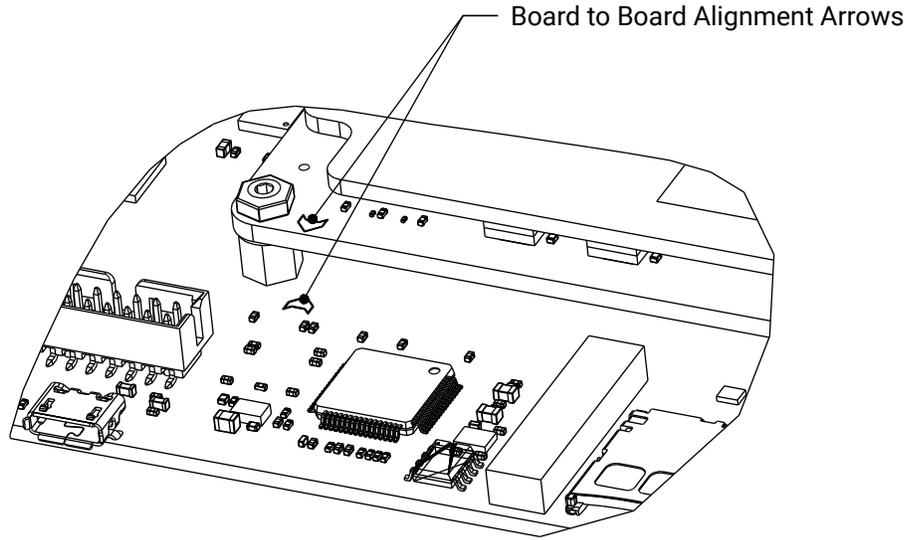


X25311-071321

See the note about the Samtec [REF-226081](#) alternative mating connector.

A recommended best practice is to put board-to-board alignment arrows on your carrier card silkscreen to aid in the orientation of the SOM to carrier card. It is important to check the connector alignment key positions before gently pressing down to fully engage the B2B connectors.

Figure 25: K26 SOM B2B Connector Orientation and Alignment



X25310-041621

## Carrier Card to K26 SOM Standoff Press-fit Process

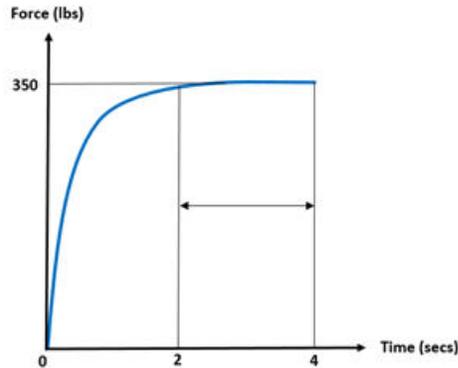
The carrier card to SOM interface requires a 5 mm (height) mechanical stand-off.

In cases where there is an expectation that the SOM might be removed from the carrier card, the recommended solution is to use the following Samtec JSOM. The Samtec JSOM-0515-01 standoffs require a press-fit process to install them onto the PCB. The JSOM standoff press-fit recommended parameters are shown the following table and the press profile is shown in the following diagram.

Table 14: JSOM Standoff Press-fit Parameters

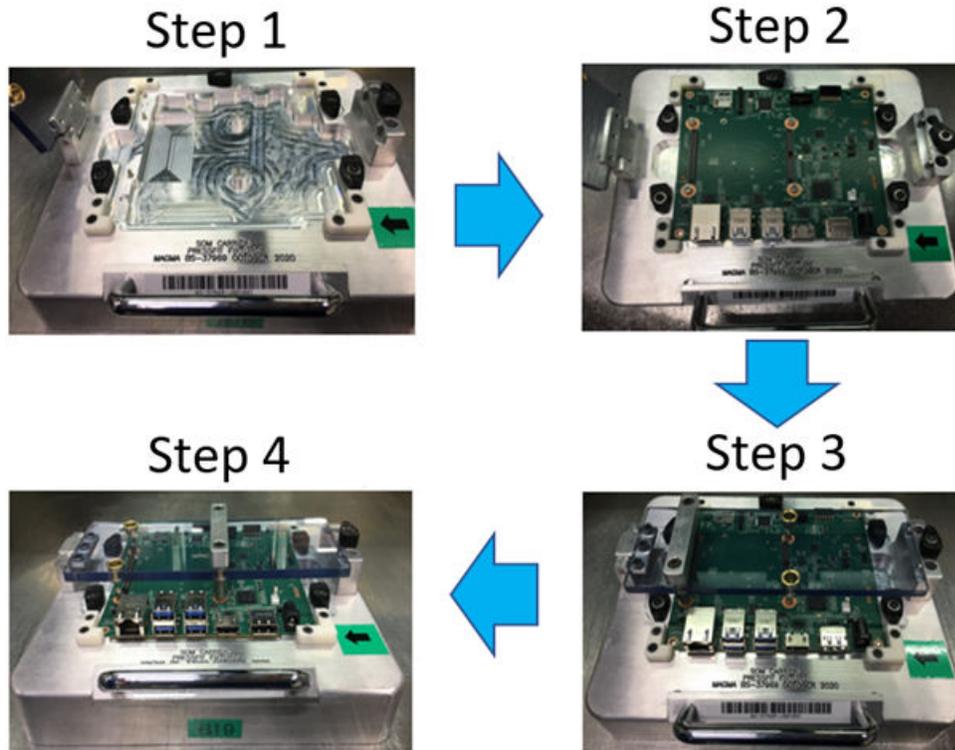
Press Parameter	Setting	Unit	Press Time
Force	350 ±10	lbs	2 secs

Figure 26: Press Profile (Force Over Time)



The following images detail the installation process by using a press-fit jig.

Figure 27: JSOM Standoff Installation Steps



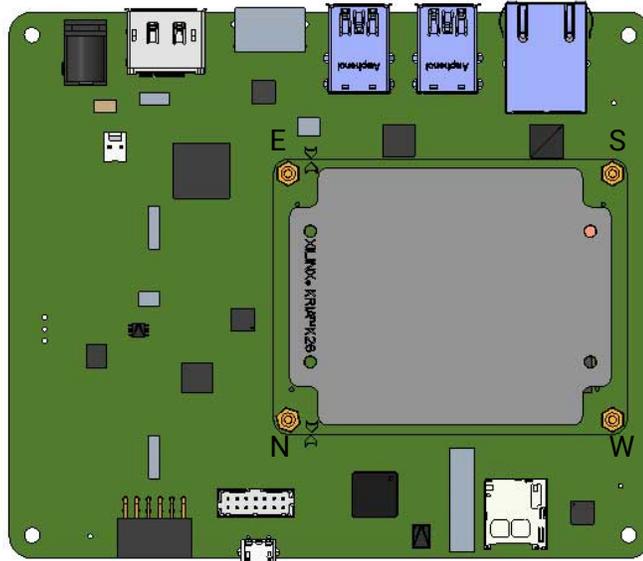
1. Open the top cover of the press-fit jig
2. Place the carrier card on the press-fit jig and insert the JSOM standoff. Close the press-fit jig cover.
3. Insert the connector top tool in the press-fit cover and place it on top of the two JSOMs located beside connector JA2. Press the JSOM standoff into the card following the parameters listed in [Table 14: JSOM Standoff Press-fit Parameters](#). Remove the top tool after the press-fit is completed.

- Repeat step 3 to install the JSOM standoff located beside connector JA1. Remove the board from the jig and inspect whether the JSOM standoff is fully flush.

## Mating: JSOM Standoff-nut Tighten Sequence and Torque Setup

To protect the mating connector from over mechanical stress and to minimize strain during board-to-board assembly, it is important to tighten the standoff nut in a specific sequence. The recommended mechanical standoff tightening sequence (S > W > N > E) is shown in the following figure. Once the S and W nuts are tightened, the SOM board is almost flat to the carrier card. The subsequent tightening of nuts N and E ensure the SOM and carrier connectors are completely engaged.

Figure 28: K26 SOM Connector Mating Sequence



The recommended torque driver setting and operation parameters are specified in the following table.

Table 15: Torque Driver Information

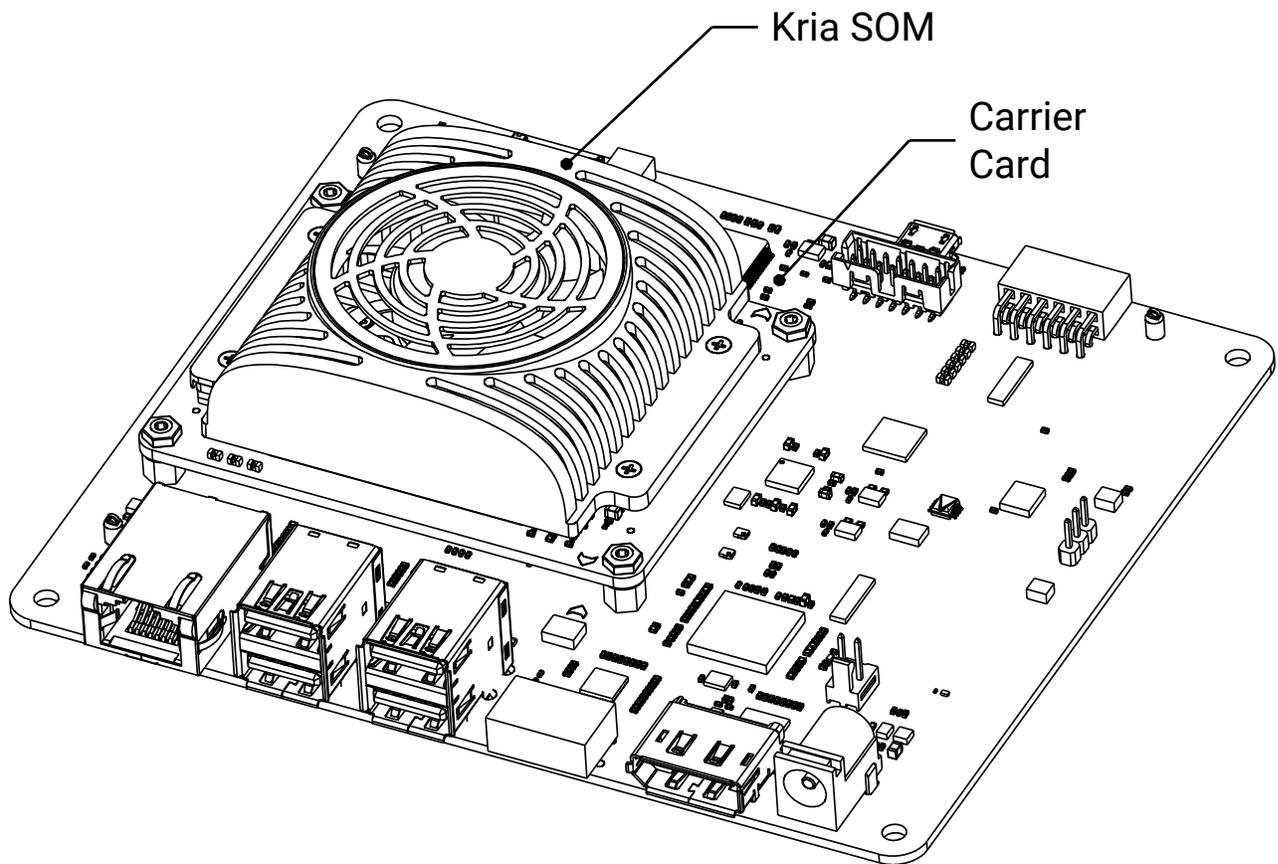
Torque Driver	Controller Module	Torque Driver	Torque Setting	Assembly Duration	RPM Setting for Each Step
Smart Torque Electrical Driver	Atlas Copco MTF600	ETD M 50 ABL V2	3.0 in.lbs (±0.5 in.lbs)	10 secs	Step 1: 300 RPM
					Step 2: 600 RPM
					Step 3: 150 RPM

## De-mating: JSOM Standoff-nut and Jack Screw Untighten Sequence

There is no special sequence required to untighten the four standoff nuts. However, they must be removed before proceeding to untighten the four jack screws. The order to untighten the four jack screws is not critical. Once all four of the jack screws are completely untightened, the SOM board pops up and the SOM connectors (male) automatically uncouple from the connectors (female) on the carrier card. Remove the SOM by carefully holding the card on the two edges.

## K26 SOM System Assembly Example

Figure 29: KV260 Vision AI Starter Kit Assembly

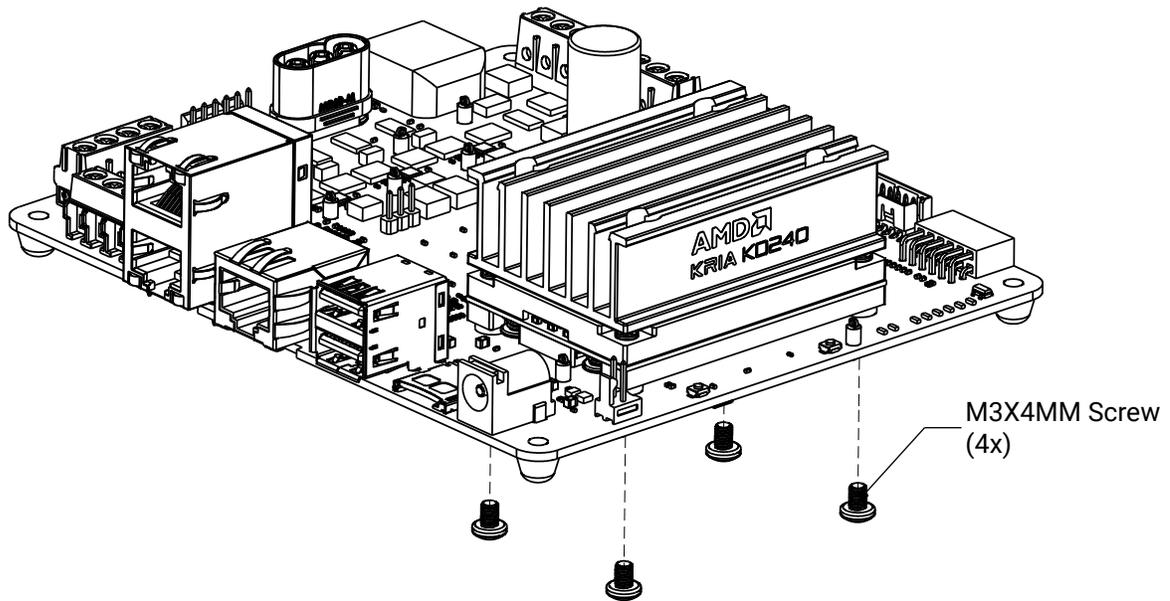


X28731-101023

## Board to Board Assembly Guidelines (K24 SOM)

The M3 screws shown in the following figure are used to secure the K24 to your carrier card. The length of the screw depends upon the assembly thickness. This example shows the KD240 starter kit with K24 SOM assembly.

Figure 30: B2B Assembly for K24 SOM



X28662-102523

See the note about the Samtec [REF-226081](#) alternative mating connector. It is important to check the connector alignment key positions before gently pressing down to fully engage the B2B connectors.

The K24 board assembly onto a KD240 carrier board is a manual mating process. Refer to the following figure for verification of the board-to-board orientation and assembly method (alignment key).

Figure 31: Board-to Connector Orientation (K24 SOM on Carrier Card)

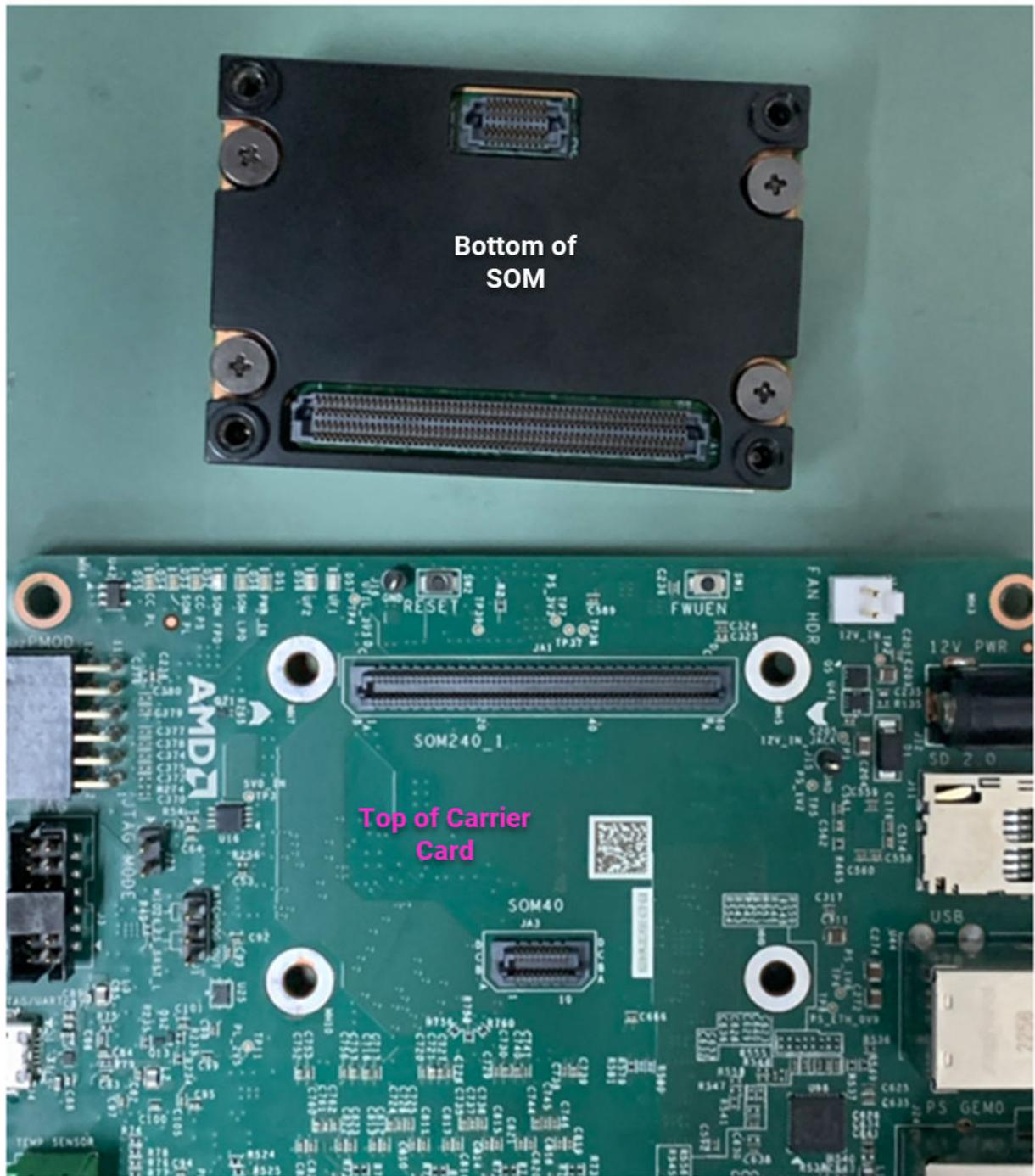
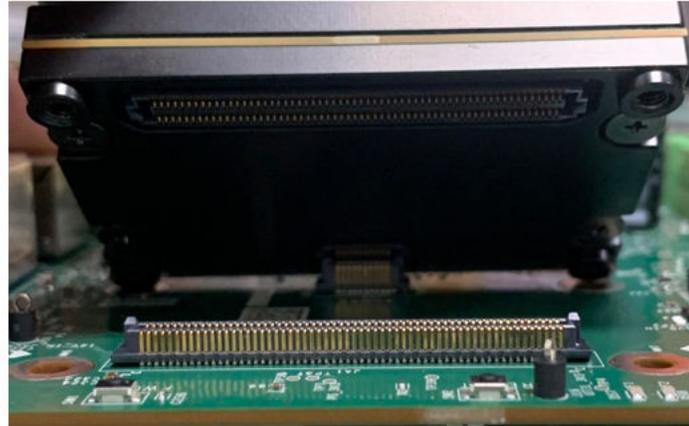


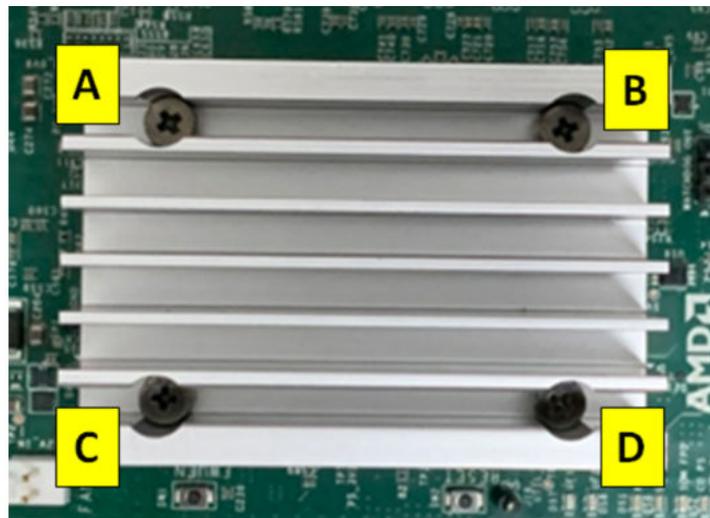
Figure 32: **B2B Assembly (Alignment Keys) (K24 SOM on Carrier Card)**



### Mating—Manual Press

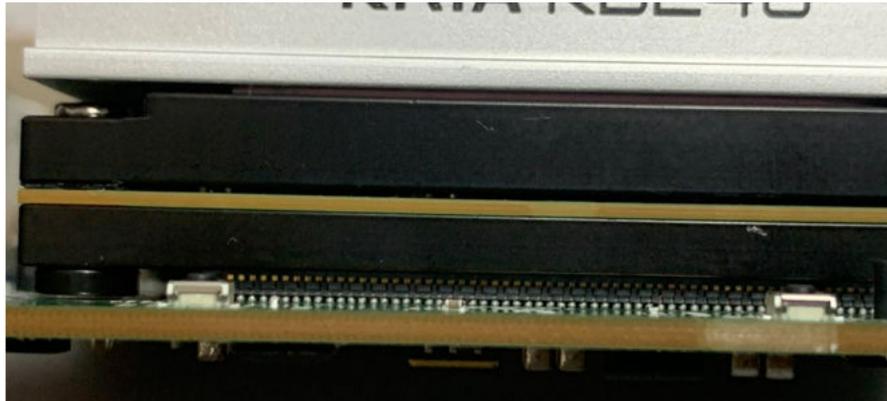
To protect the mating connector from mechanical stress and to minimize strain during board-to-board assembly, it is important to press the KD240 assembly board simultaneously on all points (A, B, C, D) as shown in the following figure.

Figure 33: **Press Points (K24 SOM on Carrier Card)**



After completing the mating process, you need to validate that both board connectors are fully engaged as shown in the following figures.

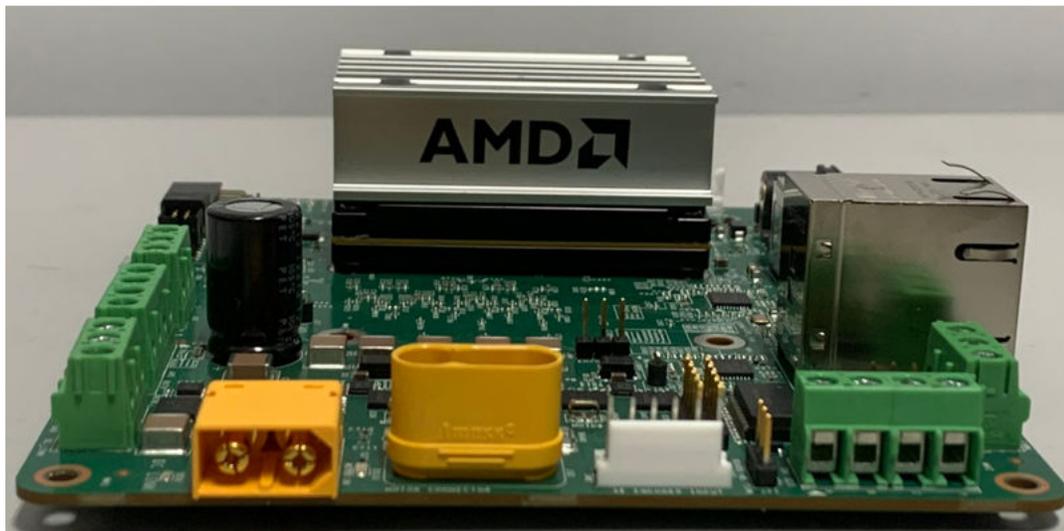
*Figure 34: Fully Engaged Connector (K24 SOM on Carrier Card)*



### Completely Mated KD240 Board

The following images show a complete, assembled KD240 carrier card.

*Figure 35: KD240 Front View*



*Figure 36: KD240 Side View*

## SOM System B2B Connector Assembly Validation-DOE (To Ensure Time 0 No Crack)

The Samtec ADF and ADM connectors placement were shifted 0% and 15% (based on connector pad diameter) on the X and Y-axis for both the SOM and carrier cards. The shifted connectors were reflowed and were able to mate without any issue.

The mated connector boards were submitted for cross section testing to validate their mating conditions. Based on the cross-section images, the connectors which shifted by 15% were able to self-align during reflow soldering. The following photos are a cross section image of the mated connectors. The proper contact of the female and male connector pins is achieved.

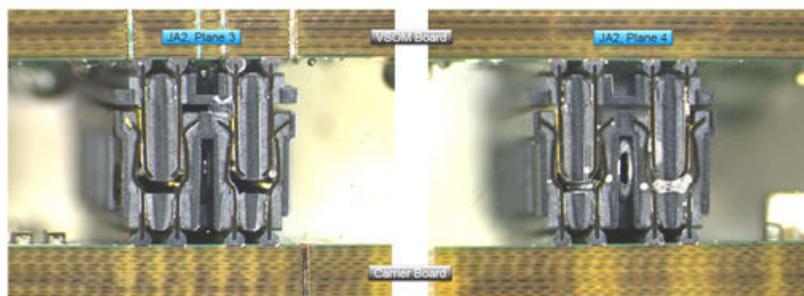
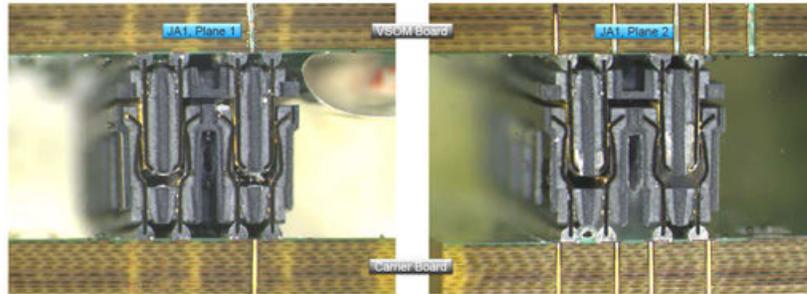
*Figure 37: Cross-section Image of Mated Connectors for 0% Shift*

Figure 38: Cross-section Image of Mated Connectors for 15% Shift



# Hardware Configuration Using Vivado Tools

The following section provides an overview of the AMD Vivado™ Design Suite carrier card hardware design support.

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## Vivado Tools Board Files

The Vivado tools board files provides a design abstraction to capture aspects of the hardware configuration that are fixed by the SOM physical hardware design. The board files, when combined with the Vivado tools board automation, can pre-populate the MIO configuration associated with these SOM fixed peripherals:

- DDR memory interface and associated timing configuration
- QSPI non-volatile memory and associated clocking
- eMMC non-volatile memory and associated clocking
- SPI interface for a trusted platform module (TPM)
- I2C peripheral bus for SOM peripherals and extensible via carrier card design
- UART for board bring-up and software debug (assumes the carrier card pins out MIO36 and MIO37 for proper UART function)
- PMU input/output (need to check default board file configuration)

Vivado tools board files are available for each SOM on the AMD GitHub [Board Store](#) and can be installed either by default installation or via installation from the XHUB store.

Documentation on installing and using the Vivado tools board files is available in the [SOM Wiki](#).

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## Vivado Software SOM Connector Abstraction

The SOM board files introduce a SOM connector abstraction that allows the hardware configuration to focus on SOM connector level physical mapping. This is intended to help eliminate the need for the carrier card designer to have to create a physical pin translation table.

The SOM connector infrastructure uses the convention of: `<connector name> + <_> + <connector_pin_number>`. For example, a SOM connector pin name of `som240_1_c18` refers to the pin C18 of the SOM240\_1 connector. Using this convention and the XDC `get_ports` functionality, a carrier card constraints file can be described in terms of a SOM physical interface when combined with a SOM constraint file that captures the AMD Zynq™ UltraScale+™ MPSoC to SOM connector pin definition.

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## SOM Vivado Tools XDC Files

The SOM Vivado board file includes an XDC file that captures the Zynq UltraScale+ MPSoC package mapping to SOM connector pin definitions. This file can be used by the carrier card designer to identify the full SOM plus carrier card design constraints.

# Additional Resources and Legal Notices

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## Finding Additional Documentation

### Technical Information Portal

The AMD Technical Information Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Technical Information Portal, go to <https://docs.amd.com>.

### Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help** → **Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools** → **DocNav**.
- At the Linux command prompt, enter `docnav`.

**Note:** For more information on DocNav, refer to the *Documentation Navigator User Guide* ([UG968](#)).

### Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the [Design Hubs](#) web page.

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## Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Support](#).

---

## References

These documents provide supplemental material useful with this guide:

1. *Kria K26 SOM Data Sheet* ([DS987](#))
2. *Kria K24 SOM Data Sheet* ([DS985](#))
3. *Kria K26 SOM Thermal Design Guide* ([UG1090](#))
4. *Kria K24 SOM Thermal Design Guide* ([UG1094](#))
5. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* ([DS925](#))
6. *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#))
7. *UltraScale Architecture PCB Design User Guide* ([UG583](#))
8. *Zynq UltraScale+ Device Technical Reference Manual* ([UG1085](#))
9. *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* ([UG1075](#))
10. *Bootgen User Guide* ([UG1283](#))
11. *UltraScale Architecture System Monitor User Guide* ([UG580](#))
12. *UltraScale Architecture GTH Transceivers User Guide* ([UG576](#))
13. Associated files:
  - a. *Kria SOM Carrier Connector Compatibility Overlay* ([XTP785](#))
  - b. *Kria K26 SOM 3D CAD Model* ([XTP680](#))
  - c. *Kria K24 SOM 3D CAD Model* ([XTP777](#))
  - d. *Kria K26 SOM Trace Delay File* ([XTP688](#))
  - e. *Kria K24 SOM Trace Delay File* ([XTP779](#))
  - f. *Schematic review checklist for Kria SOM carrier card designs* ([XTP748](#))
14. *Kria SOM K24 - Known Issues and Release Notes Master Answer Record*
15. *Kria SOM K26 - Known Issues and Release Notes Master Answer Record*

# Revision History

The following table shows the revision history for this document.

Section	Revision Summary
<b>9/18/2025 Version 1.6</b>	
<a href="#">Figure 7: K24 SOM Dimensions</a>	Updated the hole dimension to M2.5(4x) in the top view.
<a href="#">Power Sequencing</a>	Updated section with information on power up and power down sequencing.
<b>11/03/2023 Version 1.5</b>	
General	Added KD24 SOM information to guide. Removed the connector specific pinouts and signal naming conventions. See the specific SOM data sheet for that information.
<a href="#">Chapter 1: Introduction</a>	Removed the <i>K26 SOM Block Diagram</i> . See the <i>Kria K26 SOM Data Sheet (DS987)</i> .
<a href="#">SOM Connector Overview</a>	Added Connector Compatibility Across Kria SOMs discussion.
<a href="#">SOM Connector Power Pins</a>	Removed the <i>SOM Power Rails</i> table and linked to the SOM specific data sheets.
<b>5/25/2023 Version 1.4</b>	
General	Updated information on MIO banks for MIO[31] (MIO31_PMU_GPI) and MIO[35] (MIO35_PMU_GPO).
<a href="#">Sideband Signals</a>	Updated the PS_POR_L signal description.
<a href="#">Board to Board Connector PCB Layout for K26 SOM</a>	Updated to clarify images in <a href="#">Figure 14: SOM240 Connector Pad Requirements on K26 Carrier Card (Top View)</a> and <a href="#">Figure 15: K26 Keep Out Requirements on K26 Carrier Cards (Top View)</a> .
<a href="#">References</a>	Updated reference section.
<b>7/27/2022 Version 1.3</b>	
General	Added reference to the REF-226081 Samtec connector throughout data sheet.
<a href="#">SOM Configuration and Control Signals</a>	Updated descriptions in <a href="#">Power-on Reset (PS_POR_B) Signal</a> and PS_POR_L.
<a href="#">Power Management Signals</a>	Updated the PWRGD_LPD_M2C signal description.
<b>3/16/2022 Version 1.2</b>	
<a href="#">Chapter 1: Introduction</a>	Updated the <i>K26 SOM Block Diagram</i>
Signal Naming Conventions	Added Table 3: Legend for Pin Types. Added signal to connector mapping using XDC file discussion.
SOM240_1 Signal Names and Descriptions	Added the pin type column and updated the descriptions for B28 (MIO35), B29 (MIO36), B30 (MIO37), C30 (MIO29), and C31 (MIO30), and C32 (MIO31).
SOM240_2 Connector Pinout	Updated A4 description.
SOM240_2 Signal Names and Descriptions	Added the pin type column.
<a href="#">Supported I/O Standards</a>	Added power-up and configuration information.
<a href="#">PS-GTR Transceivers</a>	Added additional transceiver details.

Section	Revision Summary
<a href="#">GTH Transceivers (K26 SOM only)</a>	Added additional transceiver details.
<a href="#">Transceiver Reference Clocks</a>	Added additional transceiver details.
<a href="#">SOM Configuration and Control Signals</a>	Clarifying edits to <a href="#">PS_ERROR_OUT Signal</a> , <a href="#">PS_ERROR_STATUS Commands</a> .
<a href="#">Power Management Signals</a>	Updated descriptions on the signals in this section.
<a href="#">SOM MIO Design Considerations</a>	Updated mapping instructions and bank diagrams.
<a href="#">K26 SOM Mechanical Dimensions</a>	Added clarifying edits to the <a href="#">Figure 6: K26 SOM Dimensions</a> mechanical drawing.
<b>7/23/2021 Version 1.1</b>	
<a href="#">Chapter 1: Introduction</a>	Updated the <i>K26 SOM Block Diagram</i> .
<a href="#">SOM240_1 Connector Pinout</a>	Updated MIO35_WD_OUT and MIO26.
<a href="#">SOM240_1 Signal Names and Descriptions</a>	Updated descriptions in table.
<a href="#">SOM240_2 Connector Pinout</a>	Corrected errors in table.
<a href="#">SOM240_2 Signal Names and Descriptions</a>	Updated descriptions in table.
<a href="#">Supported I/O Standards</a>	Added description of XCK26 device.
<a href="#">SOM I/O Timing Model</a>	Added information on designing with trace length and signal delays, and removed Table 7: K26 SOM PCB Signal Delays by I/O Bank
<a href="#">Sideband Signals</a>	Added PS_REF_CLK and PS_PAD_I/O.
<a href="#">SOM Connector Power Pins</a>	Updated the V <sub>BATT</sub> recommended conditions in <i>SOM Power Rails</i> . Added discussion on connecting unused I/O bank VCCO pins.
<a href="#">Power Management</a>	Added further details on power management and PWRGD signals.
<a href="#">SOM Power Estimation</a>	Added link to <i>Kria K26 SOM Thermal Design Guide (UG1090)</i> .
<a href="#">Carrier Card Board to Board Connector Placement Guideline for K26 SOM</a>	Corrected Samtec mating connector model (ADM6-60-01.5-L-4-2-A).
<a href="#">References</a>	Added link to <i>Kria K26 SOM Thermal Design Guide (UG1090)</i> .
<b>4/20/2021 Version 1.0</b>	
Initial release.	N/A

## Please Read: Important Legal Notices

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