Recommended Design Rules and Strategies for BGA Devices

User Guide

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Chapter 1

Introduction

Xilinx® Versal® architecture, UltraScale™ architecture, 7 series, and 6 series devices come in a variety of packages that are designed for maximum performance and maximum flexibility. Four pitch sizes are available for these packages: 1.0 mm, 0.92 mm, 0.8 mm, and 0.5 mm. In general, as the pitch size decreases, the challenges for PCB routing increase as there is less room to route traces and vias between package balls. This guide illustrates various methods for successful design regardless of pitch size.

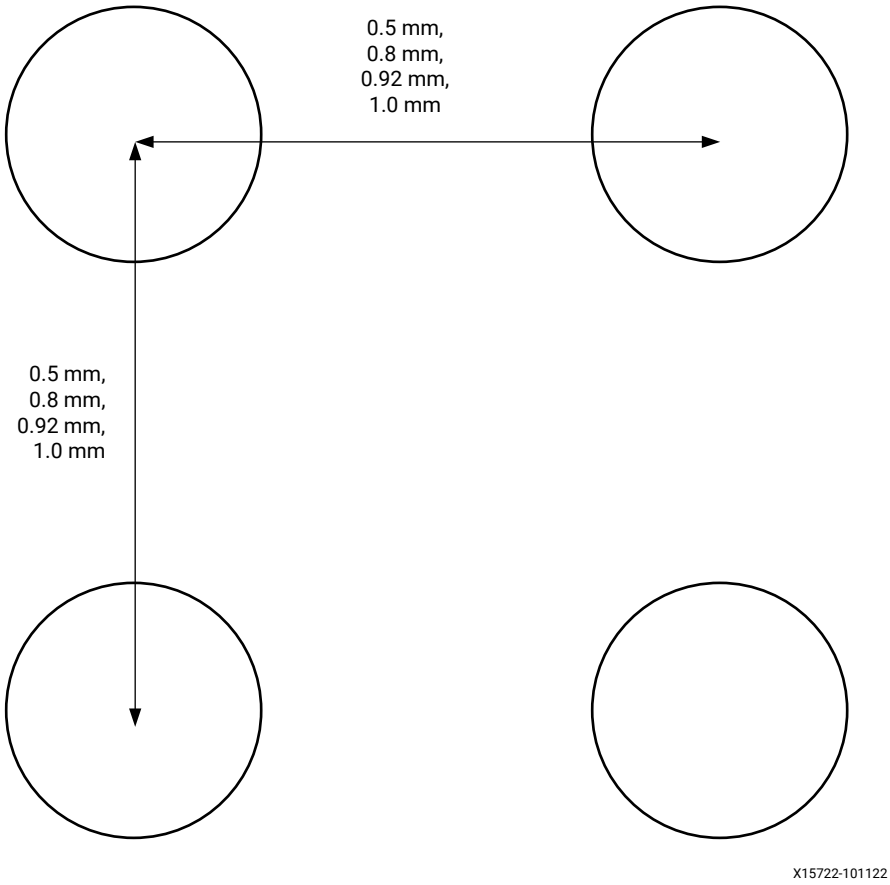
Note: *Throughout this guide, various specifications and estimates are given regarding PCB pricing, costs, and technology. As PCB manufacturing technology is constantly advancing, it is highly advised to consult with your PCB manufacturer to fully understand their capabilities regarding the information presented here.*

General BGA and PCB Layout Overview

The primary factor that determines the intricacy of BGA routing is the pitch size. In addition, factors such as the size of the BGA array, type of solder masks used, and layer count requirements also play crucial factors.

Pitch size is defined as the distance between consecutive balls on a BGA package, measured from center-to-center, as shown in the following diagram.

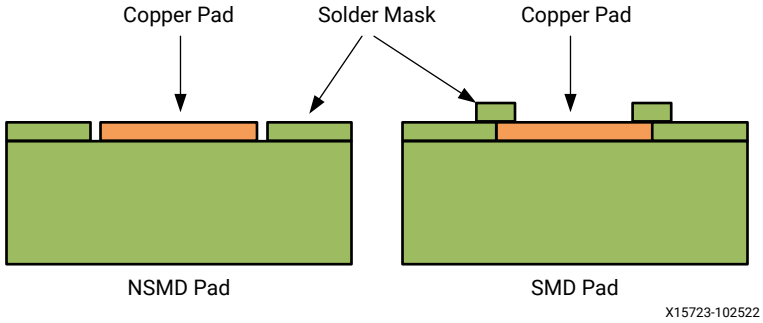
Figure 1: **Definition of Pitch Size**



BGA Landing Pads

Xilinx recommends using non-solder mask-defined (NSMD) copper BGA landing pads for optimum board design. NSMD pads are pads that are not covered by any solder mask, as opposed to Solder Mask Defined (SMD) pads in which a small amount of solder mask covers the pad landing. The following figure illustrates the difference between NSMD and SMD pads.

Figure 2: **NSMD and SMD Pads**



Layer Count Estimation and Optimization

Layer Count Estimation

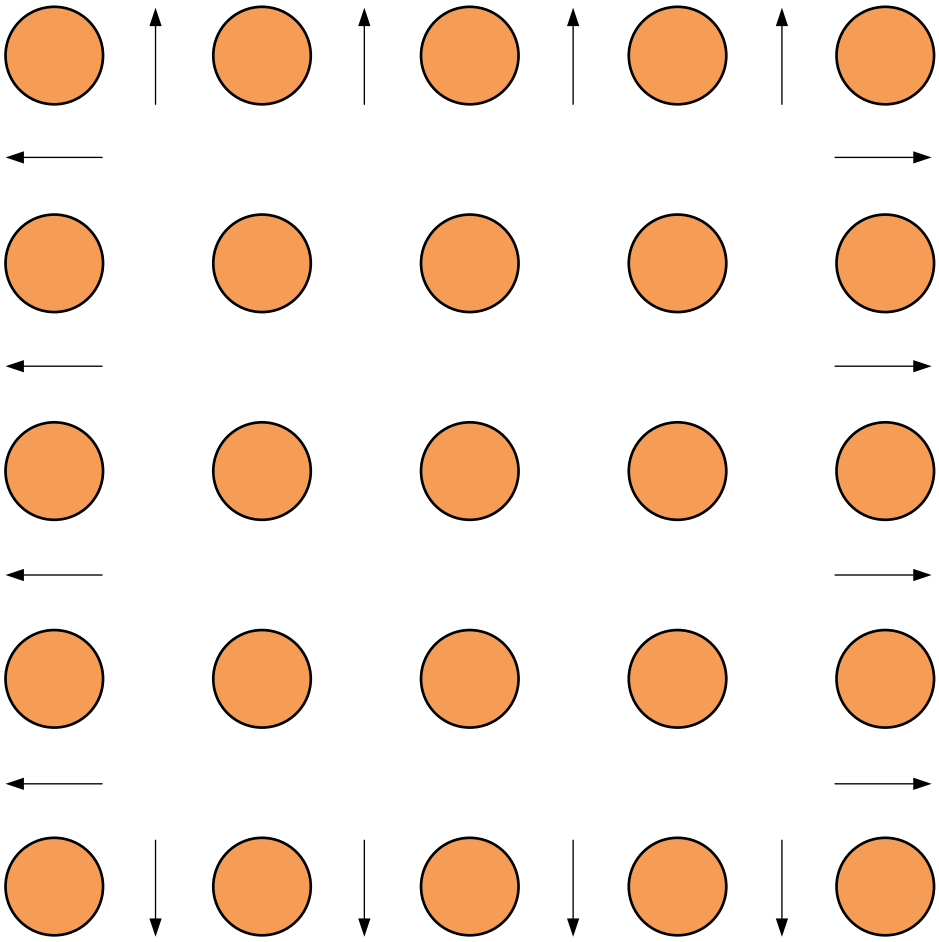
A quick way to estimate the number of *signal* routing layers required to fully break out signal pins from the FPGA would be to use the following equation:

$$Layers = \frac{Signals}{Routing\ Channels\ x\ Routes\ Per\ Channel}$$

For Xilinx® FPGAs, MPSoCs/RFSoCs, and ACAPs, the quantity of signals is approximately 60% of the number of BGA balls. The other 40% are power and ground signals that are most often routed directly down to their own dedicated planes by vias. The equation assumes full I/O utilization. If fewer I/Os are used, the number of signals to route goes down accordingly.

Routing channels are the number of available routing paths out of the BGA area (the number of BGA pins on one side minus one, times four sides). The following figure shows a 5x5 grid with sixteen total routing channels (four routing channels per side times four sides).

Figure 3: **Definition of Routing Channel**



(16 Total Routing Channels Shown)

Routes per channel is either one or two, depending on whether one or two signals are routed between BGA pads. The approximate number of signal layers required to fully route out a Xilinx FPGA or ACAP are shown in the following table.

Table 1: **Approximate Signal Layers per no. of Package Pins**

BGA Pins	Ball Pitch (mm)	Routing Channels	Estimated Signal Layers Required with All Available I/Os Routed	
			One Trace Per Routing Channel	Two Traces Per Routing Channel
196	0.5	52	2	1
196	1.0	52	2	1
225	0.8	56	2	1
236	0.5	56	3	1
238	0.5	56	3	1

Table 1: **Approximate Signal Layers per no. of Package Pins** *(cont'd)*

BGA Pins	Ball Pitch (mm)	Routing Channels	Estimated Signal Layers Required with All Available I/Os Routed	
			One Trace Per Routing Channel	Two Traces Per Routing Channel
256	1.0	60	3	1
324	0.8	68	3	1
400	0.8	76	3	2
484	0.8/1.0	84	3	2
485	0.8	84	3	2
494	0.5	84	4	2
530	0.5	88	4	2
625	0.8	96	4	2
676	1.0	100	4	2
784	0.8/1.0	108	4	2
900	1.0	116	5	2
1024	0.92	124	5	2
1154	1.0	132	5	3
1155	1.0	132	5	3
1156	1.0	132	5	3
1157	1.0	132	5	3
1365	0.92	144	6	3
1369	0.92	144	6	3
1517	1.0	152	6	3
1596	0.92	156	6	3
1759	1.0	164	6	3
1760	0.92/1.0	164	6	3
1761	1.0	164	6	3
1923	1.0	172	7	3
1924	1.0	172	7	3
1925	1.0	172	7	3
1926	1.0	172	7	3
1927	1.0	172	7	3
1928	1.0	172	7	3
1930	1.0	172	7	3
2104	1.0	180	7	4
2197	0.92	184	7	4
2377	1.0	188	8	4
2577	1.0	200	8	4
2785	0.92	208	8	4
2892	1.0	212	8	4

Table 1: **Approximate Signal Layers per no. of Package Pins** *(cont'd)*

BGA Pins	Ball Pitch (mm)	Routing Channels	Estimated Signal Layers Required with All Available I/Os Routed	
			One Trace Per Routing Channel	Two Traces Per Routing Channel
3340	0.92	228	9	4
3824	1.0	244	9	5
4072	1.0	252	10	5
5601	0.92	296	11	6

Layer Count Optimization

Versal® architecture, UltraScale™ architecture, 7 series, and 6 series packages have full matrices of solder balls. The true number of layers required for effective routing of these packages is dictated by a variety of factors, including:

- BGA Size (quantity of pins)
- Pad size, pad pitch, and trace width
- Fixed pinouts
- Back Drilling
- Fabrication Technologies

BGA Size

The quantity of pins in a BGA indicates the number of signals to route. Because of physical space constraints, the quantity of signals required to route is proportional to the amount of signal layers required.

Pad Size, Pad Pitch, and Trace Width

The pad size and pitch determine the available space between adjacent balls for signal escape. Based on the chosen trace width, one or two signals can be routed between adjacent pads. If one signal escapes between adjacent pads, then one signal row can be routed on a single metal layer. The exception to this is the outermost row, which allows two routes per layer.

To facilitate routing in the ball grid area, *necking down* the trace width in the critical space between the BGA pads/vias (the breakout area) is allowable. This then allows for two signal rows to be routed on a single metal layer (or three if routing the outermost row). The traces can then be widened after they escape the breakout area. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for the design.

Fixed Pinouts

Xilinx FPGA and ACAP pinouts are designed with maximum flexibility in mind. However, certain FPGA/ACAP signals, such as JTAG, transceiver inputs and outputs, and memory controller signals (among others) have fixed locations, which means routing of these signals is limited compared to other signals that can be swapped as needed. Fixed locations lead to layout trade-offs that can have an impact on the number of required signal layers.

Back Drilling

Back drilling is the technique is which unused via stubs have their metal drilled away to remove the potential for the stubs to cause reflections which can cause signal integrity problems. Typically, back drilling can prevent the ability to route more than one signal in-between pads and vias due to manufacturability concerns. Always consult with the PCB manufacturer regarding the ability to back drill before beginning and layout activity.

Fabrication Technologies

Several advanced fabrication technologies can be used to reduce the number of layers required to route a design, although each of these technologies increase fabrications costs of the board:

Blind Vias (+20% to +40% fabrication cost)

As opposed to a through-hole via, a blind via does not travel from the top layer to the bottom layer. A blind via travels either from the top or bottom layer to an inner signal layer, freeing up room above or below for other routing.

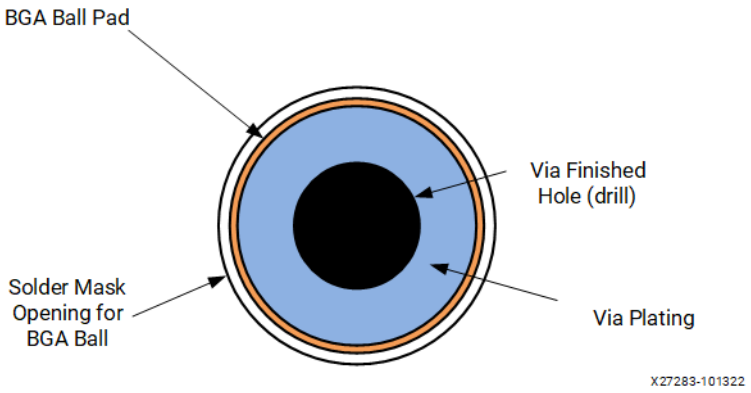
Buried Vias (+25% to +60% fabrication cost)

A buried via is located entirely inside the printed circuit board and does not touch the top or bottom layers.

Via-in-Pad (+10% to +20% fabrication cost)

Via-in-pad technology is where a via is placed directly over a BGA pad, reducing the need to*dog-bone* the signal trace on to the top or bottom layer. This allows for easier escape routing under the BGA as the signal can travel directly down to another layer from the pad. In addition, the impedance of the signal is better improved by not having any portion of it on the top or bottom routing layers. The following figure illustrates the mechanical design of a Via-in-pad.

Figure 4: **Via-In-Pad Structure**



Maximum Board Thickness and Aspect Ratio

The maximum board thickness is a function of the minimum drill diameter and aspect ratio, both of which are provided by the PCB manufacturer. A typical aspect ratio of 15:1 indicates that the board can be no thicker than fifteen times the drill diameter. A drill diameter of 10 mils, for example, would lead to a maximum board thickness of 150 mils. Apart from the CP package, Xilinx recommends finished drill diameters to be 10-15 mils, which translates to an actual drill diameter of about 13-18 mils (plating typically reduces the diameter by about 3 mils). A 10 mil drill would lead to a maximum board thickness of 100 mils for a 10:1 ration, or 150mils for a 15:1 ratio. Advanced manufacturing technologies can support from 17:1 to 22:1 ratio, but at increased costs.

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Chapter 4

Recommended BGA Ball Pad, Via, and Trace Dimensions for 1.0mm, 0.92mm, 0.8mm, and 0.5mm Devices

Note: The figures in this chapter assume that signals are routed from the BGA ball to a via in a *dog-bone* configuration where the signal from the BGA routes diagonally from the pad to a via on the same routing layer. Via-In-Pad (VIP) technology (see the Via-In-Pad Structure figure in Fabrication Technologies) can be used to place a via directly on top of a BGA pad so it can travel straight down to an inner signal layer.

Recommended BGA Ball Pad and Via Dimensions for 1.0 mm, 0.92 mm, 0.8 mm, and 0.5 mm Devices

The definition of dimensions of FPGA/ACAP ball pads and vias for Xilinx® BGA devices are show in the following figure. The table that follows shows the actual dimensions based on BGA ball pitch.

Figure 5: **BGA Ball and Via Definition of Dimensions**

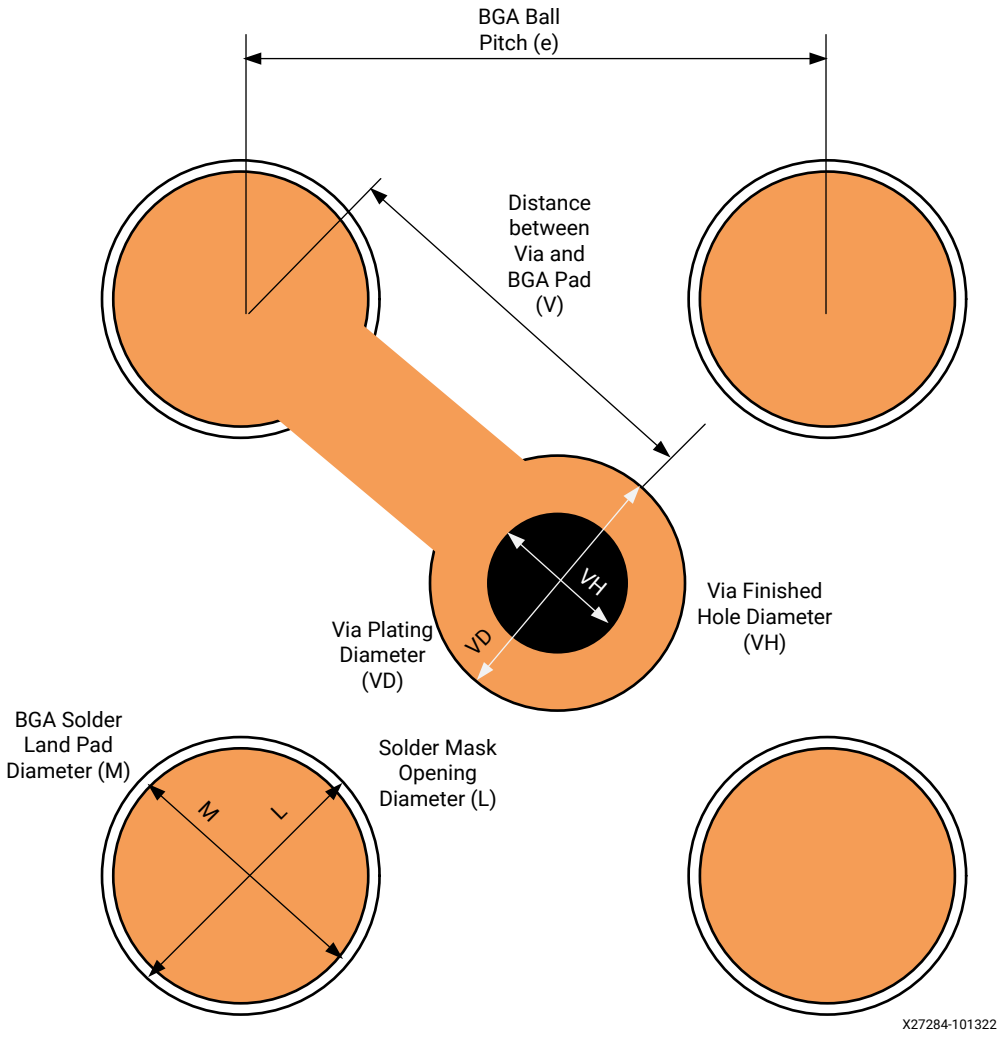


Table 2: **BGA Ball and Via Dimensions**

Solder Ball Land Pitch (e)	1.0 mm	0.92 mm	0.8 mm	0.5 mm
Solder Mask Opening Diameter (M)	20.9 mil	20.9 mil	15.7 mil	11.0 mil
	0.53 mm	0.53 mm	0.40 mm	0.28 mm
PCB Solder Land Diameter (L)	19.7 mil	20.0 mil	15.7 mil	10.2 mil
	0.50 mm	0.51 mm	0.40 mm	0.26 mm
Via Plating Diameter (VD)	19 mil	19 mil	19 mil	10 mil
	0.48 mm	0.48 mm	0.48 mm	0.254 mm
Via Finished Hole Diameter (VH)	10 mil	10 mil	10 mil	4 mil
	0.25 mm	0.25 mm	0.25 mm	0.10 mm
Distance between BGA Pad and Via)	27.83 mil	25.61 mil	22.27 mil	13.92 mil
	0.70 mm	0.65 mm	0.56 mm	0.35 mm

Recommended Trace Routing between Pads and Vias for 1.0 mm, 0.92 mm, 0.8 mm, and 0.5 mm Devices

The ball pitch and BGA pad/via diameters determine how much space is available to route traces between pads or vias. Standard PCB processes can allow for as low as 3.5 mil trace widths with 3.5 mil spacing. Advanced processes can allow for as low as 2 mil trace widths with 2 mil spacing. Recommended trace routing is shown in the following figure. The table that follows shows the actual BGA/trace routing dimensions.

Figure 6: **BGA/Trace Routing Dimensions**

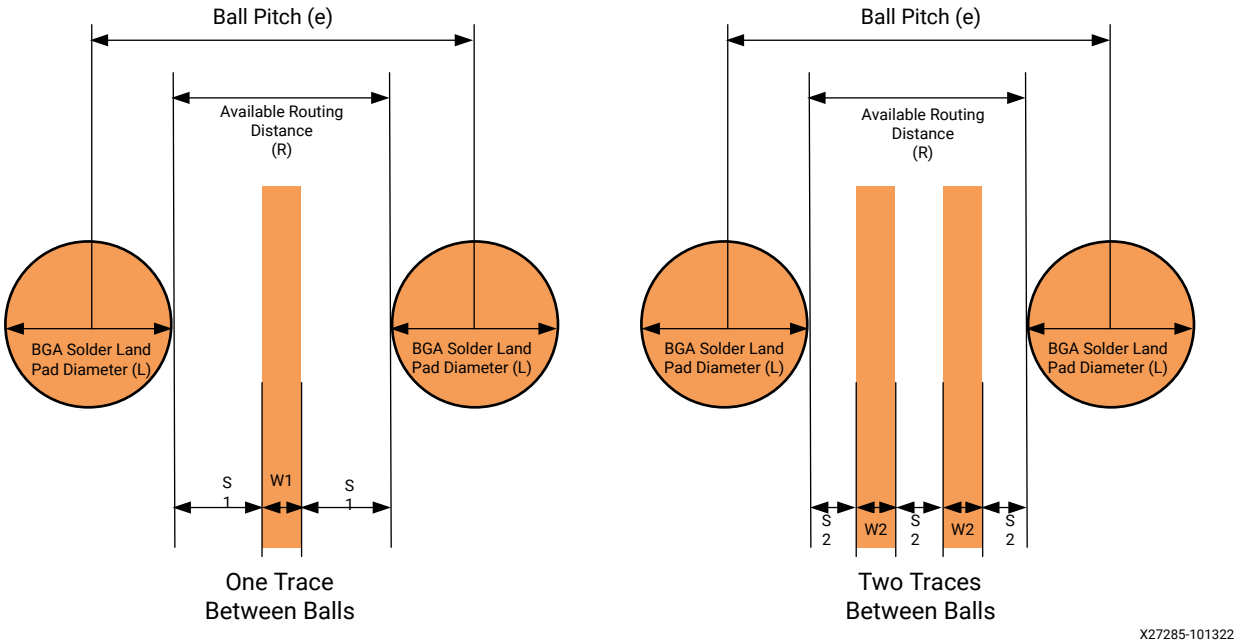


Table 3: **BGA/Trace Routing Dimensions**

Solder Ball Land Pitch (e)	39.39 mil	36.22 mil	31.40 mil	19.7 mil
	1.0 mm	0.92 mm	0.8 mm	0.5 mm
PCB Solder Land Diameter (L)	19.7 mil	20.0 mil	15.7 mil	10.63 mil
	0.50 mm	0.51 mm	0.40 mm	0.27 mm
Available Routing Distance (R)	19 mil	16 mil	15 mil	9 mil
	0.33 mm	0.40 mm	0.38 mm	0.23 mm
Pad-to-Trace/Trace-to-Trace Spacing for one route between pads (S1)	7.5 mil	6 mil	5 mil	3[1]
	0.19 mm	0.15 mm	0.13 mm	0.08 mm
Trace thickness for one route between pads (W1)	4	4	4	3
	0.10 mm	0.10 mm	0.10 mm	0.08 mm
Pad-to-Trace/Trace-to-Trace Spacing for two route between pads (S2)	4 mil	3 mil	3 mil	N/A
	0.10 mm	0.08 mm	0.08 mm	

Table 3: **BGA/Trace Routing Dimensions** *(cont'd)*

Solder Ball Land Pitch (e)	39.39 mil	36.22 mil	31.40 mil	19.7 mil
	1.0 mm	0.92 mm	0.8 mm	0.5 mm
Trace thickness for two route between pads (W2)	3 mil	3 mil	3 mil	N/A
	0.08 mm	0.08 mm	0.08 mm	

Notes:

1. 3 mil pad-to-trace is not supported by all manufacturers.

Recommended Trace Routing between Vias

One or two traces can be routed in-between vias for 1.0 mm, 0.92 mm, and 0.80 mm pitch devices. It is not practical to route traces in-between vias spaced 0.5 mm apart due to the tight spacing and trace widths required. For those situations, it is recommended to use Via-in-Pad technology for added pitch between vias. Recommended via/trace routing is shown in the following figure. The table that follows shows the actual BGA/trace routing dimensions.

Figure 7: **Via/Trace Routing**

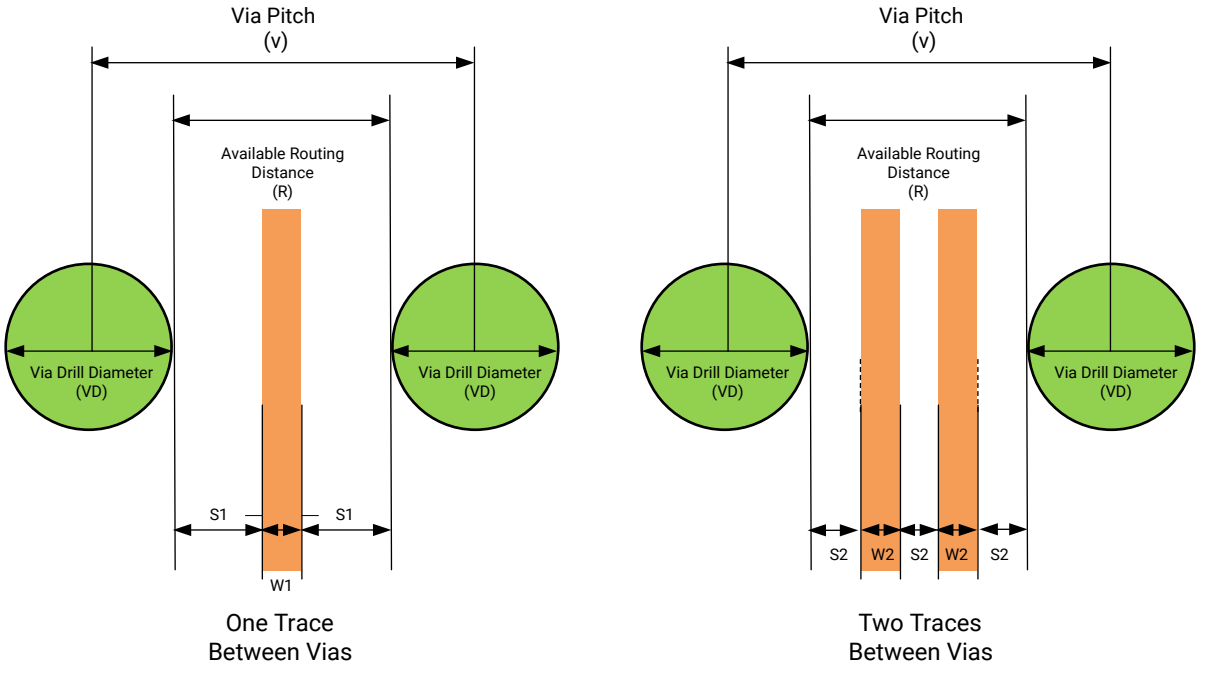


Table 4: **Via/Trace Routing Dimensions**

Solder Ball Land Pitch (e)	39.39 mil	36.22 mil	31.40 mil	19.7 mil
	1.0 mm	0.92 mm	0.8 mm	0.5 mm
Via Drill Diameter (VD)	10 mil	10 mil	10 mil	4 mil
	0.25 mm	0.25 mm	0.25 mm	0.10 mm

Table 4: **Via/Trace Routing Dimensions** *(cont'd)*

Solder Ball Land Pitch (e)	39.39 mil	36.22 mil	31.40 mil	19.7 mil
	1.0 mm	0.92 mm	0.8 mm	0.5 mm
Available Routing Distance (R)	29 mil	26 mil	21 mil	15 mil
	0.74 mm	0.66 mm	0.53 mm	0.38 mm
Via-to-Trace/Trace-to-Trace Spacing for one route between pads (S1)	12 mil	11 mil	8 mil	5 mil
	0.30 mm	0.28 mm	0.20 mm	0.13 mm
Trace thickness for one route between pads (W1)	4 mil	4 mil	4 mil	4 mil
	0.10 mm	0.10 mm	0.10 mm	0.10 mm
Pad-to-Trace/Trace-to-Trace Spacing for two route between pads (S2)	10 mil	6 mil	5 mil	3 mil[1]
	0.25 mm	0.15 mm	0.13 mm	0.08 mm
Trace thickness for two route between pads (W2)	4 mil	4 mil	3 mil	3 mil
	0.10 mm	0.10 mm	0.08 mm	0.08 mm

Notes:

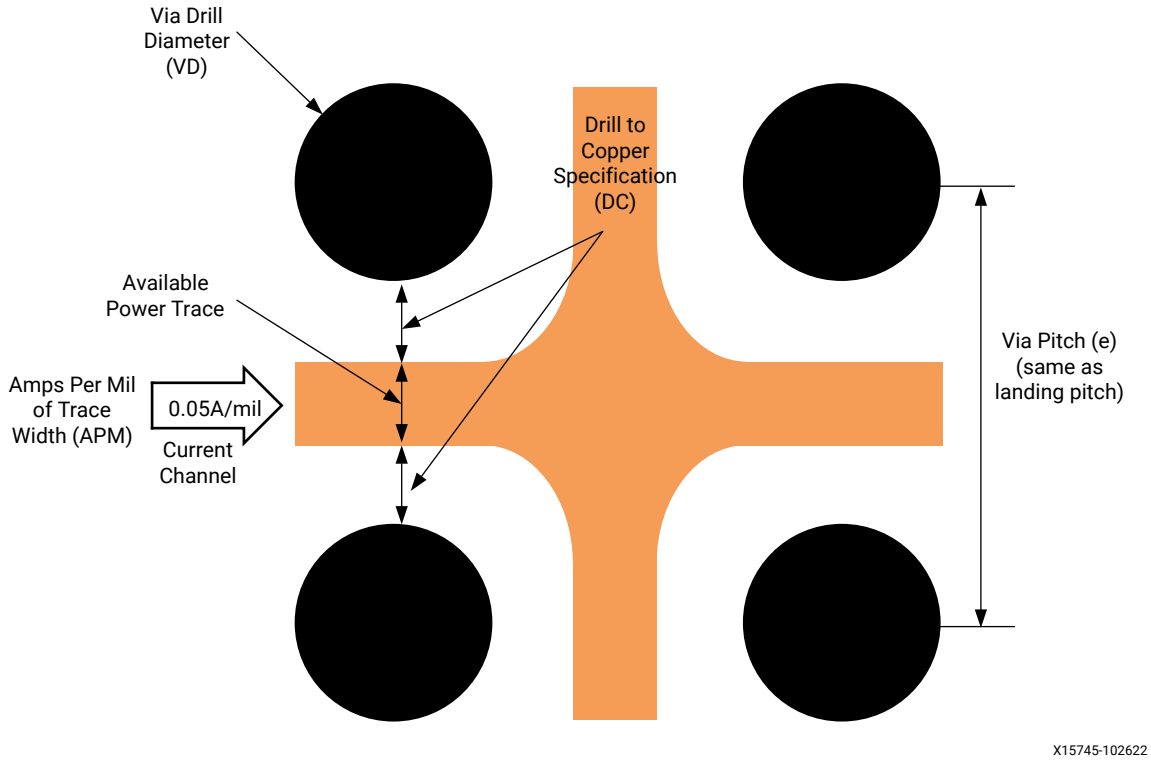
1. 3 mil pad-to-trace is not supported by all manufacturers.

Power Delivery to the FPGA

Power needs must be assessed early in the design phase to assure that there are enough layers and area to provide sufficient power to the BGA balls that require power. Because most of the BGA power pins are located in the center of the BGA area, the path the current travels traverses a myriad of vias in the BGA area. The space between vias can conservatively carry about 0.05A per mil of trace width (for 0.5 oz copper). The trace width between vias is defined by the pitch of the vias (usually the same as the pitch of the BGA), the via drill diameter, and drill-to-copper specification as defined by the fabrication house. The following figure shows how to calculate the amount of current that can pass through each via channel. Ensure that the power planes are wide enough and encompassing enough to supply the needed amperage to the BGA power balls. The following equation can be used to calculate the current per channel:

$$Current\ Per\ Channel = (ViaPitch - ViaDrillDiameter - 2xDrillToCopperSpecification)xAmpsPerUnitTraceWidth$$

Figure 8: **Power Delivery within BGA Area (0.5 oz Copper)**



The following table shows current per channel values for 0.8 mm and 1.0 mm pitch devices. Because of the very fine pitch of 0.5 mm devices, it is not possible to route in-between standard vias. Micro-vias under the BGA pads are recommended for 0.5 mm devices in order to reach the power planes

Table 5: **Current Per Channel Calculation for 0.8 mm, 0.92 mm, and 1.0 mm Devices**

	0.8 mm Pitch	0.92 mm Pitch	1.0 mm Pitch
Via Pitch	31.40 mil	36.22 mil	39.37 mil
Via Drill Diameter	10 mil	10 mil	10 mil
Drill to Copper Specification[1]	8 mil	8 mil	8 mil
Amps per Unit Trace Width (ATW), 0.5 oz Cu	0.05 A	0.05 A	0.05 A
Amps per Unit Trace Width (ATW), 1.0 oz Cu	0.075 A	0.075 A	0.075 A
Current per Channel, 0.5 oz Cu	0.27 A	0.51 A	0.67 A
Current per Channel, 1.0 oz Cu	0.41 A	0.77 A	1.00 A

Notes:

1. Drill-to-Copper of 8 mils is considered standard. Between 6.5 and 8 mil are considered advanced processes.

PCB Routing for Remote Voltage Sense Lines

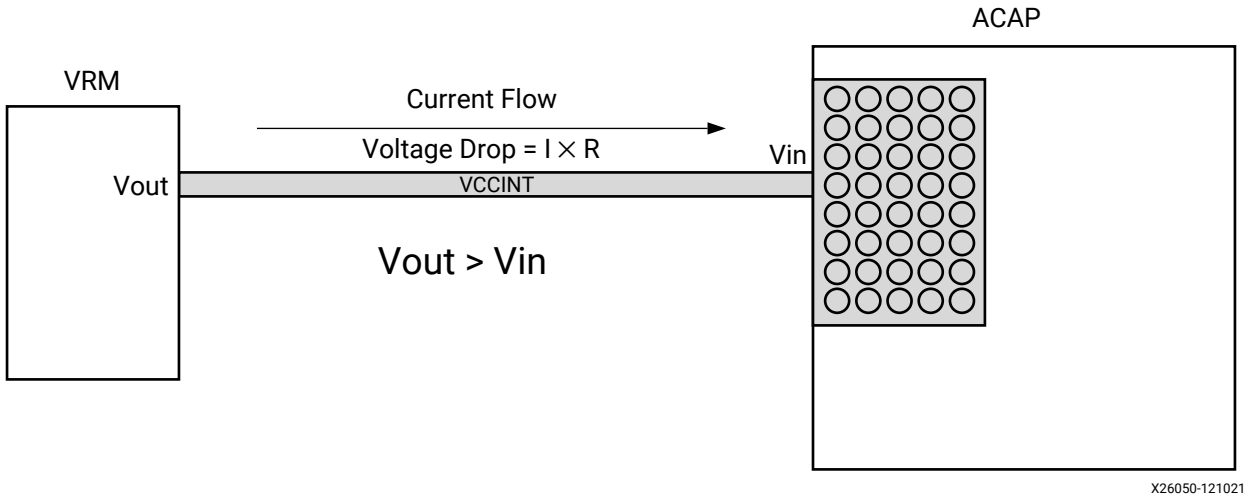
In order to correctly compensate for IR voltage drop across the PCB due to high current loads, proper routing of voltage regulator module (VRM) sense lines is critical for maintaining proper voltage levels at the ACAP die.

***Note*:** Be sure to always follow the sense line recommendations from the VRM vendors because regulator designs, pinouts, and requirements vary.

Purpose of Sense Lines

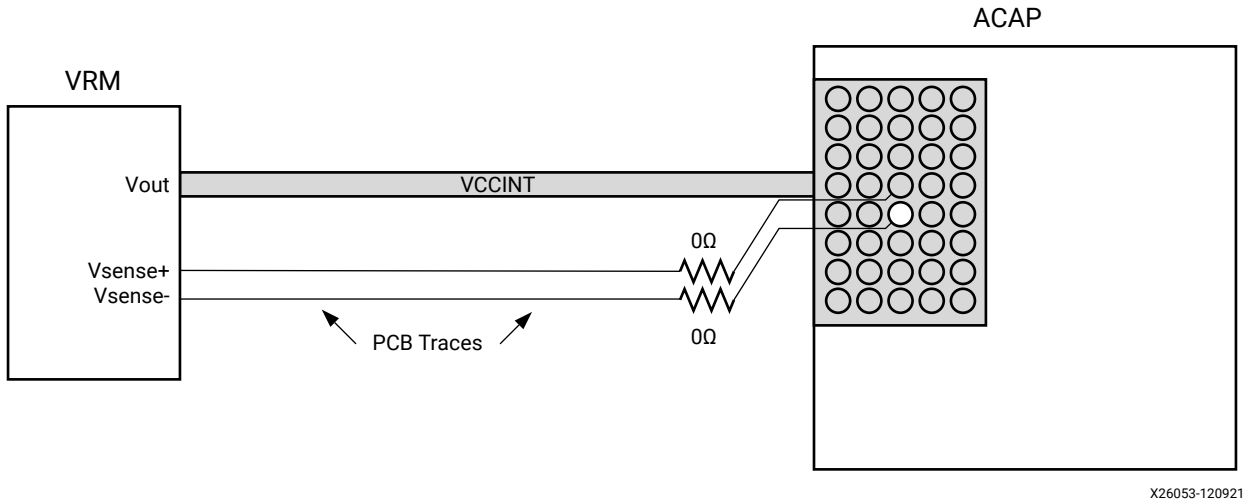
As voltage regulators are often quite a distance away from the devices they supply power to, there is often a DC voltage *IR* drop in voltage between the regulator and the main points-of-load, especially if there is high current load. If the regulator was not accounting for this drop, the voltage at the point-of-load can possibly be quite a bit lower than what the regulator sees. The resulting lower voltage can thus be out of the required limits for proper device operation. The following figure illustrates the direction of current flow and the resulting voltage drop.

Figure 9: **DC Voltage Drop between VRM and Point-of-Load**



To overcome this voltage drop, regulators implement *sense lines* that connect directly from the regulator to the point-of-load. These sense lines are direct traces between the regulator and point-of-load and do not carry any current. Because they do not carry any current, the voltage at the regulator sense pins is exactly the same as seen at the point-of-load. The regulator can thus properly adjust its output voltage as necessary so that the voltage at the point-of-load is within the required specification. The following figure illustrates the placement and routing of sense lines from the VRM to the point-of-load.

Figure 10: **Example of Sense Lines**

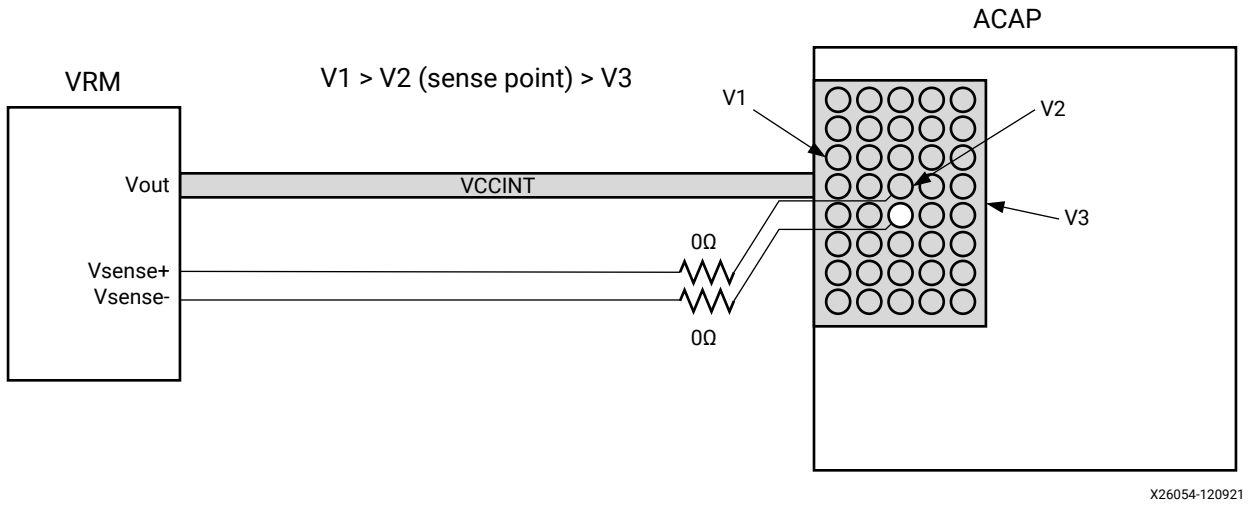


Limitations of Sense Lines

Voltage Disparity

Because sense lines can only be placed at one location at the point-of-load, other areas in front of the sense points might show a higher voltage, while points beyond the point-of-load might see lower voltage. The following figure illustrates this voltage disparity. As the current flows from the VRM to the point-of-load, the voltage at point V1 is higher than the sense point at V2. Likewise, the voltage at point V3 is lower than at the sense point V2.

Figure 11: **Voltages at Various Points in BGA Pin Field**



VRMs with Only One Sense Pin

Some VRMs do not include a sense pin for ground. The primary limitation of this arrangement is that fluctuations in the ground voltage at the point-of-load are not accounted for by the VRM, resulting in less precise voltage regulation.

ACAPs with Dedicated Sense Pins

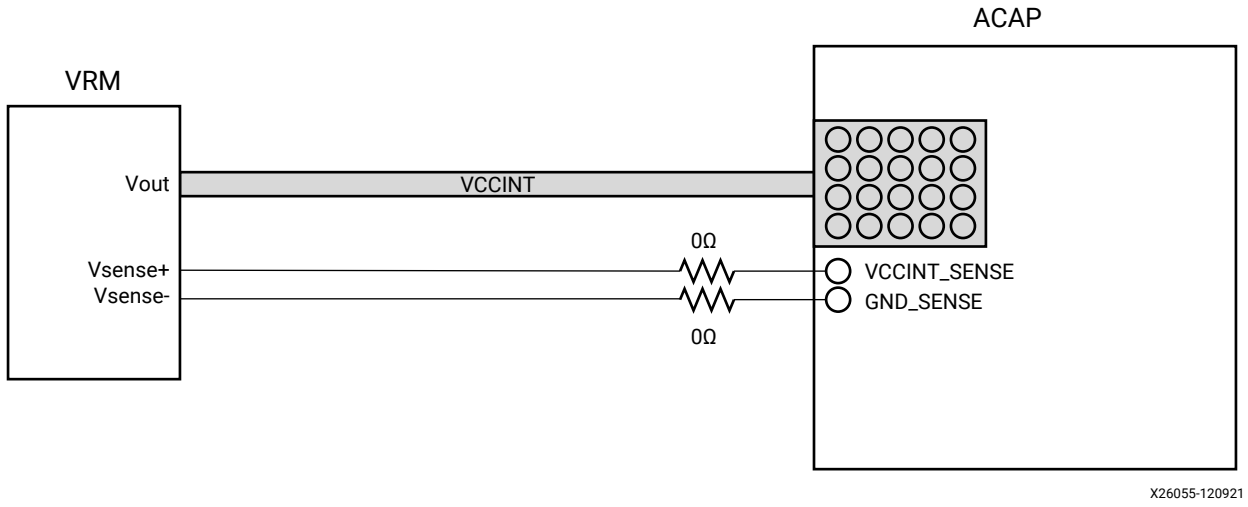
Select Versal ACAPs contain dedicated remote voltage sense pins for VCCINT and its associated ground return. They provide the closest look at the die possible.

The following figure shows recommended sense line routing for ACAPs with dedicated sense pins.

- Place inline 0Ω resistors close to the ACAP:
  - Resistors are required to ensure sense lines are routed as traces and not dropped to the plane.

- Route sense lines as 50Ω loosely coupled differential transmission lines:
  - Ground is required to sense true differential between power and ground.

Figure 12: **Dedicated Sense Pin Routing**



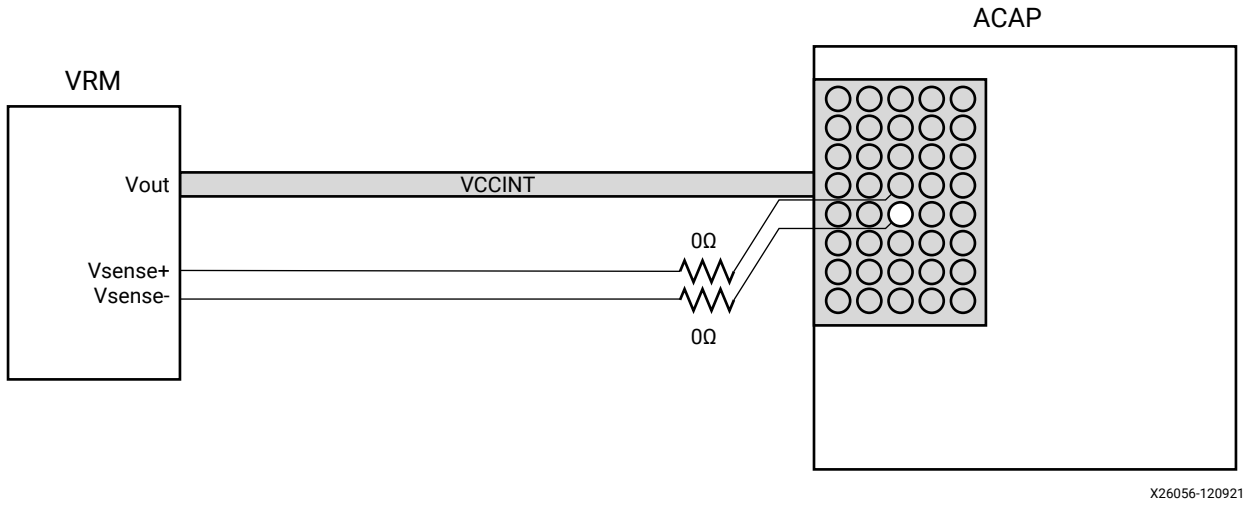
ACAPS without Dedicated Sense Pins

For ACAPs without dedicated sense pins, the sense line connections should connect to BGA balls that are as close as possible to the most significant point-of-load on the ACAP. This can be best estimated via DC simulation or via the device view in the Vivado tools. If the point-of-load cannot be estimated, placing the sense connections towards the center of the BGA pin field is recommended. Placing at the ball furthest from the regulator is also an option, though less preferred.

- Place inline 0Ω resistors close to the ACAP:
  - Resistors are required to ensure sense lines are routed as traces and not dropped to the plane.
- Route sense lines as 50Ω loosely coupled differential transmission lines:
  - Ground is required to sense true differential between power and ground.

For optimum power transfer, ensure that the balls connecting to the sense lines fully connect to their respective planes, i.e., do not leave them unconnected as “spy holes” (see the following figure).

Figure 13: **Sense Pin Routing without Dedicated Sense Pins**

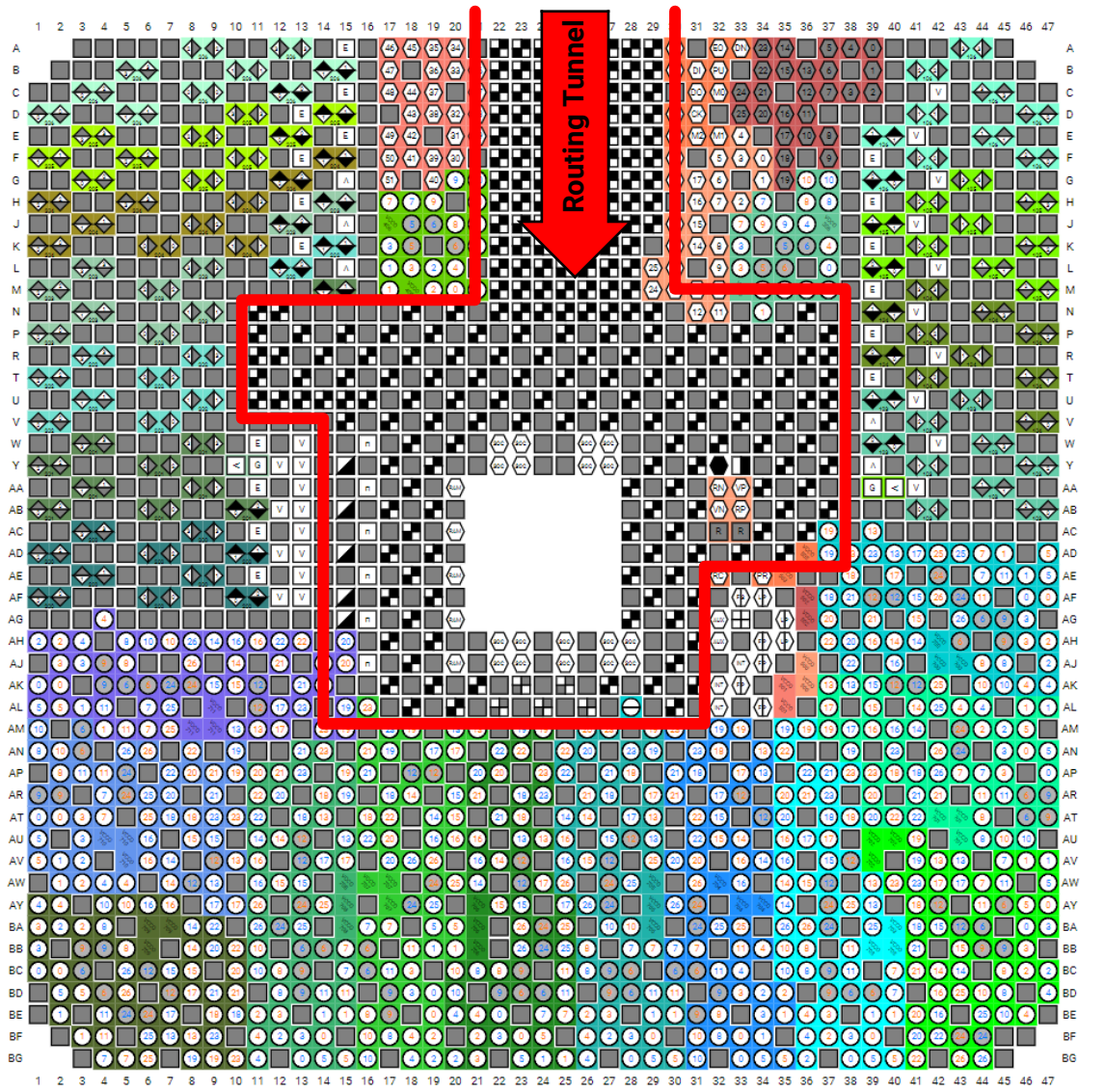


The Use of Routing Tunnels and Sense Lines

Some Versal ACAPs have a dedicated “tunnel” of BGA pins that are specifically placed so as to provide for the maximum amount of power delivery with minimal IR drop. This so-called *routing tunnel* removes via keep-out areas that result in holes in the power plane. The pins in the routing tunnel do not connect directly to the die on the ACAP. These pins are only present so that the PCB routing planes for VCCINT do not require via keep-out holes from other signals or power rails.

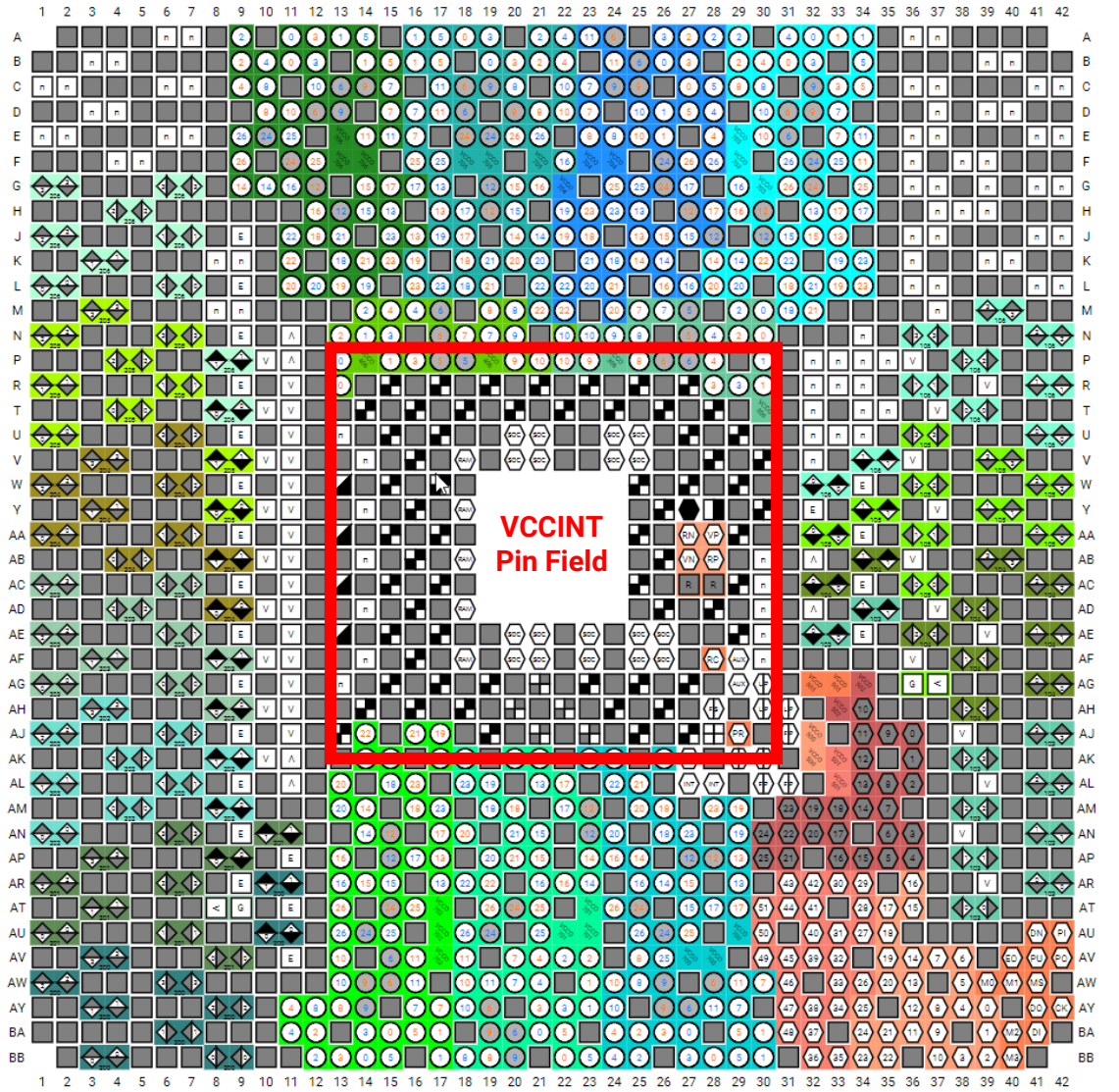
The following figure shows the BGA pin field of the VC1902-A2197 device with the VCCINT pin field outlined. The pins in the routing tunnel area do not require via keep-outs to the VCCINT planes below, so there are no holes in the metal planes that supply power to VCCINT. Optimal sense line placement is at any point on the VCCINT pin field that is outside of the routing tunnel.

Figure 14: **VC1902-A2197 with VCCINT Routing Tunnel**



The following figure shows the BGA pin field of the VM1802-C1760 device with the VCCINT pin field outlined. There is no routing tunnel on this device, so the power planes on the BGA have via keep-outs that reduce power delivery efficiency. Sense line placements would be recommended anywhere near the center of this pin field.

Figure 15: **VM1802-C1760 VCCINT Pin Field**



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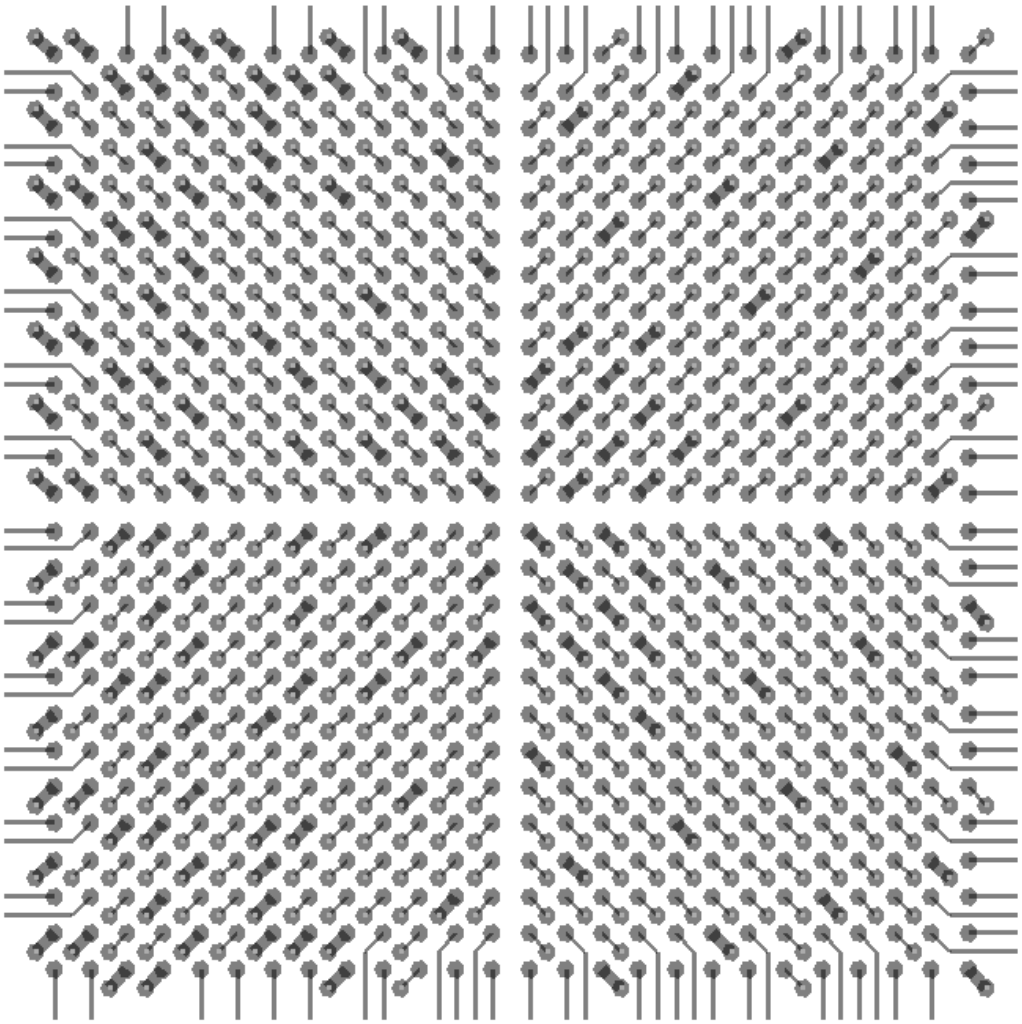
Chapter 6

Sample Breakouts for 1.0 mm, 0.92, and 0.8mm Pitch Devices

The following figures show two example layouts showing the BGA routing breakout areas of a representative 1.0 mm/0.92 mm/0.80 mm pitch Xilinx® device.

Sample Breakout with One Route between BGA Balls and Vias

Figure 16: **Top Layer Breakout (1.0 mm/0.92 mm/0.8 mm), One Route between BGA Balls**



X15861-102622

Figure 17: **Inner Signal Layer One Breakout (1.0 mm/0.92 mm/0.8 mm), One Route between Vias**

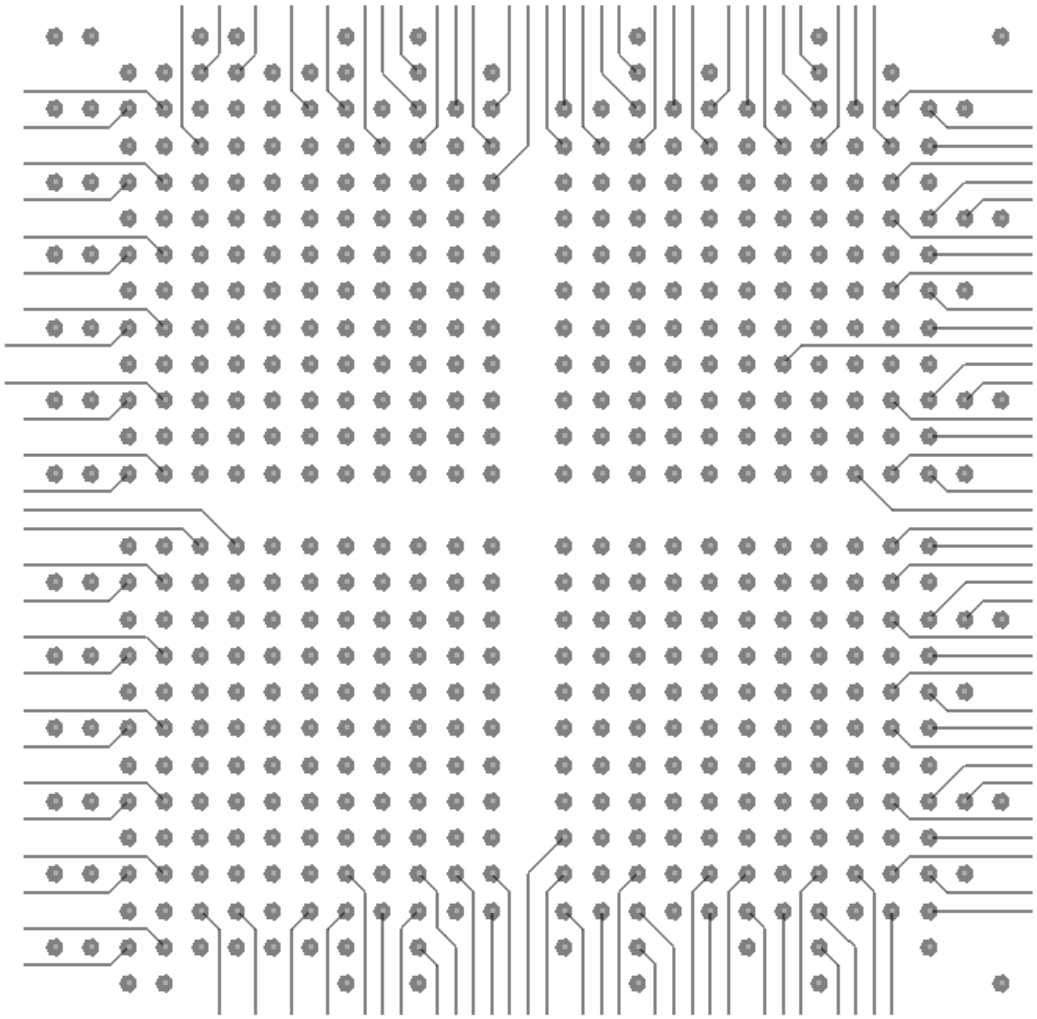


Figure 18: **Inner Signal Layer Two Breakout (1.0 mm/0.92 mm/0.8 mm), One Route between Vias**

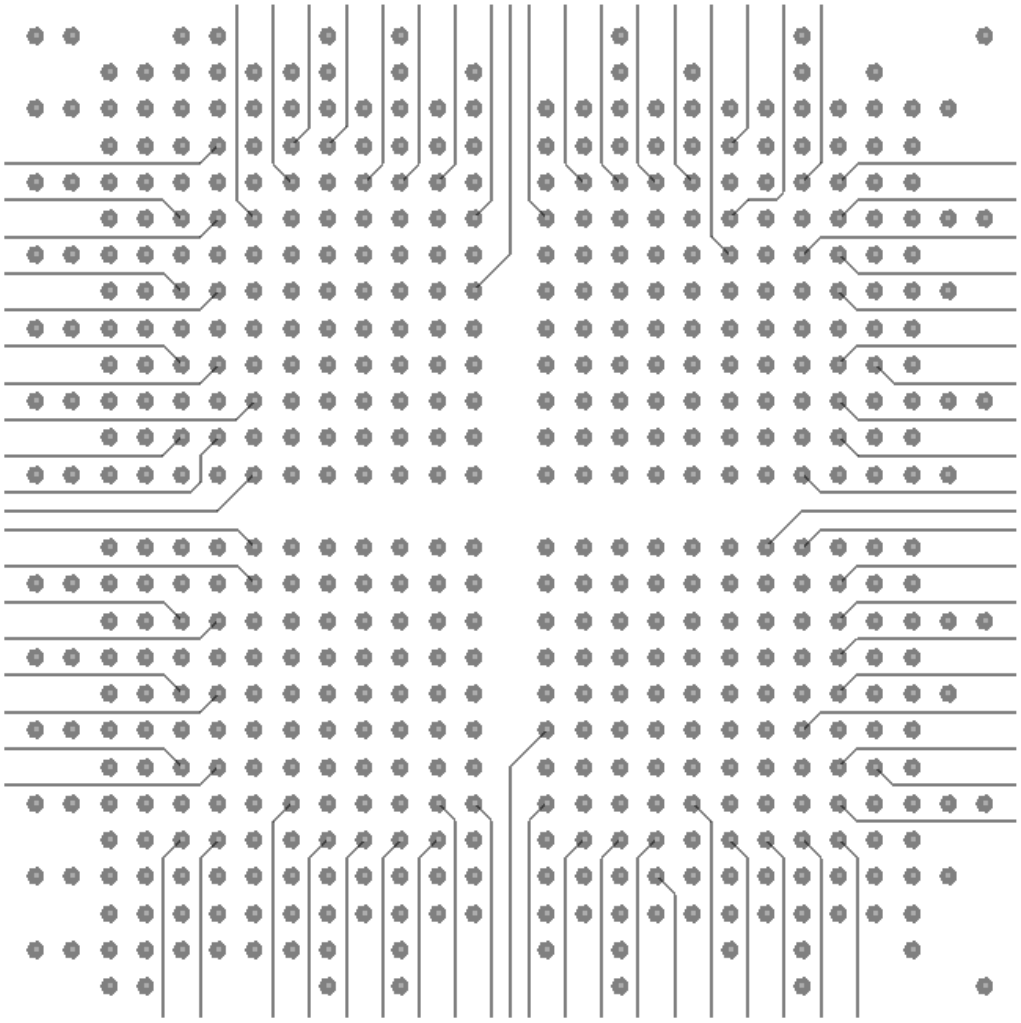


Figure 19: **Inner Signal Layer Three Breakout (1.0 mm/0.92 mm/0.8 mm), One Route between Vias**

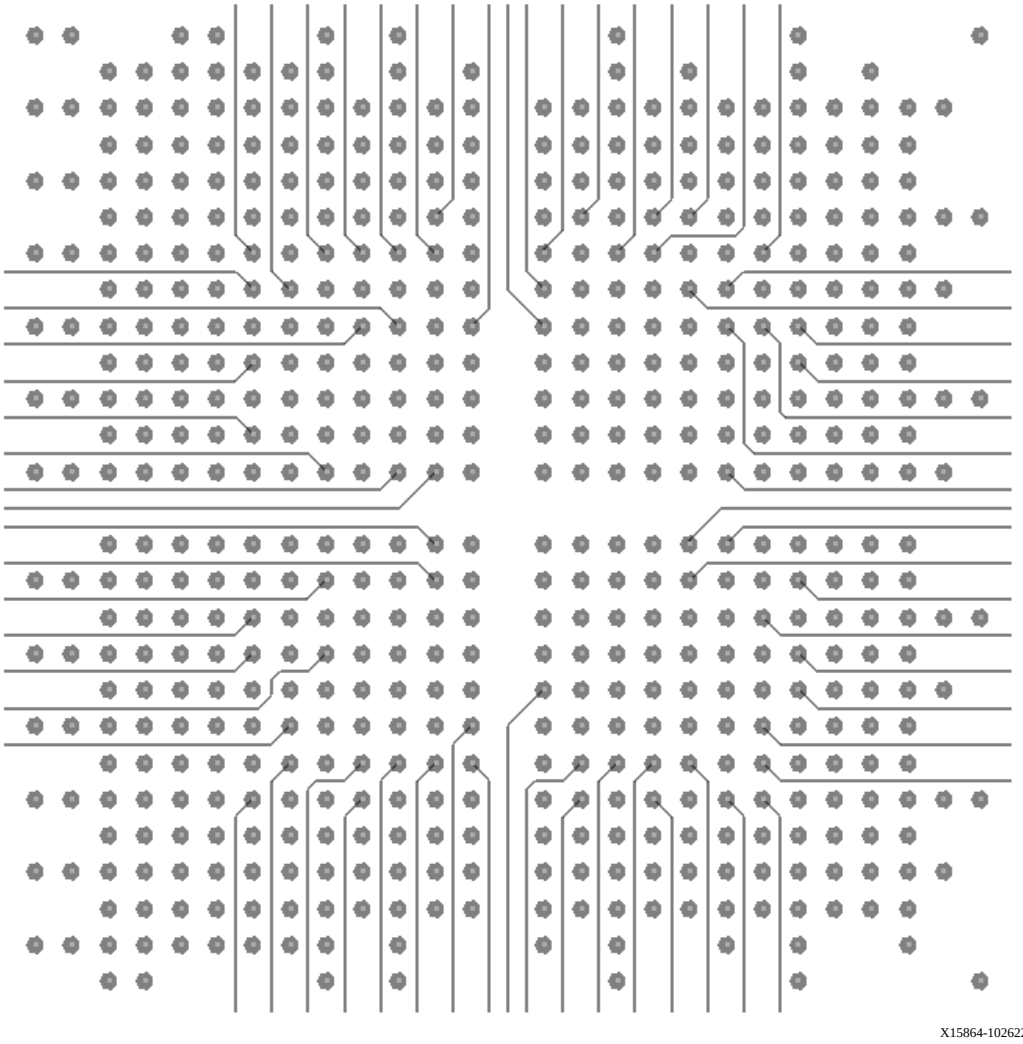
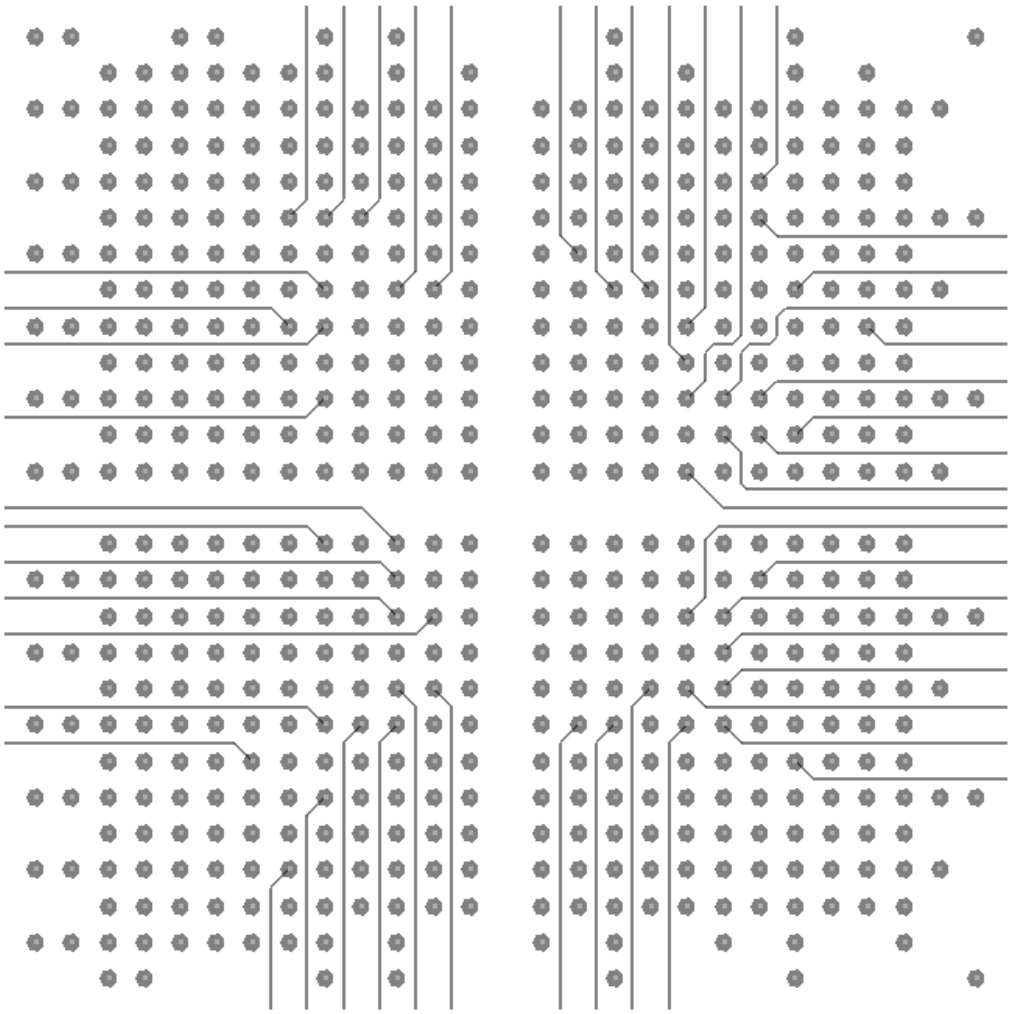
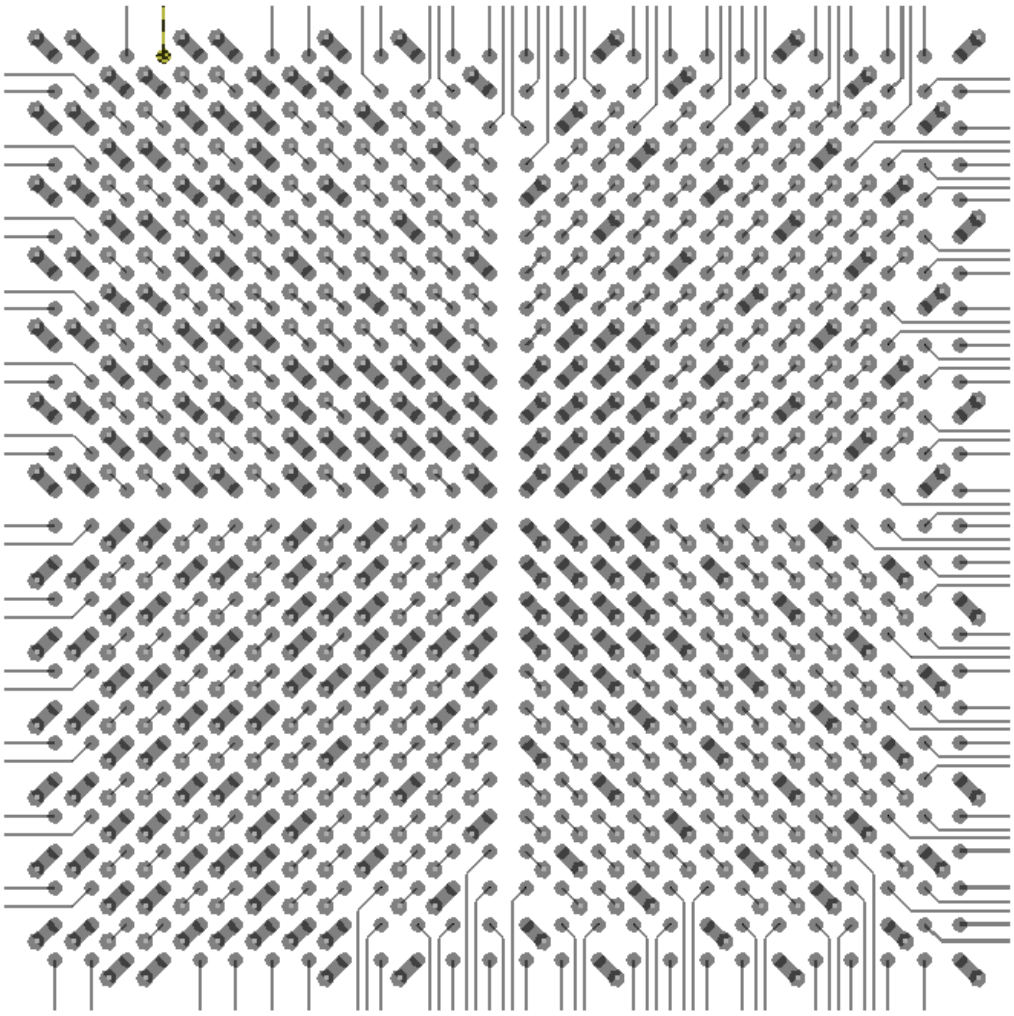


Figure 20: **Inner Signal Layer Five Breakout (1.0 mm/0.92 mm/0.8 mm), One Route between Vias**



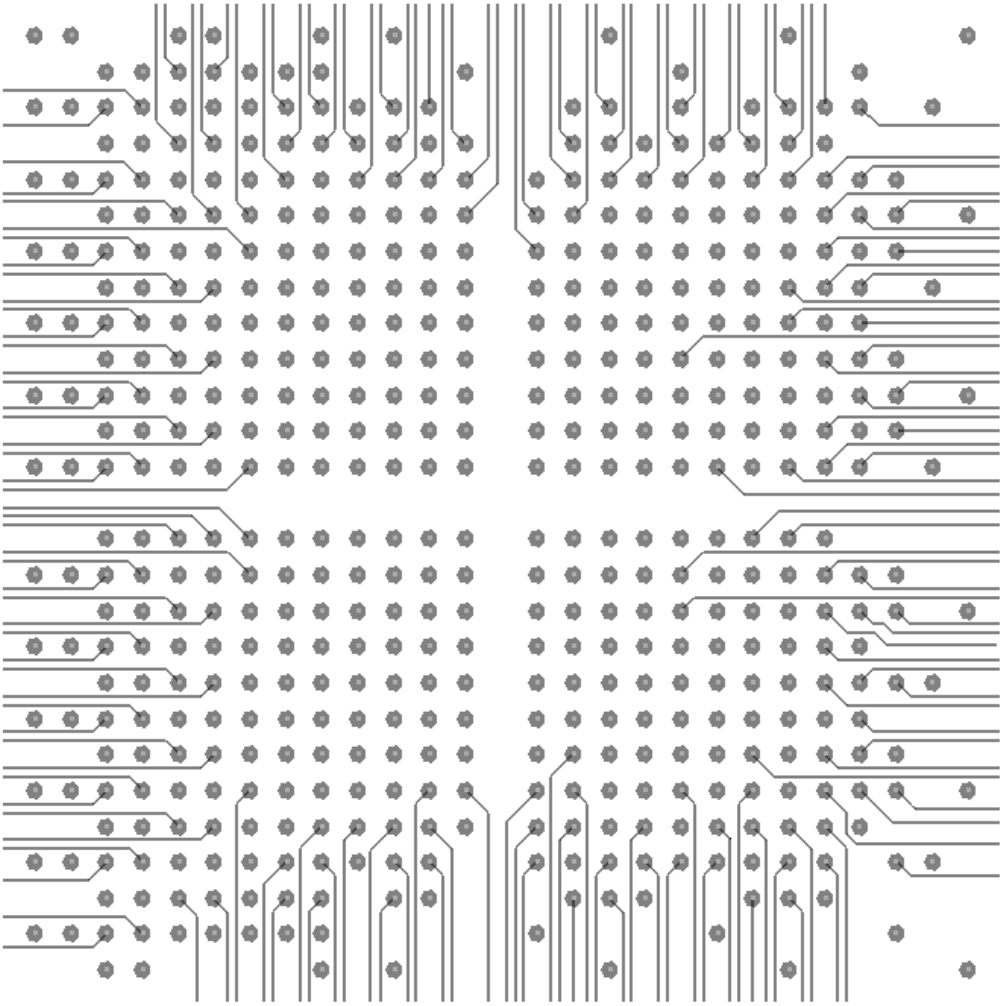
Sample Breakout with Two Routes between BGA Balls and Vias

Figure 21: **Top Layer Breakout (1.0 mm/0.92 mm/0.8 mm), Two Routes between BGA Balls**



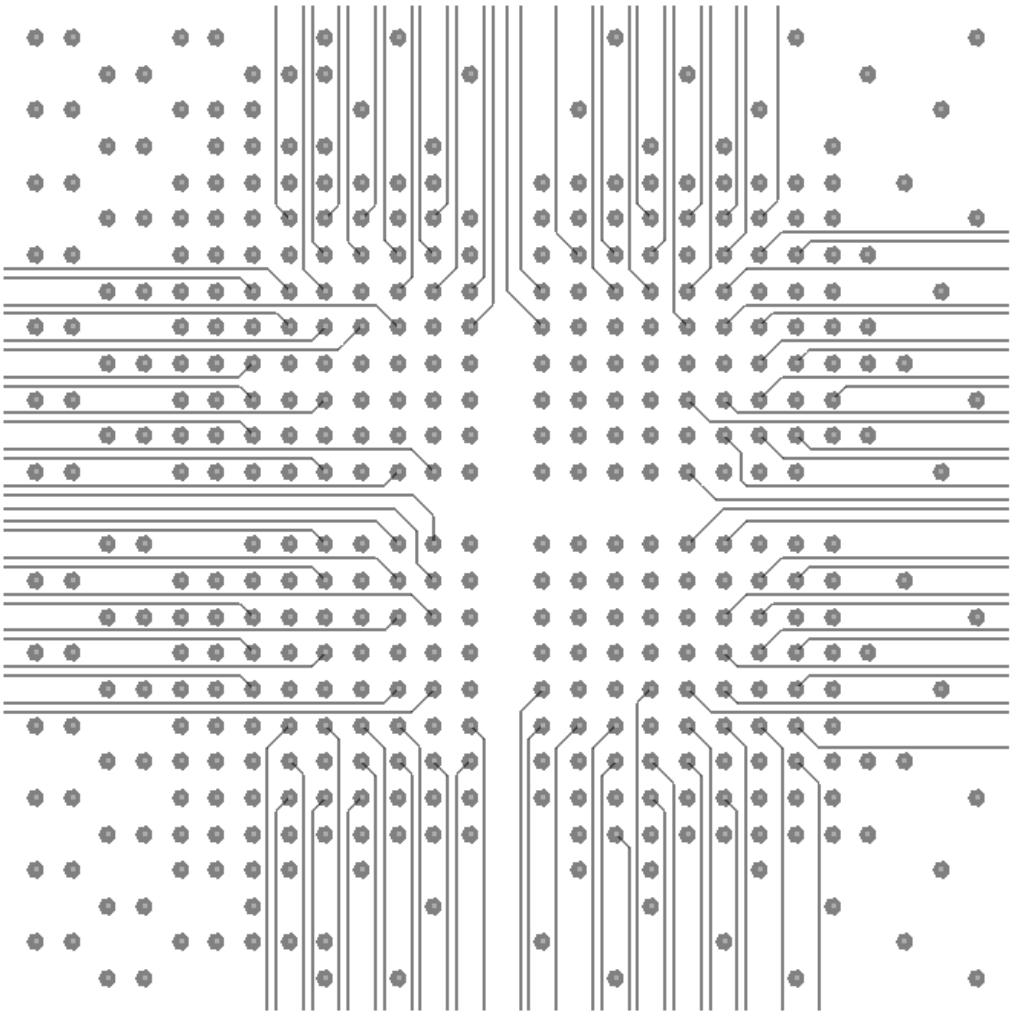
X15866-102622

Figure 22: **Inner Signal Layer One Breakout (1.0 mm/0.92 mm/0.8 mm), Two Routes between Vias**



X15867-102622

Figure 23: **Inner Signal Layer Two Breakout (1.0 mm/0.92 mm/0.8 mm), Two Routes between Vias**



Sample Breakout for 0.5 mm Pitch Devices

The following figures show an example layout showing the BGA routing breakout areas of a 0.5 mm pitch Xilinx® device. The footprint is for a UBVA530 “InFO” device.

Figure 24: **Top Layer Breakout (0.5 mm), One Route between BGA Balls**

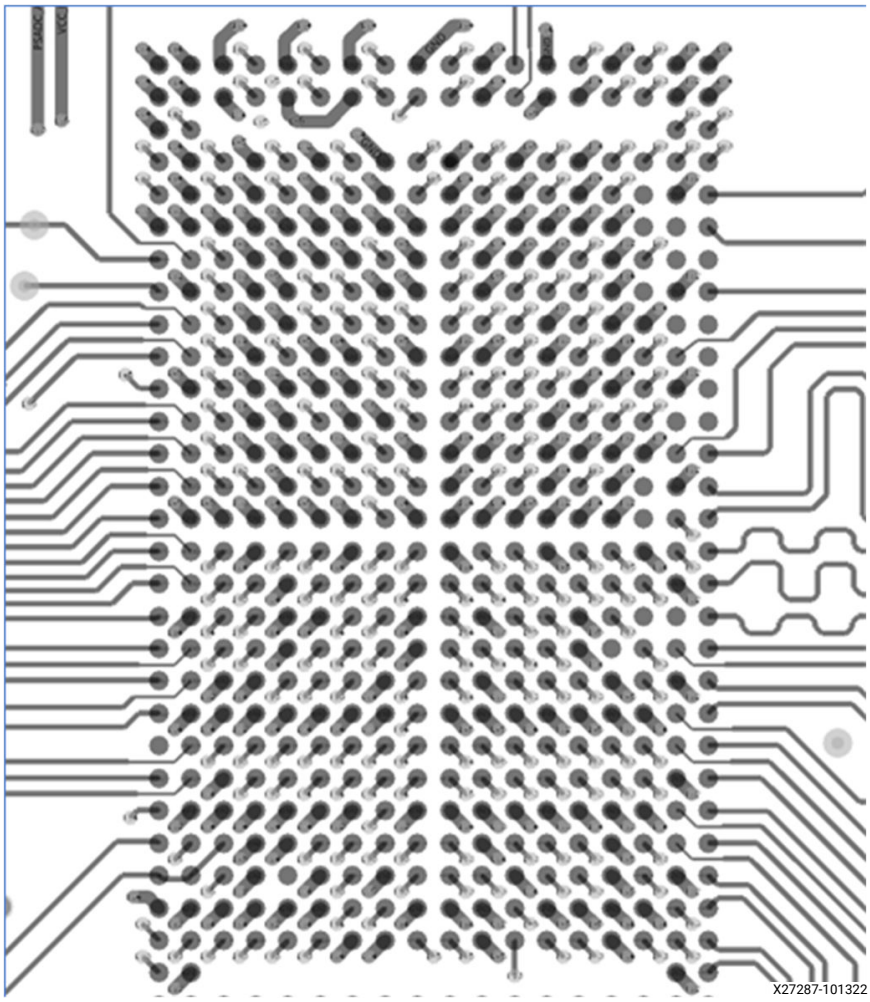


Figure 25: **First Inner Signal Breakout (0.5 mm), One Route between BGA Balls**

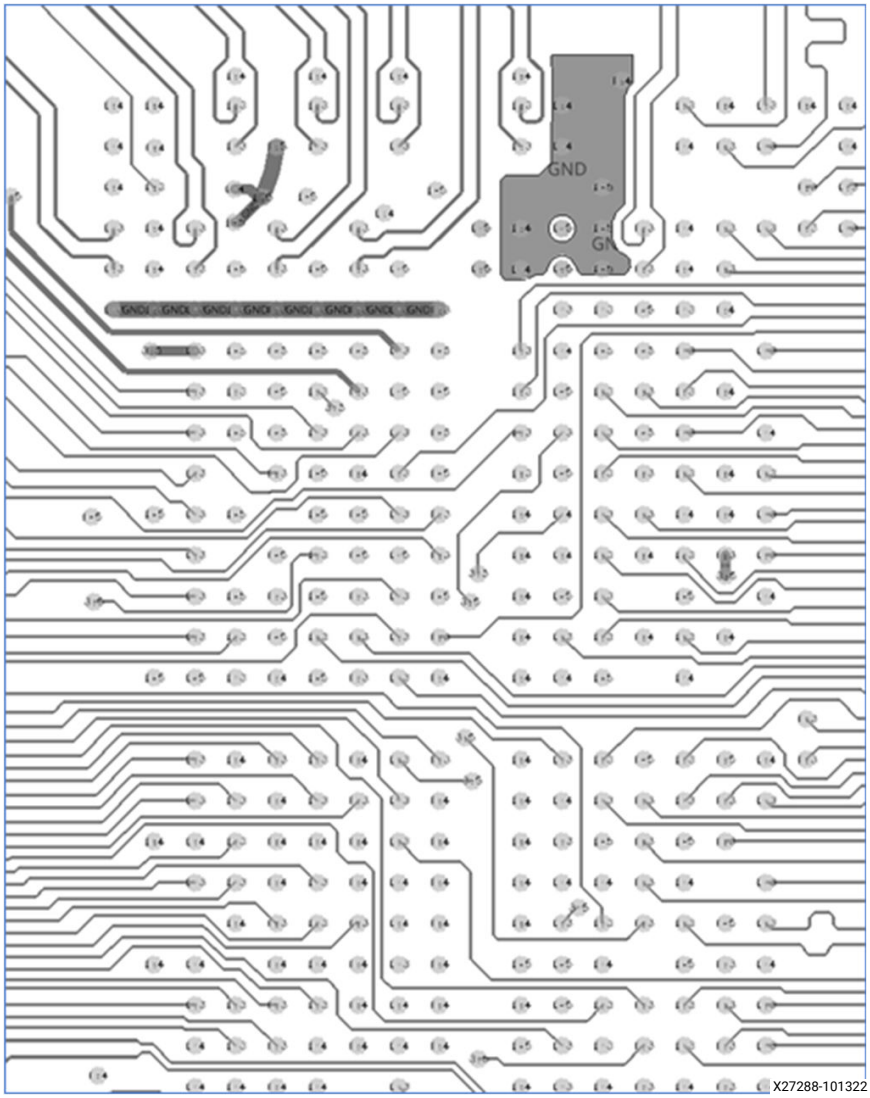
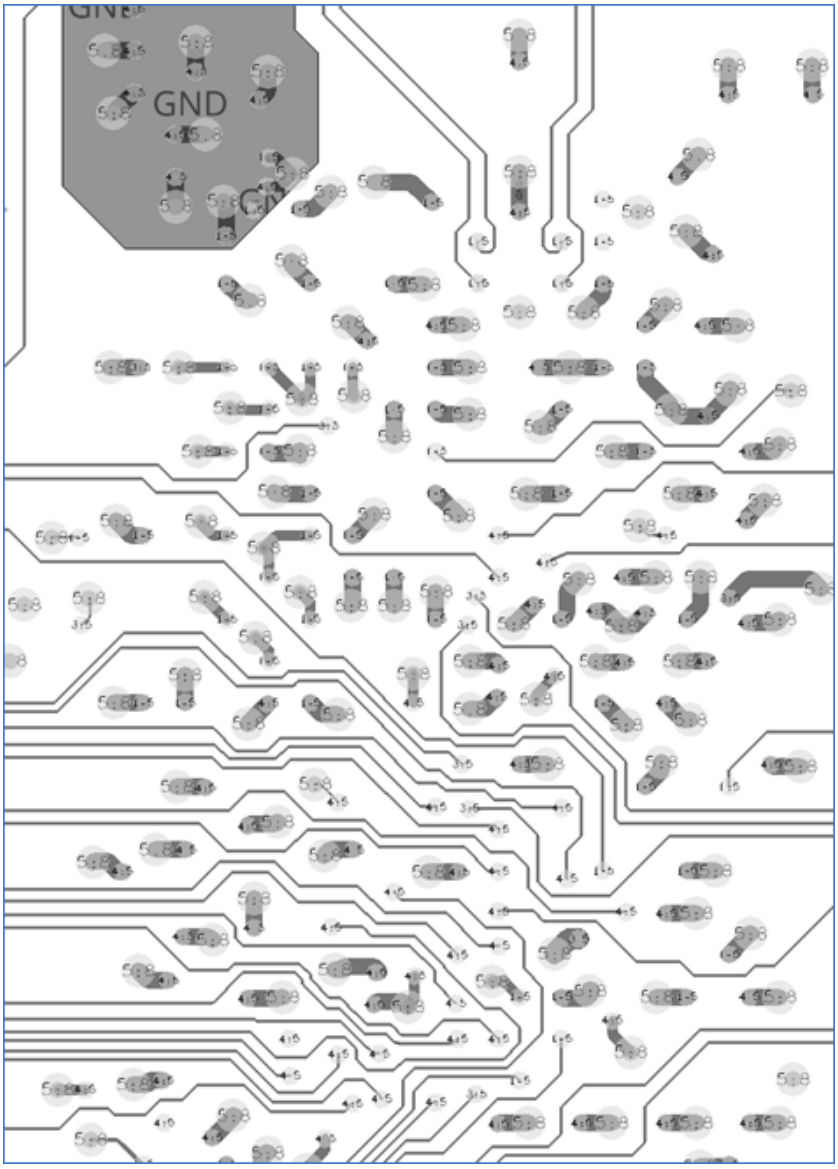


Figure 26: **Second Inner Signal Breakout (0.5mm), One Route between BGA Balls**



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Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Versal ACAP PCB Design User Guide* (UG863)
2. *UltraScale Architecture PCB Design User Guide* (UG583)
3. *Zynq-7000 SoC PCB Design Guide* (UG933)
4. *7 Series FPGAs PCB Design Guide* (UG483)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/23/2022 Version 2.0	
N/A	Re-worked entire document, adding information for Versal architecture.
03/01/2016 Version 1.0	
Initial release.	N/A

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