Using LVAUX Mode in XQ Ruggedized UltraScale+ Devices for Airborne Systems

Design Guide

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Chapter 1

Introduction

AMD UltraScale+™ devices are susceptible to radiation induced upsets, as are virtually all advanced and complex semiconductor devices. The industry broadly refers to radiation effects under the umbrella term of single-event effects (SEE). For an introduction to radiation effects, and a full write-up of types of SEE and the impact to AMD devices, see *Considerations Surrounding Single Event Effects in FPGAs, ASICs, and Processors* (WP402). AMD proactively designs for reduction and mitigation of SEEs, with an objective to reduce the SEE rates with each successive product family.

UltraScale+ devices are built on the TSMC 16 nm FinFET+ process node. This first FinFET node for AMD has allowed for great reductions in single event upset (SEU) rates. While previous platforms were not susceptible to single-event latch-up (SEL), the UltraScale+ devices have exhibited SEL, as identified in the IEEE paper (*Single Event Latch-Up: Increased Sensitivity from Planar to FinFET*, J. Karp, M. J. Hart, P. Maillard, Xilinx, Inc.; G. Hellings, D. Linten, IMEC; IEEE NSREC 2017, http://ieeexplore.ieee.org/document/8141939/). This SEL rate was discovered and characterized through extensive pre-production radiation testing and characterization. While the SEL rate is significantly mitigated through silicon design enhancements, a very low rate, low current, and non-destructive or damaging SEL rate remains.

Certain classes of Aerospace & Defense (A&D) applications that are exposed to significantly higher levels of radiation, such as applications targeting commercial aircraft, might seek to assess and mitigate the remaining low-rate SEL. For applications where this is important, the AMD Defense-grade (XQ) UltraScale+ devices allow for an additional mitigation method that is not available in the AMD Commercial (XC) or AMD Automotive (XA) devices. This SEL mitigation method is achieved by using the auxiliary I/O in low-voltage (LVAUX) mode that is only available when specifying the XQ ruggedized packages. The background on UltraScale+ SEL rates and the mitigation approaches are discussed in this document along with detailed guidelines on how to design for and operate the device in the LVAUX mode.

See the *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895) for available XQ UltraScale+ devices and ruggedized packages.

SEL Rate and Impact Assessment

The low-rate residual SEL was characterized though extensive neutron and proton beam testing on AMD Zynq™ UltraScale+™ devices, AMD Kintex™ UltraScale+™ FPGAs, and AMD Virtex™ UltraScale+™ FPGAs.

The impacted circuits in the device reside in the System Monitor (SYSMON) block and the high-performance (HP) I/O auxiliary block that controls level shifting and digitally-controlled impedance for the HP I/O pins. When following standard PCB guidelines and data sheet specifications for XC devices, these blocks are powered by the V_{CCAUX}, V_{CC_PSAUX}, and the V_{CCAUX_IO} supplies that are connected together and powered at 1.8V. The number of SYSMON blocks depends on the device. See the *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895) for how many SYSMON blocks are available by device. All UltraScale+ devices have an HP I/O auxiliary block for each HP I/O pin.

An SEL event manifests in an increased current draw on the supply line of interest. The only way to clear that increased SEL current is to power cycle the affected voltage line to a point below the holding voltage of 1V. Applying this approach on an XC device, where all the affected power rails are connected to 1.8V, would trigger power-on reset. Employing a more granular power system that independently controls the processing system (PS) and programmable logic (PL) affected supplies can allow for independent PS and PL recovery from an SEL event.

UltraScale+ Device SEL

The device-level SEL is not destructive for UltraScale+ devices when operating within the Earth's atmosphere. The device continues to operate with any potential impact isolated to the function of the block where the SEL occurred. The SEL only impacts the operation of the SYSMON block or the HP I/O pin where it occurred. SEL due to alpha particles or thermal neurtrons was not observed in SYSMON blocks (V_{CCAUX}) or HP I/O auxiliary blocks (V_{CCAUX_IO}).

The residual SEL rate for a ZU9EG device is approximately 0.25 FIT at 85°C junction temperature (T_j), and 0.65 FIT at 125°C T_j at New York City sea-level. The device-level SEL rate scales based on the previously mentioned resource count in each device, and based on T_j along with the relative neutron flux per the following guidance:

- Device SEL rate [FIT] = SYSMON SEL rate + HP I/O auxiliary block SEL rate
- SYSMON SEL rate [FIT] = 0.050 × Number of SYSMONs × Avg flux scaling × Avg T_j scaling
- HP I/O auxiliary SEL rate [FIT] = 0.0008 × Number of HP I/O auxiliary blocks × Avg flux scaling × Avg T_j scaling

AMD provides an SEU FIT rate calculator tool to calculate the relative flux scale factor. For more information or to download the calculator, go to https://www.xilinx.com/member/avionics.

Table 1: **Average T_j Scaling Factor**

T_j	20	30	40	50	60	70	80	90	100	110	120	125
Scaling	0.31	0.38	0.46	0.58	0.69	0.85	1.00	1.23	1.50	1.81	2.19	2.42

Table 2: **Maximum HP I/O Auxiliary Blocks per Device**

Device	Ruggedized Packages	Maximum HP I/O Auxiliary Blocks per Device[1]
XQKU5P	SFRB784 and FFRB676	208
XQKU15P	FFRA1156 and FFRE1517	572
XQVU3P	FFRC1517	520
XQVU7P	FLRA2104 and FLRB2104	1040
XQVU11P	FLRC2104	624
XQZU3EG	SFRA484 and SFRC784	156
XQZU5EV	SFRC784 and FFRB900	208
XQZU7EV	FFRB900 and FFRC1156	416
XQZU9EG	FFRC900 and FFRB1156	208
XQZU11EG	FFRC1156 and FFRC1760	416
XQZU15EG	FFRC900 and FFRB1156	208
XQZU19EG	FFRB1517 and FFRC1760	572
XQZU21DR	FFRD1156	416
XQZU28DR	FFRE1156 and FFRG1517	416
XQZU29DR	FFRF1760	416
XQZU48DR	FFRE1156 and FFRG1517	416
XQZU49DR	FSRF1760	416
XQZU65DR	FFRE1156	260
XQZU67DR	FFRE1156	260

Notes:

1. Maximum number of HP I/O auxiliary blocks includes bonded and unbonded HP I/O pins.

SEL Impact

For XC, XA, and XQ devices operating within the Earth's atmosphere, the SYSMON SEL currents are a few hundred mA or less with no impact to device-level silicon. The SEL currents associated with the HP I/O auxiliary blocks can be up to 1A and while this is not destructive damage to the device, there can be electrically induced physical damage (EIPD) in a metal layer in the device. This could cause a long-term reliability impact, even while the device might not exhibit any functional degradation in the near term.

***Note*:** For XQ ruggedized UltraScale+ devices operated in LVAUX mode, the SEL events on HP I/O auxiliary blocks are eliminated. Only the SYSMON SEL currents (up to a few hundred mA or less) remain and have no impact on the device-level silicon. Refer to the SEL Mitigation Options Overview for further details on the available methods to mitigate SEL.

The impact of an SEL event on the SYSMON can manifest as either a frozen reading of the SYSMON ADCs seen as a constant count value reading from the ADC, or an extreme reading of the die temperature, such as an out of bounds T_j reading for either extreme cold or hot. If any one of these conditions is present, the SYSMON that is being read has been upset. In designs using a Zynq UltraScale+ device, there are two SYSMON blocks, and one can still read an accurate die temperature even if the other has been affected by an SEL event.

The impact of an SEL event on an HP I/O auxiliary block can be less obvious, if even apparent at all to device function. The affected HP I/O auxiliary block controls the digitally-controlled impedance (DCI) and level shifting for the HP I/O pin. In most cases, it will be masked with no impact to the system. Several reasons exist for this outcome:

- The DCI is not necessary in most applications running at 2400 Mb/s or slower.
- The level shifting impacts can be masked by forgiveness in the I/O standard because an interface device might accept signaling outside of parameters of the selected interface standard.
- The HP I/O pin might not be used because either the design does not use all available HP I/O pins in the package or the device has more HP I/O pins and HP I/O auxiliary blocks than are bonded out in the package chosen.

To determine whether an SEL mitigation method is necessary, consider the different measures of SEL impact to the system along with the duration between power cycling of the device in the system. AMD testing included holding several devices in the latched-up state for hundreds of hours without any effect beyond the increased current draw. The most prudent method is to detect and power cycle to clear the SEL in a shorter time frame to best balance impacts on the end system. For some systems, power could be applied nearly continuously for days, months, or years without normal power cycling. Other systems might have a shorter mission duration of a few hours or a day at a time, with power cycled following the mission. It could be sufficient to do nothing in the case of the shorter time frame between power cycling; therefore, SEL mitigation might not be necessary. In assessing the impact and whether mitigation is necessary, consider the expected operating lifetime of a device in the system, the duration between power cycling of the device in the system, the probability of an SEL event in a device operating lifetime in the system, the total application SEL rate across the total volume of deployed device operating hours, and other architectural mitigation or background functional monitoring of this device in the system.

Following an assessment of the SEL rate, if mitigation is needed, read on. When SEL mitigation is not necessary for the application, no further information from this document is needed. If SEL mitigation is not being used, then there could be up to 1A of additional current drawn on the 1.8V HP I/O auxiliary supply, leading to an additional 1.8W being dissipated within the device. These two factors should be accounted for in applications that are designed to ride through SEL events without additional monitoring.

SEL Mitigation Options Overview

Based on assessment of the SEL rate for the system, and considering the impact of an SEL on the system, a system architect can assess whether an SEL mitigation approach is required. Use the following information to select an appropriate mitigation approach, which could include using the device in LVAUX mode. Mitigation approaches should consider the following guidance:

- Monitor the junction temperature of the device.
  - Monitor for temperatures outside the range of the recommended operating minimum and maximum junction temperatures for the device (T_j) available in the *Recommended Operating Conditions* tables in the UltraScale+ device data sheets.
  - Monitor the SYSMON temperature readings in the PS and PL when designing with either the Zynq UltraScale+ MPSoCs or Zynq UltraScale+ RFSoCs.
- Monitor for flat-line (stuck-at) SYSMON readings.
  - Junction temperature
  - Other ADC readings
- Monitor current on the three rails and look for current step on 1.8V auxiliary supplies.
  - Monitor the current on the combined sum of 1.8V auxiliary supply rail currents.
    - V_{CCAUX}
    - V_{CCAUX_IO}
    - V_{CC_PSAUX}
  - Additional separate monitoring for each independent auxiliary supply rail. For self-monitoring, use the PL SYSMON ADC for measuring 1.8V auxiliary current(s).
    - Use dedicated VP/VN pins to monitor the total 1.8V auxiliary current.
    - Other analog inputs can be used for additional monitoring.
  - Following device initialization, monitor for SEL current step that is greater than 100 mA within less than 10 µs.
    - Monitor step should be functionally tested over environmental conditions.
    - The monitor step value could need adjustment to ensure no false SEL triggers occur as a result of dynamic behavior in the specific design implementation.
- Run monitor code in platform management unit (PMU) for Zynq UltraScale+ devices, or triple-modular redundancy (TMR) MicroBlaze™ processor in UltraScale+ FPGAs.
  - Use a pulsing output signal to indicate status of good.
  - Use a steady High or Low output signal to indicate SEL or another anomalous condition.
- Power cycle to clear the increased SEL current draw.
  - The affected power supply rail must fall below 1V to clear the SEL condition.
  - Power cycling on the affected PL supplies will trigger a power-on reset.

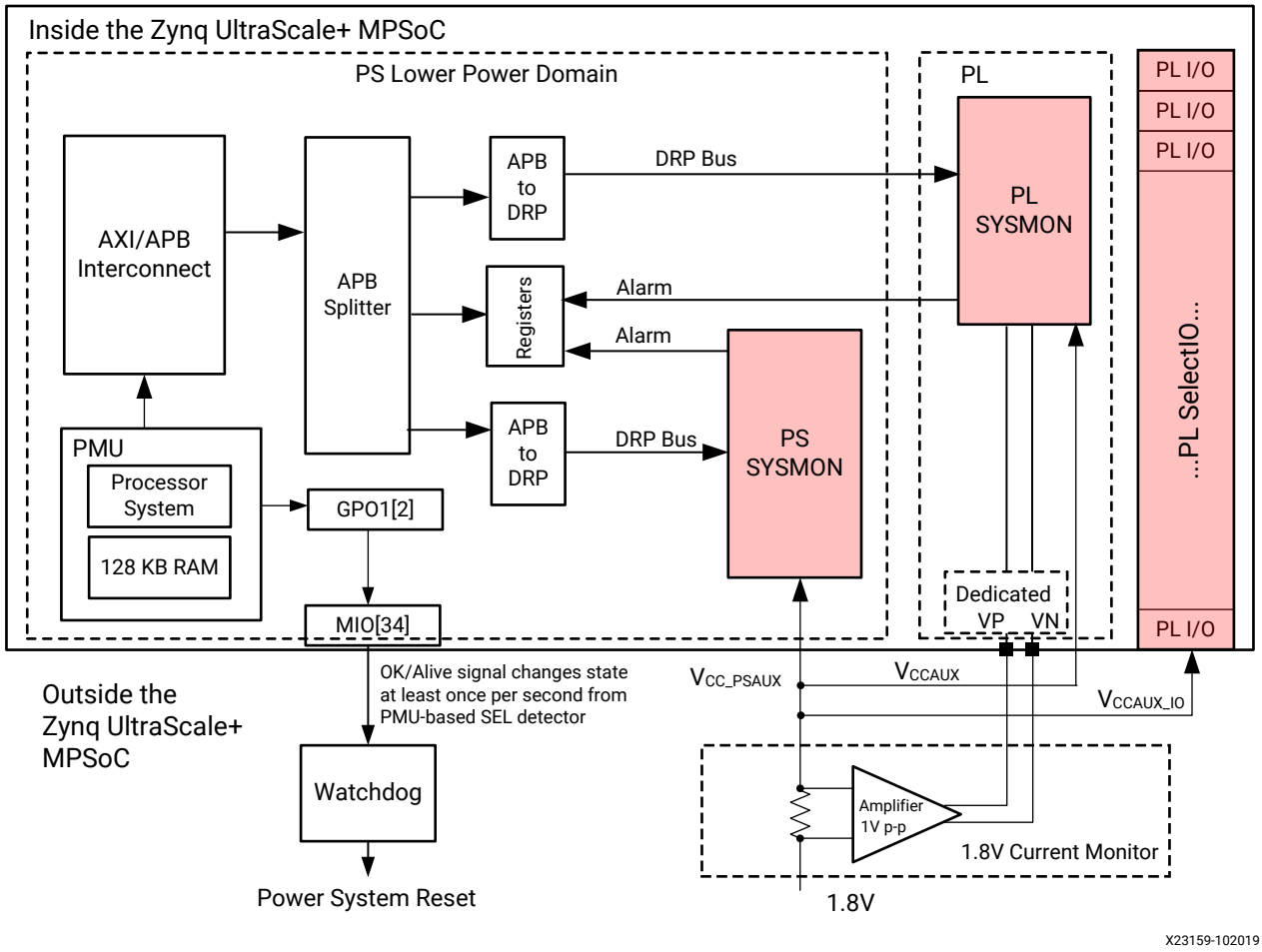
    - If necessary, the PS and PL can be cycled independently (requires additional guidance).
- Monitor and log events at the system level and store in non-volatile memory.
    - Long-term reliability could be impacted as a result of SEL in the HP I/O auxiliary block.
    - SEL events in SYSMON have no impact on device reliability.
    - Logging of SEL events to non-volatile memory can be a valuable maintenance tool.
- Develop SEL mitigation circuits that monitor temperature changes and reduces voltage to a level that clears an SEL as described in patent US9793899B1.

SEL rates can be managed independently in the SoC. Partitioning the device-level SEL into a PS SEL rate and a PL SEL rate allows for the possibility of independent power cycling of the PS and PL. This approach requires additional guidance beyond the scope of this document. It also adds complexity to the power-on and booting of the device including an additional impact to any PS APU and RPU embedded code and the PL design.

Current Monitoring

The conceptual current monitoring circuit and architecture shown in the following diagram can be used for self-monitoring of the SEL conditions in a Zynq UltraScale+ device. An external current sense amplifier can feed into dedicated VP/VN analog monitor pins that are directly wired into the PL SYSMON ADC. It is used with a customized code base for the PMU to monitor for the current step and other SEL conditions. The PMU code base for SEL monitoring, which accounts for the previous guidance, makes this type of self-monitoring solution viable. An alternative approach of running SEL monitoring code in the RPU or APU, rather than the PMU, also can be viable.

Figure 1: **Current Monitoring Circuit**

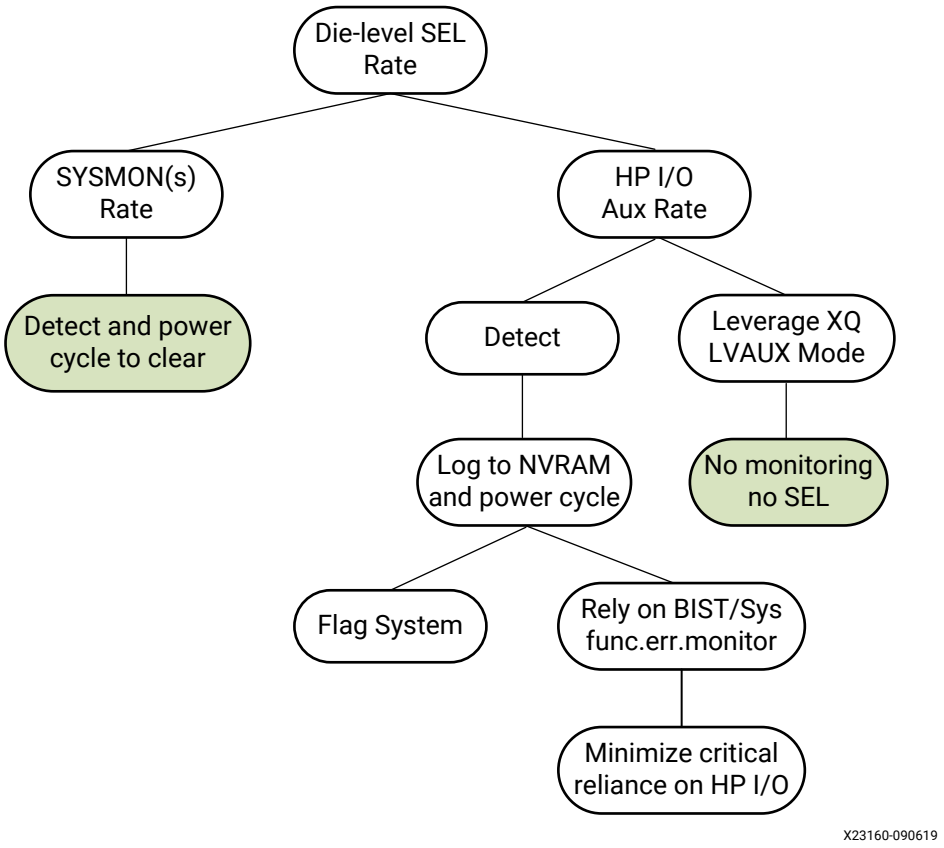


Leveraging the additionally supported LVAUX mode in XQ ruggedized devices, the SEL rate on HP I/O auxiliary blocks is eliminated. LVAUX mode eliminates the need for monitoring SEL on the V_{CCAUX_IO} power supply, significantly reducing the device SEL rate and removing any long-term reliability concern that can result from SEL. When LVAUX mode is implemented, the PS and PL SYSMON blocks are the only remaining SEL susceptible elements in the device. This document provides guidance on how to configure the device to operate in LVAUX mode.

Decision Tree

The following decision tree summarizes the high-level SEL mitigation options based on the previously outlined details. The remainder of this user guide describes the technical parameters and use of LVAUX mode in the XQ ruggedized UltraScale+ devices.

Figure 2: **Decision Tree**



LVAUX Mode Overview

This section illustrates the differences between standard operating mode and LVAUX mode and provides a broad overview on how to configure the XQ ruggedized device in LVAUX mode. The main differences involve applying the LVAUX I/O standards to HP I/O banks and changing the auxiliary HP I/O power supply voltage (V_{CCAUX_IO}) configuration.

Only XQ UltraScale+ devices in ruggedized packages can be used in LVAUX mode. XQ Kintex UltraScale+ and Zynq UltraScale+ ruggedized packages support separated auxiliary supplies for the HP I/O and HD I/O. Correspondingly, these XQ Kintex UltraScale+ and Zynq UltraScale+ ruggedized packages have unique pin names for the HP I/O auxiliary voltage supply rail (VCCAUX_HPIO) and the high-density (HD) I/O auxiliary voltage supply rail (VCCAUX_HDIO). The V_{CCAUX_HPIO} supply powers the auxiliary HP I/O circuity, and the V_{CCAUX_HDIO} supply powers the auxiliary HD I/O circuity.

In standard operating mode, the VCCAUX_HDIO and VCCAUX_HPIO power supply pins should be connected to a common V_{CCAUX_IO} supply. V_{CCAUX_IO} is shared with V_{CCAUX} and both are powered at 1.8V. In AMD documentation, the V_{CCAUX_HPIO} and V_{CCAUX_HDIO} supplies are collectively referred to as V_{CCAUX_IO}. The References section lists the documentation used to operate the device in standard operating mode.

IMPORTANT! *The XQ Virtex UltraScale+ devices do not have HD I/O, and thus their package VCCAUX_IO pins are inherently isolated to supply auxiliary power to only the HP I/O. References and LVAUX mode recommendations for the VCCAUX_HPIO supply/pins through the remainder of this document are applicable to the XQ Virtex UltraScale+ device VCCAUX_IO supply/pins. See the Special Considerations for XQ Ruggedized FPGAs section for additional details.*

The rest of this document details how to operate the device in LVAUX mode. For any operation or specification not mentioned in this document, AMD recommends following the standard guidelines provided in the documents listed in References. For example, to operate the device in LVAUX mode, the specification for V_{CC_PSAUX} is not changed. Therefore, you can refer to the applicable documents listed in References for guidance.

In the ruggedized packaging, the VCCAUX_IO pins are split and referred to as VCCAUX_HDIO and VCCAUX_HPIO pins. This split allows different supply voltages operating the device in LVAUX mode. V_{CCAUX_HPIO} and V_{CCO} for all HP I/O banks must be powered by 1.2V when operating in LVAUX mode. All HP I/O pins used in the design must be set to the LVAUX I/O standards in the AMD Vivado™ Design Suite. Refer to the 1.2V LVAUX I/O Standards list. The V_{CCAUX_HDIO} and V_{CCAUX} supplies must always be powered at 1.8V. For all HD I/O banks, V_{CCO} has the same requirements and specifications as standard operating mode.

All XQ references in this user guide are specific to the UltraScale+ devices available in XQ ruggedized packages. See the *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895) for further information regarding the available XQ ruggedized devices.

SelectIO Resources

The XQ ruggedized UltraScale+ devices have some combination of HP I/O and HD I/O. The *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895) lists these resources by device and package. See *UltraScale Architecture SelectIO Resources User Guide* (UG571) for details on HD I/O and HP I/O.

When the device is in LVAUX mode, each HP I/O pin that is used in the design must be configured to use one of the 1.2V LVAUX I/O standards listed here:

- LVCMOS12_LVAUX
- SSTL12_LVAUX
- DIFF_SSTL12_LVAUX
- AIO12_LVAUX
- DIFF_AIO12_LVAUX
- LVDS12_LVAUX

- MIPI_DPHY_LVAUX

***Note*:** System monitor external analog inputs (I/O standard = ANALOG or ANALOG_SE) are not supported in LVAUX mode HP I/O banks. Instead, if HD I/O are available in the device, consider routing external analog inputs through an HD I/O.

Supply Voltages for SelectIO Pins

V_{CCO}

Refer to the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for details on the general V_{CCO} requirements. The V_{CCO} requirements and optional internal differential terminations for LVAUX I/O standards are described in Table 28: Rules for Combining I/O Standards in the Same Bank. When the device is in LVAUX mode, V_{CCO} must be 1.2V on all HP I/O banks. For all HD I/O banks, V_{CCO} has the same requirements and specifications as standard operating mode.

V_{REF}

Refer to the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for details regarding the V_{REF} supply requirements.

V_{CCAUX}

When designing with the XQ ruggedized devices in standard operating mode or LVAUX mode, the V_{CCAUX} supply must be maintained at 1.8V. In the case of SEL mitigation, this supply can be power cycled to remove an SEL condition. Refer to the UltraScale+ device data sheets for guidance on this power supply. If the minimum voltage is not maintained, the device power-on reset is triggered.

V_{CCAUX_IO}, V_{CCAUX_HPIO}, and V_{CCAUX_HDIO}

In XQ ruggedized UltraScale+ devices, the VCCAUX_IO pins are split for the HD and HP I/O banks, as identified in the package files for these devices in the Package File Portal. The combined set of VCCAUX_HPIO pins and VCCAUX_HDIO pins in the XQ ruggedized packaging for Kintex UltraScale+ FPGAs and Zynq UltraScale+ devices replace the VCCAUX_IO pins that are used in the XC packages.

To operate the XQ ruggedized UltraScale+ device in LVAUX mode, V_{CCAUX_HPIO} must be powered at 1.2V and V_{CCAUX_HDIO} must be powered at 1.8V.

To operate the XQ ruggedized device in standard operating mode, use a single 1.8V supply for all VCCAUX_HDIO pins and VCCAUX_HPIO pins (or VCCAUX_IO pins for Virtex UltraScale+ FPGAs without HD I/O pins only). Apply guidance from the *UltraScale Architecture SelectIO Resources User Guide* (UG571) about VCCAUX_IO to these pins.

Special Considerations for XQ Ruggedized FPGAs

XQ Ruggedized Virtex UltraScale+ FPGAs Package Pin and Supply Names

The XQ ruggedized Virtex UltraScale+ devices do not have HD I/O, and their packages use the common VCCAUX_IO pin name, rather than the special VCCAUX_HPIO pin name. Thus, these XQ ruggedized Virtex UltraScale+ device VCCAUX_IO pins are inherently isolated to supply auxiliary power to only the HP I/O. References and LVAUX mode recommendations for the VCCAUX_HPIO supply/pins through the remainder of this document are applicable to the XQ ruggedized Virtex UltraScale+ device VCCAUX_IO supply/pins. The VCCAUX_HDIO supply/pins references and recommendations in this document do not apply to XQ ruggedized Virtex UltraScale+ devices.

The following table summarizes HP I/O and HD I/O pin names, supply names, and recommendations for the XQ ruggedized UltraScale+ devices.

Table 3: **Package Pin and Supply Names for Normal and LVAUX Mode by Family**

Device Family	I/O Type	XQ Ruggedized Package Pin Names	Auxiliary HP I/O and HD I/O Banks Supply Names and Voltages			
		I/O Pins	Normal Mode Supply		LVAUX Mode Supplies	
		Pin Name	Supply Name	Supply Voltage	Supply Name	Supply Voltage
XQ Ruggedized Zynq UltraScale+ Devices	HP I/O	VCCAUX_HPIO[1]	V_{CCAUX_IO}[1]	1.8V[1]	V_{CCAUX_HPIO}[2]	1.2V[2]
	HD I/O	VCCAUX_HDIO[1]			V_{CCAUX_HDIO}[2]	1.8V[2]
XQ Ruggedized Kintex UltraScale+ Devices	HP I/O	VCCAUX_HPIO[1]	V_{CCAUX_IO}[1]	1.8V[1]	V_{CCAUX_HPIO}[2]	1.2V[2]
	HD I/O	VCCAUX_HDIO[1]			V_{CCAUX_HDIO}[2]	1.8V[2]
XQ Ruggedized Virtex UltraScale+ Devices	HP I/O	VCCAUX_IO[3]	V_{CCAUX_IO}[3]	1.8V[3]	V_{CCAUX_HPIO}[4] (for VCCAUX_IO pins)	1.2V[4]
	HD I/O[5]	N/A	N/A	N/A	N/A	N/A

Notes:

1. In normal mode, XQ Ruggedized Zynq UltraScale+ and XQ Ruggedized Kintex UltraScale+ device VCCAUX_HPIO, VCCAUX_HDIO, and VCCAUX pins must be tied together; and V_{CCAUX_IO} and V_{CCAUX} must be supplied from one 1.8V power supply.
2. In LVAUX mode, XQ Ruggedized Zynq UltraScale+ and XQ Ruggedized Kintex UltraScale+ device VCCAUX_HDIO and VCCAUX pins must be tied together; and V_{CCAUX_IO} and V_{CCAUX} must be supplied from one 1.8V power supply. A separate 1.2V V_{CCAUX_HPIO} source must supply the VCCAUX_HPIO pins.
3. In normal mode, XQ Ruggedized Virtex UltraScale+ device VCCAUX_IO and VCCAUX pins must be tied together; and V_{CCAUX_IO} and V_{CCAUX} must be supplied from one 1.8V power supply.
4. In LVAUX mode, XQ Ruggedized Virtex UltraScale+ device VCCAUX pins must be supplied from a 1.8V V_{CCAUX} power supply, and a separate 1.2V V_{CCAUX_HPIO} source must supply the VCCAUX_IO pins.
5. XQ Ruggedized Virtex UltraScale+ devices do not have HD I/O.

Managing the Bank 0 V_{CCO_0} in XQ Ruggedized UltraScale+ FPGAs

In XQ ruggedized Kintex UltraScale+ and Virtex UltraScale+ FPGAs, bank 0 is reserved for specific power on and configuration signals. V_{CCO_0} is the supply voltage for bank 0. For V_{CCO_0}, the minimum recommended operating voltage for power-up through configuration is 1.425V. During configuration, V_{CCO_0} must be set to 1.5V or 1.8V.

XQ Ruggedized UltraScale+ FPGA Configuration Modes

For XQ ruggedized Kintex UltraScale+ and Virtex UltraScale+ FPGAs, the configuration interfaces that use bank 65 are not supported in LVAUX mode. This is because bank 65 requires a greater voltage than the LVAUX mode supports. The following FPGA configuration modes are *not* supported in LVAUX mode:

- Master SPI (x8 (dual x4))
- Master BPI (x8, x16)
- Slave SelectMAP (x8, x16, x32)

The following configuration modes are supported for LVAUX mode:

- Slave serial without DOUT
- JTAG
- Master SPI (x1) without EMCCLK and DOUT
- Master SPI (x2, x4) without EMCCLK

Summary of LVAUX Mode versus Standard Operating Mode

The following table lists the key differences when operating a device in standard operating mode versus LVAUX mode.

Table 4: **Key Differences Between Standard Operating Mode and LVAUX Mode**

Standard Operating Mode	LVAUX Mode
Power Considerations	
V_{CCAUX} = 1.8V	No change
V_{CCAUX}, V_{CCAUX_IO}, V_{CCAUX_HPIO}, and V_{CCAUX_HDIO} must be powered with 1.8V. VCCAUX_HPIO and VCCAUX_HDIO pins can be considered to be the same as the VCCAUX_IO pins on XC equivalent devices. Follow the standard guidance for these supplies.	V_{CCAUX} and V_{CCAUX_HDIO} must be powered with 1.8V. V_{CCAUX_HPIO} must be powered with 1.2V to prevent the possibility of SEL on the auxiliary HP I/O blocks in the XQ ruggedized device.
The V_{CCO} supply for HP and HP I/O pins should be powered in accordance with standard device guidance for standard operating mode.	The supply V_{CCO} for HP I/O pins must not exceed the V_{CCAUX_HPIO} supply voltage. The VCCO pins of unused HP I/O pins must be powered on and must be connected to the V_{CCAUX_HPIO} supply voltage. V_{CCAUX}, V_{CCAUX_HPIO}, and V_{CCAUX_HDIO} must be powered on for the device to operate as intended. V_{CCAUX_HPIO} and V_{CCO} for HP I/O pins must be powered at 1.2V to avoid SEL on the HP I/O auxiliary blocks even if no HP I/O pins are used in the design. However, in this special scenario where no HP I/O pins are used, these voltage supplies can share another 1.2V supply when used for another function on this device. V_{CCO} for HD I/O pins should be powered in accordance with standard device guidance for standard operating mode.
Estimate power and current consumption of combined HP I/O and HD I/O using Xilinx Power Estimator	Estimate power and current consumption of HP I/O only using Xilinx Power Estimator and guidelines in Chapter 3: Estimating Power Estimate power and current consumption of HD I/O only using Xilinx Power Estimator and guidelines in Chapter 3: Estimating Power
ESD Considerations	
Do not connect unused VCCO pins to GND.	No change
To reduce ESD, a general recommendation is to connect all unused VCCO pins to a valid power supply.	No change

Table 4: **Key Differences Between Standard Operating Mode and LVAUX Mode** *(cont'd)*

Standard Operating Mode	LVAUX Mode
Unused I/Os can be connected to the same potential as V_{CCO} or left floating.	Unused HP I/O pins must be powered by V_{CCO} = 1.2V for HP I/O banks. Where applicable, unused HD I/O banks can be connected to the same potential as V_{CCO} or left floating.
Vivado Design Suite Considerations	
N/A	The LVAUX I/O standards and DDR4 SDRAM (MIG) in the IP catalog are fully supported by Vivado Design Suite 2019.2 or later for XQ ruggedized UltraScale+ devices only.
N/A	If an HP I/O bank uses an LVAUX I/O standard, all HP I/O banks must use LVAUX I/O standards.
Memory Considerations	
See the specific UltraScale+ data sheet in References for the maximum physical interface (PHY) rate for memory interfaces.	See Table 43: Maximum Physical Interface (PHY) Rate for Memory Interfaces.
System Monitor External Analog Input Considerations	
System monitor external analog inputs supported in HP I/O and HD I/O banks.	System monitor external analog inputs supported in HD I/O banks only–not supported in LVAUX mode HP I/O banks.

LVAUX Mode Checklists

Use the following checklists to set up the design to support LVAUX mode.

PCB Design Checklist

- V_{CCAUX} must be powered at 1.8V.
- V_{CCAUX_HDIO} must be powered at 1.8V.
- V_{CCO} for HD I/O banks must be powered in accordance with standard device guidance.
- V_{CCAUX} and V_{CCAUX_HDIO} should be powered from a common supply source, although V_{CCAUX} can be fed separately through a current sense resistor for SEL monitoring and mitigation.
- V_{CCAUX_HPIO} must be powered at 1.2V for all used and unused HP I/O pins.
- V_{CCO} must be powered at 1.2V for all used and unused HP I/O pins.
- V_{CCAUX_HPIO} and V_{CCO} for HP I/O banks must be shared.
- For XQ UltraScale+ FPGAs only, the bank 0 voltage (V_{CCO_0}) must be 1.5V or 1.8V, and configuration is limited to the supported configuration modes listed in FPGA Configuration Modes.

I/O Standards Checklist

- DCI versions of the LVAUX I/O standards are not supported.
- LVCMOS12_LVAUX only supports a drive strength of 8 mA.

- SSTL12_LVAUX, DIFF_SSTL12_LVAUX, AIO_LVAUX, and DIFF_AIO_LVAUX only support the 40Ω source termination feature (OUTPUT_IMPEDANCE attribute) and on-die termination (ODT) attribute of 40Ω or 60Ω.
- LVDS12_LVAUX must have differential termination turned on and set to 100Ω (attributes DIFF_TERM = TRUE and DIFF_TERM_ADV = TERM_100).
- ANALOG and ANALOG_SE I/O standards are not supported in LVAUX mode HP I/O banks. (Instead, if HD I/O are available in the device, consider routing external analog inputs through an HD I/O.)

Power Checklist

- Devices operating in LVAUX mode require approximately the same amount of power as standard operating mode. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to determine the power consumption of your device.
- Devices operating in LVAUX mode draw more current than standard operating mode. See Chapter 3: Estimating Power for the methodology to calculate the current drawn from a device in LVAUX mode.

Vivado Design Suite Checklist

- All used HP I/O pins must use an LVAUX I/O standard listed in SelectIO Resources. You cannot apply non-LVAUX I/O standards to HP I/O pins when using the device in LVAUX mode.
- Design must be completed in Vivado Design Suite 2019.2 or later.
- IBUF_LOW_PWR attribute on all LVAUX HP I/O pins must be set to FALSE.

Memory Checklist

- DDR4 component memory is the only DDR support for PL operating in LVAUX mode, with the supported maximum speeds as identified in this document in Chapter 5: Memory Interface Guidelines.
- DDR4 memory interfaces must be generated through the IP catalog in the Vivado tools with a special LVAUX Tcl command. See Chapter 4: Vivado Tools Requirements and Design Guidelines for more information.

Chapter 2

Hardware Requirements and Guidelines for LVAUX Mode

This chapter discusses the deviations from the published specifications and guidance that must be made to operate the device in LVAUX mode. The deviations outlined in this chapter override any conflicting guidance that could be found in the published UltraScale+ device data sheets. When using the device in standard operating mode and for parameters not listed in this section, refer to the standard specifications listed in References. The LVAUX mode guidance provided in this section includes the deviations related to:

- Data sheet specifications and PCB guidance on voltage supply levels and connectivity of V_{CCAUX_IO}, V_{CCAUX_HDIO}, and for the HP I/O banks, V_{CCAUX_HPIO}, and V_{CCO}.
- Supported LVAUX HP I/O standards, their detailed performance specifications, and guidance for selecting these standards in the Vivado tools.

DC and AC Switching Characteristics

Absolute Maximum Ratings

The absolute maximum ratings for V_{CCAUX_HPIO} and V_{CCAUX_HDIO} are identified in the following table.

Table 5: **Absolute Maximum Ratings**

Symbol	Description[1]	Min	Max	Units
VCCAUX_HPIO	Auxiliary supply voltage for the HP I/O banks	–0.500	2.000	V
VCCAUX_HDIO[2]	Auxiliary supply voltage for the HD I/O banks	–0.500	2.000	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCAUX_HDIO} must be connected to V_{CCAUX}.

Recommended Operating Conditions

Table 6: **Recommended Operating Conditions**

Symbol	Description[1, 2]	Min	Typ	Max	Units
V_{CCAUX_HDIO}[3]	Auxiliary HD I/O supply voltage	1.746	1.800	1.854	V
V_{CCAUX_HPIO}	Auxiliary HP I/O supply voltage	1.164	1.200	1.236	V
V_{CCO}[4]	Supply voltage for HP I/O banks	1.164	1.200	1.236	V

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult the *UltraScale Architecture PCB Design User Guide* (UG583).
3. V_{CCAUX_HDIO} must be connected to V_{CCAUX}.
4. For HP I/O banks, V_{CCAUX_HPIO} must be connected to V_{CCO}.

Table 7: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA

Power Guidelines

The following table describes the typical quiescent supply current from the V_{CCAUX_HPIO} and V_{CCAUX_HDIO} power supplies. These numbers are pessimistic estimates. The actual quiescent supply current will most likely be lower than the values shown here.

Table 8: **Typical Quiescent Supply Current**

Symbol	Description[1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
XQ Ruggedized Kintex UltraScale+ FPGAs							
I_{CCAUX_HPIOQ} and I_{CCAUX_HDIOQ}	Quiescent V_{CCAUX_HPIO} and V_{CCAUX_HDIO} supply current	XQKU5P	32	32	N/A	32	mA
		XQKU15P	74	74	N/A	74	mA
XQ Ruggedized Virtex UltraScale+ FPGAs							
I_{CCAUX_HPIOQ}	Quiescent V_{CCAUX_HPIO}	XQVU3P	62	62	62	62	mA
		XQVU7P	124	124	124	124	mA
		XQVU11P	79	79	79	79	mA

Table 8: **Typical Quiescent Supply Current** *(cont'd)*

Symbol	Description[1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
XQ Ruggedized Zynq UltraScale+ MPSoCs							
I_{CCAUX_HPIOQ} and I_{CCAUX_HDIOQ}	V_{CCAUX_HPIO} and V_{CCAUX_HDIO} supply current	XQZU3EG	26	26	N/A	26	mA
		XQZU5EV	32	32	N/A	32	mA
		XQZU7EV	56	56	N/A	56	mA
		XQZU9EG	33	33	N/A	33	mA
		XQZU11EG	56	56	N/A	56	mA
		XQZU15EG	33	33	N/A	33	mA
		XQZU19EG	74	74	N/A	74	mA
XQ Ruggedized Zynq UltraScale+ RFSoCs							
I_{CCAUX_HPIOQ} and I_{CCAUX_HDIOQ}	V_{CCAUX_HPIO} and V_{CCAUX_HDIO} supply current	XQZU21DR	58	58	N/A	58	mA
		XQZU28DR	58	58	N/A	58	mA
		XQZU29DR	58	58	N/A	58	mA
		XQZU48DR	58	58	58	58	mA
		XQZU49DR	58	58	58	58	mA
		XQZU65DR	36	36	36	36	mA
		XQZU67DR	36	36	36	36	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, and all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified. See Chapter 3: Estimating Power to estimate power consumption of HP I/O banks and HD I/O banks in LVAUX mode. Typical values depend upon your configuration. To accurately estimate all PS and PL supply currents, use XPE.

PL/FPGA Power-On/Off Power Supply Sequencing

To achieve minimum current draw and to ensure that the I/Os are 3-stated at power-on, use the following recommended power-on sequence:

1. V_{CCINT}
2. V_{CCINT_IO} and V_{CCBRAM}
3. V_{CCAUX} and V_{CCAUX_HDIO}
4. V_{CCAUX_HPIO}
5. V_{CCO}

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. V_{CCAUX}/ V_{CCAUX_HDIO} and V_{CCO} for HD I/O banks have the same recommended voltage levels and can be powered by the same supply and ramped simultaneously. V_{CCAUX_HPIO} and V_{CCO} for HP I/O banks have the same recommended voltage levels, and they *must* be powered by the same supply and ramped simultaneously. V_{CCAUX} must be connected to V_{CCAUX_HDIO}. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

Power Supply Requirements

The following table shows the minimum current, in addition to I_{CCQ} maximum, required by each UltraScale+ device for proper power-on and configuration. If these current minimums are met, the device powers on after all supplies have passed through their power-on and reset threshold voltages. These numbers are pessimistic estimates. The actual power-on current will most likely be lower than the values shown here. The device must not be configured until after V_{CCINT} is applied. After the device is initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) and instructions from Chapter 3: Estimating Power to estimate current drain on these supplies. XPE can be used to estimate power-on current for all voltage supplies.

Table 9: **Power-on Current by Device**

I_{CC} Min =	$I_{CCINTMIN}$	I_{CCINT_IOMIN} + $I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN}$	$I_{CCAUX\_HDIOMIN}$	$I_{CCAUX\_HPIOMIN}$	$I_{CCSDFECMIN}$	Units
I_{CCQ} +	I_{CCINTQ} +	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} +	I_{CCOQ} +	I_{CCAUXQ} +	I_{CCAUX_IOQ} +	I_{CCAUX_IOQ} +	$I_{CCSDFECQ}$ +	
XQ Ruggedized Kintex UltraScale+ FPGAs								
XQKU5P	770	305	50	515	515	515	N/A	mA
XQKU15P	3433	1145	96	1240	1240	1240	N/A	mA
XQ Ruggedized Virtex UltraScale+ FPGAs								
XQVU3P	2000	670	50	350	350	350	N/A	mA
XQVU7P	4000	1340	100	700	700	700	N/A	mA
XQVU11P	6549	2194	164	1146	1146	1146	N/A	mA
XQ Ruggedized Zynq UltraScale+ MPSoCs								
XQZU3EG	464	155	50	111	111	111	N/A	mA
XQZU5EV	770	257	50	386	386	386	N/A	mA
XQZU7EV	1514	505	50	362	362	362	N/A	mA
XQZU9EG	1800	600	50	650	650	650	N/A	mA
XQZU11EG	1961	654	55	709	709	709	N/A	mA
XQZU15EG	2242	748	63	810	810	810	N/A	mA
XQZU19EG	3433	1145	96	1240	1240	1240	N/A	mA
XQ Ruggedized Zynq UltraScale+ RFSoCs								
XQZU21DR	4500	770	50	320	320	320	250	mA

Table 9: **Power-on Current by Device** *(cont'd)*

I_{CC} Min =	$I_{CCINTMIN}$	I_{CCINT_IOMIN} + $I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN}$	$I_{CCAUX\_HDIOMIN}$	$I_{CCAUX\_HPIOMIN}$	$I_{CCSDFECMIN}$	Units
I_{CCQ} +	I_{CCINTQ} +	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} +	I_{CCOQ} +	I_{CCAUXQ} +	I_{CCAUX_IOQ} +	I_{CCAUX_IOQ} +	$I_{CCSDFECQ}$ +	
XQZU28DR	4500	770	50	320	320	320	250	mA
XQZU29DR	4500	1020	50	320	320	320	N/A	mA
XQZU48DR	4500	1020	50	320	320	320	250	mA
XQZU49DR	4500	1020	50	320	320	320	N/A	mA
XQZU65DR	3516	602	50	261	261	261	N/A	mA
XQZU67DR	3516	602	50	261	261	261	N/A	mA

Table 10: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCAUX_HPIO}	Ramp time from GND to 95% of V_{CCAUX_HPIO}	0.2	40	ms
T_{VCCAUX_HDIO}	Ramp time from GND to 95% of V_{CCAUX_HDIO}	0.2	40	ms

DC I/O Levels

Table 11: **SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard[1]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS12_LVAUX	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	8.0	8.0
SSTL12_LVAUX	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
MIPI_DPHY_ LVAUX_LP	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.

Table 12: **DC Input Levels for Single-ended AIO12_LVAUX I/O Standard**

I/O Standard[1]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
AIO12_LVAUX	–0.300	V_{REF} – 0.068[2]	V_{REF} + 0.068[2]	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. $V_{REF} = V_{CCO}/4$

Table 13: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]			V_{ILHS}[3]	V_{IHHS}[3]	V_{OCM} (V)[4]			V_{OD} (V)[5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
MIPI_DPHY_LVAUX_HS[6]	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. High-speed option for MIPI_DPHY_LVAUX. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 14: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_SSTL12_LVAUX	0.300	0.600	0.63	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.0	–8.0

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 15: **DC Input Levels for Differential AIO I/O Standard**

I/O Standard[1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_AIO12_LVAUX	0.22	0.30	0.38	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 16: **DC Output Levels for Single-ended and Differential AIO_LVAUX Standards**

Symbol	Description[1, 2]	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 17)	24	40	56	Ω
R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 17)	24	40	56	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 17: **Definitions for DC Output Levels for Single-ended and Differential AIO12_LVAUX Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}[1]	DC output mid-measurement level (for IV curve linearity)	0.8 x V_{CCO}	V

Notes:

1. The driver for the V_{OM_DC} level using the AIO12_LVAUX standard is similar to the driver for the POD12 standard.

LVDS12_LVAUX

The following table contains the DC specifications for the LVDS12_LVAUX I/O standard. When the LVDS12_LVAUX I/O standard is used as a transmitter (TX), it can drive the reduced range receivers (RX) specified in the IEEE Std 1596.3-1996. AMD recommends placing TX and RX on the same PCB to minimize the ground difference between them.

Table 18: **LVDS12_LVAUX DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage for HP I/O banks		1.164	1.200	1.236	V
V_{CCAUX_HPIO}	Auxiliary HP I/O supply		1.164	1.200	1.236	V
V_{OH}	Output High voltage for Q and $\overline{Q}$ signals	R_T = 100Ω across Q and $\overline{Q}$ signals	–	–	1.236	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$ signals	R_T = 100Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}[1]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	150	222	300	mV
V_{OCM}[1]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	0.900	1.000	1.200	V
V_{IDIFF}[2]	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.00V	100	222	400[2]	mV
V_{ICM_DC}[3, 4]	Input common-mode voltage (DC coupling)		0.825	1.200	1.380	V
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks		–50%	100	50%	Ω

Notes:

1. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
3. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
4. AC coupled common mode (V_{ICM_AC}) is not supported by the LVDS12_LVAUX I/O standard.

IOB High Performance Switching Characteristics

The IOB HP switching characteristics for the LVAUX I/O standards are mostly equivalent to their non-LVAUX counterparts available in the UltraScale+ device data sheets. The following table shows the LVAUX I/O standards and their non-LVAUX versions.

Table 19: **LVAUX and Non-LVAUX I/O Standards**

LVAUX Standard	Original Standard
LVCMOS12_LVAUX	LVCMOS12
SSTL12_LVAUX	SSTL12
DIFF_SSTL12_LVAUX	DIFF_SSTL12
LVDS12_LVAUX[1]	LVDS
MIPI_DPHY_LVAUX_LP	MIPI_DPHY_DCI_LP
MIPI_DPHY_LVAUX_HS	MIPI_DPHY_DCI_HS
AIO12_LVAUX	POD12
DIFF_AIO12_LVAUX	DIFF_POD12

Notes:

1. For compatibility of LVDS12_LVAUX with LVDS, check Table 11: SelectIO DC Input and Output Levels for HP I/O Banks and LVDS12_LVAUX for restrictions and for comparison to interfacing LVDS transmitter/receiver specifications.

I/O Guidelines

This section discusses the features of the LVAUX I/O standards. For parameters not listed in this section, refer to the standard specifications listed in *UltraScale Architecture SelectIO Resources User Guide* (UG571). The LVAUX I/O standards are listed in the following table. These standards are available for HP I/O banks only. No DCI versions of the LVAUX I/O standards are available.

- Single-ended LVAUX I/O standards
  - LVCMOS12_LVAUX
  - SSTL12_LVAUX
  - MIPI_DPHY_LVAUX_LP
  - AIO12_LVAUX
- Differential LVAUX I/O standards
  - LVDS12_LVAUX
  - DIFF_AIO12_LVAUX
  - DIFF_SSTL12_LVAUX

  - MIPI_DPHY_LVAUX_HS
- LVAUX I/O standards that support uncalibrated termination for HP I/O banks
  - SSTL12_LVAUX
  - DIFF_SSTL12_LVAUX
  - AIO12_LVAUX
  - DIFF_AIO12_LVAUX

***Note*:** System monitor external analog inputs (I/O standard = ANALOG or ANALOG_SE) are not supported in LVAUX mode HP I/O banks. Instead, if HD I/O are available in the device, consider routing external analog inputs through an HD I/O.

The LVAUX I/O standards are very similar to industry I/O standards (for example, SSTL12_LVAUX is derived from the SSTL12 I/O standard). The differences are primarily to optimize the design using LVAUX mode.

LVCMOS12_LVAUX

LVCMOS12_LVAUX is an LVCMOS standard. See the LVCMOS section in *UltraScale Architecture SelectIO Resources User Guide* (UG571) for information on how LVCMOS standards typically function. Except for the differences highlighted in this section, LVCMOS12_LVAUX functions the same way as LVCMOS12.

- LVCMOS12_LVAUX is only available for HP I/O banks.
- LVCMOS12_LVAUX only has a drive strength of 8 mA. Unlike the other LVCMOS standards, it does not support drive strengths of 4 mA or 12 mA.

Table 20: **LVCMOS12_LVAUX Allowed Attributes**

Attributes	Primitives			
	IBUF		OBUF/OBUFT/IOBUF	
	HP I/O Banks		HP I/O Banks	
	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	**LVCMOS12_LVAUX**		**LVCMOS12_LVAUX**	
DRIVE	N/A		8	8
SLEW	N/A		FAST, MEDIUM, SLOW	SLOW

SSTL12_LVAUX and DIFF_SSTL12_LVAUX

SSTL12_LVAUX and DIFF_SSTL12_LVAUX are SSTL standards. See the SSTL section in the*UltraScale Architecture SelectIO Resources User Guide* (UG571) for information on how SSTL standards typically function. Except for the differences highlighted in this section, SSTL12_LVAUX and DIFF_SSTL12_LVAUX function the same way as SSTL12 and DIFF_SSTL12.

- SSTL12_LVAUX and DIFF_SSTL12_LVAUX are SSTL I/O standards for 1.2V.
- SSTL12_LVAUX and DIFF_SSTL12_LVAUX only support DDR4 memory. They do not support the Micron Next Generation RLDRAM3 memory.
- SSTL12_LVAUX and DIFF_SSTL12_LVAUX are only available for HP I/O banks.
- SSTL12_LVAUX and DIFF_SSTL12_LVAUX supports 40Ω for the source termination feature (OUTPUT_IMPEDENCE). They do not support a 60Ω or 48Ω source termination feature.
- SSTL12_LVAUX and DIFF_SSTL12_LVAUX support ODT values of RTT_40 and RTT_60 only. They do not support an ODT value of RTT_NONE.
- DIFF_SSTL_LVAUX only supports DQS_BIAS set to FALSE.

Table 21: **SSTL12_LVAUX Allowed Attributes**

Attributes	Primitives					
	IBUF/IBUF3/IBUFDS/ IBUFDSE3		OBUF/OBUFT		IOBUF/IOBUFE3/ IOBUFDS/IOBUFDSE3	
	HP I/O Banks		HP I/O Banks		HP I/O Banks	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	**SSTL12_LVAUX**		**SSTL12_LVAUX**		**SSTL12_LVAUX**	
SLEW	N/A		FAST MEDIUM SLOW	SLOW	FAST MEDIUM SLOW	SLOW
ODT	RTT_40 RTT_60	RTT_40	N/A		RTT_40 RTT_60	RTT_40
OUTPUT_IMPEDENCE	N/A		RDRV_40_40	RDRV_40_40	RDRV_40_40	RDRV_40_40
IOSTANDARD	**DIFF_SSTL12_LVAUX**		**DIFF_SSTL12_LVAUX**		**DIFF_SSTL12_LVAUX**	
SLEW	N/A		FAST MEDIUM SLOW	SLOW	FAST MEDIUM SLOW	SLOW
DQS_BIAS	FALSE	FALSE	N/A		FALSE	FALSE
ODT	RTT_40 RTT_60	RTT_40	N/A		RTT_40 RTT_60	RTT_40
OUTPUT_IMPEDENCE	N/A		RDRV_40_40	RDRV_40_40	RDRV_40_40	RDRV_40_40

AIO12_LVAUX and DIFF_AIO12_LVAUX

The adaptive I/O (AIO) standards are intended to provide 1.2V I/O standards for LVAUX mode that are similar to the POD12 and DIFF_POD12 I/O standards. See the POD12 and POD10 section in the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for information on how POD standards typically function. The differences between AIO12_LVAUX/ DIFF_AIO12_LVAUX and POD12/DIFF_POD12 are highlighted in this section.

- The AIO12_LVAUX and DIFF_AIO12_LVAUX standards support the 40Ω source termination feature (OUTPUT_IMPEDANCE). They do not support the 60Ω or 48Ω source termination feature used by POD12 and DIFF_POD12.
- The AIO12_LVAUX and DIFF_AIO12_LVAUX standards support ODT values of RTT_40 and RTT_60. They do not support an ODT value of RTT_NONE.
- The AIO12_LVAUX and DIFF_AIO12_LVAUX standards only support a PRE_EMPHASIS of RDRV_240. They do not support a PRE_EMPHASIS value of RDRV_NONE used by POD12 and DIFF_POD12.
- AMD does not support the DCI versions of AIO12_LVAUX and DIFF_AIO12_LVAUX.
- AIO12_LVAUX and DIFF_AIO12_LVAUX are only available for HP I/O banks and use V_{REF}.

Table 22: **AIO Allowed Attributes**

Attributes	Primitives					
	IBUF/IBUF3/IBUFDS/ IBUFDSE3		OBUF/OBUFT		IOBUF/IOBUFE3/IOBUFDS/ IOBUFDSE3	
	HP I/O Banks		HP I/O Banks		HP I/O Banks	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	**AIO_LVAUX DIFF_AIO12_LVAUX**		**AIO_LVAUX DIFF_AIO12_LVAUX**		**AIO_LVAUX DIFF_AIO12_LVAUX**	
SLEW	N/A		FAST MEDIUM SLOW	SLOW	FAST MEDIUM SLOW	SLOW
PRE_EMPHASIS	N/A		RDRV_240	RDRV_240	RDRV_240	RDRV_240
DQS_BIAS	FALSE	FALSE	N/A		FALSE	FALSE
ODT	RTT_40 RTT_60	RTT_40	N/A		RTT_40 RTT_60	RTT_40
OUTPUT_IMPEDENCE	N/A		RDRV_40_40	RDRV_40_40	RDRV_40_40	RDRV_40_40

Table 23: **Allowed Combinations of OUTPUT_IMPEDENCE, ODT, and PRE_EMPHASIS**

OUTPUT_IMPEDENCE	SLEW	ODT	PRE_EMPHASIS
RDRV_40_40 (40Ω)	FAST	RTT_40	RDRV_240
RDRV_40_40 (40Ω)	FAST	RTT_60	RDRV_240

Table 24: **Allowed Combinations of OUTPUT_IMPEDENCE and PRE_EMPHASIS**

OUTPUT_IMPEDENCE	SLEW	PRE_EMPHASIS
RDRV_40_40 (40Ω)	FAST	RDRV_240

LVDS12_LVAUX

LVDS12_LVAUX is intended to provide a 1.2V standard compatible with LVDS standards. See the LVDS and LVDS_25 section in *UltraScale Architecture SelectIO Resources User Guide* (UG571) for information on how LVDS standards typically function. The differences between LVDS12_LVAUX and LVDS are highlighted in this section.

- LVDS12_LVAUX requires V_{CCO} = 1.2V.
- LVDS12_LVAUX only supports a DQS_BIAS value of FALSE.
- LVDS12_LVAUX only supports a DIFF_TERM value of TRUE. When using LVDS12_LVAUX, you must explicitly set the DIFF_TERM to TRUE because the default value is FALSE. This automatically maps the DIFF_TERM_ADV attribute to TERM_100.
- LVDS12_LVAUX has internal differential termination (100Ω) that is turned on by default when in 3-state/receiving mode for OBUFTDS, IBUFDS, and IOBUFDS. LVDS12_LVAUX does not have a driving mode.
- LVDS12_LVAUX is only available in HP I/O banks.
- AC coupled common mode (V_{ICM_AC}) is not supported by the LVDS12_LVAUX I/O standard.

Table 25: **LVDS12_LVAUX Allowed Attributes**

Attributes	Primitives			
	IBUFDS		OBUFDS	
	HP I/O Banks		HP I/O Banks	
	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	**LVDS12_LVAUX**		**LVDS12_LVAUX**	
EQUALIZATION	EQ_NONE	EQ_NONE	N/A	
DQS_BIAS	FALSE	FALSE	N/A	
DIFF_TERM	TRUE	FALSE[1]	N/A	
DIFF_TERM_ADV	TERM_100	TERM_NONE[1]	N/A	

Notes:

1. You must explicitly change DIFF_TERM to TRUE. This automatically maps DIFF_TERM_ADV to TERM_100.

Table 26: **Internal Differential Termination Behavior**

Primitives	Driving	3-state/Receiving
OBUFDS	N/A	N/A
OBUFTDS	N/A	Internal differential termination is ON.
IBUFDS	N/A	When DIFF_TERM = TRUE or DIFF_TERM_ADV = TERM_100, internal differential termination is ON. This is the only allowed behavior. DIFF_TERM is not allowed to be set to FALSE. You must explicitly set DIFF_TERM to TRUE.
IOBUFDS	N/A	Internal differential termination is ON, irrespective of the DIFF_TERM or DIFF_TERM_ADV attributes.

MIPI_DPHY_LVAUX

MIPI_DPHY_LVAUX is a MIPI_DPHY standard. See *UltraScale Architecture SelectIO Resources User Guide* (UG571) for information on how a MIPI_DPHY standard typically functions. Except for the differences highlighted in this section, MIPI_DPHY_LVAUX functions similar to MIPI_DPHY_DCI.

- MIPI_DPHY_LVAUX is not a DCI standard. AMD does not support the DCI version of MIPI_DPHY_LVAUX.
- MIPI_DPHY_LVAUX are only available in the HP I/O banks.

Table 27: **MIPI_DPHY_LVAUX Allowed Attributes**

Attributes	Primitives			
	IBUFDS_DPHY		OBUFDS_DPHY	
	HP I/O Banks		HP I/O Banks	
	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	**MIPI_DPHY_LVAUX**		**MIPI_DPHY_LVAUX**	
SLEW	N/A		N/A	
DIFF_TERM	TRUE	FALSE[1]	N/A	
DIFF_TERM_ADV	TERM_100	TERM_NONE[1]	N/A	

Notes:

1. You must explicitly change DIFF_TERM to TRUE. This automatically maps DIFF_TERM_ADV to TERM_100.

Rules for Combining I/O Standards in the Same Bank

See the *Rules for Combining I/O Standards in the Same Bank* section in the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for details on how to combine different input, output, and bidirectional standards in the same bank. When using the device in LVAUX mode, all HP I/O banks must be set to an LVAUX I/O standard. The following table summarizes the V_{CCO} and V_{REF} requirements for each LVAUX I/O standard. AMD recommends to separate LVDS12_LVAUX and MIPI_DPHY_LVAUX I/O pins from memory interfaces.

Table 28: **Rules for Combining I/O Standards in the Same Bank**

I/O Standard	I/O Bank Availability	V_{CCO} (V) for HP I/O Banks			V_{REF} (V)
		Output	Input	Input with DIFF_TERM_ADV and DIFF_TERM Support	Input
LVCMOS12_LVAUX	HP	1.2	1.2	N/A	N/A
SSTL12_LVAUX	HP	1.2	1.2	N/A	0.6V
DIFF_SSTL12_LVAUX	HP	1.2	1.2	N/A	N/A
AIO12_LVAUX	HP	1.2	1.2	N/A	0.3V
DIFF_AIO12_LVAUX	HP	1.2	1.2	1.2	N/A
LVDS12_LVAUX	HP	1.2	1.2	1.2	N/A
MIPI_DPHY_LVAUX	HP	1.2	1.2	1.2	N/A

Notes:

1. System monitor external analog inputs (I/O standard = ANALOG or ANALOG_SE) are not supported in LVAUX mode HP I/O banks. Instead, if HD I/O are available in the device, consider routing external analog inputs through an HD I/O.

The following table summaries the DRIVE and SLEW attribute options and bidirectional buffer availability for each LVAUX I/O standard.

Table 29: **Attributes Options and Bidirectional Buffer Availability**

I/O Standard	I/O Bank Type	Output Slew		Output Drive		Bidirectional Buffers	Termination Type	
		HP I/O Banks		HP I/O Banks			Input	Output
		Allowed Values	Default	Allowed Values	Default			
LVCMOS12_LVAUX	HP	SLOW MEDIUM FAST	SLOW	8	8	Yes	None	None
SSTL12_LVAUX	HP	SLOW MEDIUM FAST	SLOW	N/A	N/A	Yes	Split	Driver
DIFF_SSTL12_LVAUX	HP	SLOW MEDIUM FAST	SLOW	N/A	N/A	Yes	Split	Driver
LVDS12_LVAUX[1]	HP	N/A	N/A	N/A	N/A	Yes	DIFF_TERM_100	None
DIFF_AIO12_LVAUX	HP	SLOW MEDIUM FAST	SLOW	N/A	N/A	Yes	Single	Driver
AIO12_LVAUX	HP	SLOW MEDIUM FAST	SLOW	N/A	N/A	Yes	Single	Driver
MIPI_DPHY_LVAUX	HP	N/A	N/A	N/A	N/A	No	DIFF_TERM_100	Driver

Notes:

1. The bidirectional configuration on these I/O standards is a fixed impedance structure optimized to 100Ω differential. They are intended to only be used in point-to-point transmissions that do not have turn-around timing requirements.
2. System monitor external analog inputs (I/O standard = ANALOG or ANALOG_SE) are not supported in LVAUX mode HP I/O banks. Instead, if HD I/O are available in the device, consider routing external analog inputs through an HD I/O.

Termination Options for Simultaneous Switching Noise Analysis

The following table lists all of the default terminations for each of the LVAUX I/O standards supported by the XQ ruggedized UltraScale+ devices when using the SSN predictor tool in the Vivado Design Suite.

Table 30: **Default Termination for SSN Noise Analysis by I/O Standard**

I/O Standard	Drive	Termination Option
DIFF_AIO12_LVAUX	–	Far V_{CCO} 40Ω
DIFF_SSTL12_LVAUX	–	Far V_{TT} 40Ω
LVCMOS12_LVAUX	8	None
LVDS12_LVAUX	–	Far differential 100Ω
AIO12_LVAUX	–	Far V_{CCO} 40Ω
SSTL12_LVAUX	–	Far V_{TT} 40Ω

Packaging and Pinouts

The UltraScale+ device packaging and pinout user guides describe the standard packaging and pinout specifications. This section highlights the changes necessary when operating in LVAUX mode.

Pin Definitions

The standard pin definitions are specified in the UltraScale+ device packaging and pinout user guides. The pin definitions for V_{CCAUX_HPIO} and V_{CCAUX_HDIO} are defined in the following table.

Table 31: **Pin Definitions**

Pin Name	Type	Direction	Description
VCCAUX_HPIO	Dedicated	N/A	Auxiliary power-supply pins for the HP I/O banks. V_{CCAUX_HPIO} must *not* be connected to V_{CCAUX}.
VCCAUX_HDIO	Dedicated	N/A	Auxiliary power-supply pins for the HD I/O banks. V_{CCAUX_HDIO} must be connected to V_{CCAUX}.

Device Diagrams

The UltraScale+ device packaging and pinout user guides contain the package-device configuration/power diagrams for all XQ ruggedized UltraScale+ devices. The power pins labeled VCCAUX_IO show all the combined VCCAUX_HPIO and VCCAUX_HDIO pins under a single label. To determine whether a VCCAUX_IO pin is a VCCAUX_HDIO or VCCAUX_HPIO pin, cross reference the package file of the device (in the Package File Portal).

PCB Design Guidelines

The PCB design guidelines for the LVAUX mode are generally the same as for standard mode XQ devices, *except* a separate 1.2V V_{CCAUX_HPIO} power supply with its own decoupling capacitors is required for the VCCAUX_HPIO device power pins.

Refer to *UltraScale Architecture PCB Design User Guide* (UG583) and *UltraScale+ FPGAs and Zynq Ultrascale+ Devices Schematic Review Checklist* (XTP427) for PCB guidelines. Refer to the following section for decoupling capacitor recommendations which include recommendations for the V_{CCAUX_HPIO} supply.

Decoupling Capacitors

The recommended decoupling capacitor quantities for the specific XQ ruggedized UltraScale+ device-packages in LVAUX mode are listed in the tables below. The optimized quantities of PCB decoupling capacitors assume that the voltage regulators have stable output voltages and meet the regulator manufacturer's minimum output capacitance requirements.

The assumptions used for the decoupling quantities are shown below. If any of these assumptions significantly differ from the actual design, simulations are recommended to determine the actual amount of required capacitance, which could be higher or lower. The decoupling recommendations are designed for optimal performance between roughly 100 kHz and 10–20 MHz.

Because device capacitance requirements vary with programmable logic and I/O utilization, PCB decoupling guidelines are provided on a per-device basis based on very high utilization so as to cover a majority of use cases. Resource usage consists (in part) of:

- 80% of LUTs and registers at 245 MHz and 25% toggle rate
- 80% block RAM and DSP at 491 MHz and 50% toggle rate
- 50% MMCM and 25% PLL at 500 MHz
- 25% I/O at SSTL 1.2/1.35 at 1200 MHz and 40% toggle rate
- 75% I/O at POD 1.2 at 1200 MHz DDR mode and 40% toggle rate

Different step loads are assumed for each main voltage rail. The step load is the percentage of the dynamic current that is expected to be demanded at any given switching event. The following table lists the step load percentage used when calculating device capacitance requirements.

Table 32: **Step Load for Device Capacitance**

Voltage Rail	Step Load
V_{CCINT}/V_{CCINT_IO}	25%
V_{CCBRAM}	40%
V_{CCAUX}/V_{CCAUX_HDIO}	100%
V_{CCAUX_HPIO}	100%
V_{CCO} (HD/HP/PS)	100%
$V_{CC\_PSTINFP}/V_{CC\_PSINTLP}$	33%

The slew rate of the switching event is dependent on the design, and can be estimated to be between 1 ns and 100 ns (or longer). Smaller current designs generally have faster current slew rates, while larger designs tend to have slower slew rates. A general rule of thumb for high-current designs can be considered to be 0.25 ns per amp (or 4 A/ns) of step current. The Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) is used to estimate the current on each power rail.

See the Recommended Operating Conditions in this document for the operating range of the V_{CCAUX_HPIO} supply. Otherwise, see the *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922), *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923), *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925), or *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926) for the operating range for all other power rails. The PCB designer should ensure that the AC ripple plus the DC tolerance of the voltage regulator do not exceed the operating range.

The capacitor numbers shown in this user guide are based on the following assumptions:

- VCCINT operating range from the data sheet = 3%
- Assumed DC tolerance = 1%
- Therefore, allowable AC ripple = 3% – 1% = 2%

The target impedance is calculated using the 2% AC ripple along with the current estimates from XPE for the above resource utilization to arrive at the capacitor recommendations. The equation for target impedance is:

$$Z_{target} = VoltageRailValue \times (\%\ Ripple/100) / StepLoadCurrent$$

V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} capacitors are listed as the quantity per device, while V_{CCO} capacitors are listed as the quantity per I/O bank. Device performance at full utilization is equivalent across all devices when using these recommended networks.

The decoupling capacitor tables below do not provide the decoupling networks required for the GTY or GTH transceiver power supplies. For this information, refer to the *UltraScale Architecture GTY Transceivers User Guide* (UG578) or *UltraScale Architecture GTH Transceivers User Guide* (UG576).

TIP: *Refer to the UltraScale+ FPGAs and Zynq Ultrascale+ Devices Schematic Review Checklist (XTP427) for a comprehensive checklist for schematic review which complements this user guide.*

Recommended decoupling capacitor quantities in the tables below are based on the following capacitors and capacitor placement.

Table 33: **Recommended PCB Capacitor Specifications and Placement Guidelines for XQ Devices**

Nominal Value (µF)	Case Size	Temp/Change (%)	Manufacturer	Manufacturer Part Number	Ideal Placement to Device[1]
330	7343	TantPoly	Kemet	T541X337M010AH6510	1–4”
47	7343	TantPoly	Kemet	T541X476M035AH6510	0.5–3”
22	1210	X7R	Kemet	C1210C226K8RAL7800	0.5–2”
2.2	0805	X7R	Kemet	C0805C225K4RAL7800	0–1”
0.47	0603	X7R	Kemet	C0603C474K4RAL7867	0–1”
0.1	0402	X7R	Kemet	C0402C104K4RAL7867	0–1”

Notes:

1. Ideal placement is to minimize distance between capacitor and device.

The following are recommended decoupling capacitor quantities based on the above capacitors and assumptions.

Table 34: **XQ Ruggedized Kintex UltraScale+ FPGA Decoupling Capacitor Recommendations for LVAUX Mode**

Device-Package	V_{CCINT} or V_{CCINT}/V_{CCINT_IO}/V_{CCBRAM}[1]						V_{CCINT_IO}/ V_{CCBRAM}[2]			V_{CCAUX}/ V_{CCAUX_HDIO}[3]			V_{CCAUX_HPIO}			HDIO/ HPIO V_{CCO} (per bank)[4]	
	330 µF	47 µF	22 µF	2.2 µF	0.47 µF	0.1 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF
XQKU5P-SFRB784	2	4	5	17	36	42	1	1	1	1	1	1	1	1	1	1	1
XQKU5P-FFRB676	2	3	5	10	11	9	1	1	1	1	1	1	1	1	1	1	1
XQKU15P-FFRA1156	2	4	7	14	22	34	1	1	1	1	1	1	1	1	1	1	1
XQKU15P-FFRE1517	2	4	7	14	22	34	1	1	1	1	1	1	1	1	1	1	1

Notes:

1. Applicable for standalone V_{CCINT} for the -1LI (0.72V) speed grade; and applicable for combined V_{CCINT}/V_{CCINT_IO}/V_{CCBRAM} for -2I (0.85V), -1I (0.85V), -1M (0.85V), and -1LI (0.85V) speed grades. The capacitors listed are the total number of capacitors for each scenario.
2. Applicable for combined V_{CCINT_IO} and V_{CCBRAM} for the -1LI (0.72V) speed grade. The capacitors listed are the total number of capacitors for the combined rail.
3. V_{CCAUX} and V_{CCAUX_HDIO} must share the same plane on the PCB. The capacitors listed are the total number of capacitors for the combined rail.
4. The 22 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 35: **XQ Ruggedized Virtex UltraScale+ FPGA Decoupling Capacitor Recommendations for LVAUX Mode**

Device-Package	V_{CCINT} or $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$[1]						V_{CCINT_IO}/V_{CCBRAM}[2]			V_{CCAUX}[3]			V_{CCAUX_IO}			HPIO V_{CCO} (per bank)[4]	
	330 µF	47 µF	22 µF	2.2 µF	0.47 µF	0.1 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF
XQVU3P-FFRC1517	2	4	7	14	22	34	1	1	1	1	1	1	1	1	1	1	1
XQVU7P-FLRA2104	4	7	13	25	50	100	1	1	2	2	1	1	2	1	1	1	1
XQVU7P-FLRB2104	3	7	13	25	50	100	1	1	2	1	1	1	1	1	1	1	1
XQVU11P-FLRC2104	6	11	21	41	91	199	1	1	2	1	1	1	1	1	1	1	1

Notes:

1. Applicable for standalone V_{CCINT} for the -2LE (0.72V) (0.72V) speed grade; and applicable for combined $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$ for -2I (0.85V), -2LE (0.85V), and -1M (0.85V) speed grades. The capacitors listed are the total number of capacitors for each scenario.
2. Applicable for combined V_{CCINT_IO} and V_{CCBRAM} for the -2LE (0.72V) speed grade. The capacitors listed are the total number of capacitors for the combined rail.
3. V_{CCAUX} and V_{CCAUX_HDIO} must share the same plane on the PCB. The capacitors listed are the total number of capacitors for the combined rail.
4. The 22 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 36: **XQ Ruggedized Zynq UltraScale+ MPSoC Decoupling Capacitor Recommendations for LVAUX Mode**

Devices-Package	V_{CCINT} or $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$[1]						V_{CCINT_IO}/V_{CCBRAM}[2]			V_{CCAUX}/V_{CCAUX_HDIO}[3]			V_{CCAUX_HPIO}			HDIO/HPIO V_{CCO} (per bank)[4]	
	330 µF	47 µF	22 µF	2.2 µF	0.47 µF	0.1 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF
EG Devices																	
XQZU3EG-SFRA484	1	3	1	1	16	2	1	1	1	1	1	1	1	1	1	1	1
XQZU3EG-SFRC784	1	3	1	1	16	2	1	1	1	1	1	1	1	1	1	1	1
XQZU9EG-FFRC900	2	3	6	12	16	22	1	1	1	1	1	1	1	1	1	1	1
XQZU9EG-FFRB1156	2	3	6	12	17	22	1	0	1	1	1	1	1	1	1	1	1
XQZU11EG-FFRC1156	2	4	7	13	20	28	1	1	1	1	1	1	1	1	1	1	1
XQZU11EG-FFRC1760	2	4	7	13	20	28	1	1	1	1	1	1	1	1	1	1	1
XQZU15EG-FFRC900	2	4	7	15	24	40	1	1	1	1	1	1	1	1	1	1	1
XQZU15EG-FFRB1156	2	4	8	15	25	40	1	1	1	1	1	1	1	1	1	1	1
XQZU19EG-FFRB1517	2	4	7	14	22	34	1	1	1	1	1	1	1	1	1	1	1
XQZU19EG-FFRC1760	2	4	7	14	22	34	1	1	1	1	1	1	1	1	1	1	1
EV Devices																	
XQZU5EV-SFRC784	1	3	2	9	26	22	1	1	1	1	1	1	1	1	1	1	1
XQZU5EV-FFRB900	1	2	4	7	5	0	1	1	1	1	1	1	1	1	1	1	1
XQZU7EV-FFRB900	2	3	5	10	11	8	1	1	1	1	1	1	1	1	1	1	1
XQZU7EV-FFRC1156	2	3	5	10	11	9	1	1	1	1	1	1	1	1	1	1	1

Notes:

1. Applicable for standalone V_{CCINT} for the -1LI (0.72V) speed grade; and applicable for combined $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$ for -2I (0.85V), -1I (0.85V), -1M (0.85V), and -1LI (0.85V) speed grades. The capacitors listed are the total number of capacitors for each scenario.
2. Applicable for combined V_{CCINT_IO} and V_{CCBRAM} for the -1LI (0.72V) speed grade. The capacitors listed are the total number of capacitors for the combined rail.
3. V_{CCAUX} and V_{CCAUX_HDIO} must share the same plane on the PCB. The capacitors listed are the total number of capacitors for the combined rail.
4. The 22 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 37: **XQ Ruggedized Zynq UltraScale+ RFSoC Decoupling Capacitor Recommendations for LVAUX Mode**

Device-Package	V_{CCINT} or $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$ [1]						V_{CCINT_IO}/V_{CCBRAM} [2]			V_{CCAUX}/V_{CCAUX_HDIO} [3]			V_{CCAUX_HPIO}			HDIO/HPIO V_{CCO} (per bank) [4]	
	330 µF	47 µF	22 µF	2.2 µF	0.47 µF	0.1 µF	22 µF	2.2 µF	0.47 µF	22 µF	2.2 µF	0.1 µF	22 µF	2.2 µF	0.47 µF	22 µF	02.2 µF
XQZU21DR-FFRD1156	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	1
XQZU28DR-FFRE1156	3	5	9	18	30	55	1	1	1	1	1	1	1	1	1	1	1
XQZU28DR-FFRG1517	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	1
XQZU29DR-FFRF1760	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	1
XQZU48DR-FFRE1156	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	1
XQZU48DR-FSRG1517	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	1
XQZU49DR-FSRF1760	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	1
XQZU65DR-FFRE1156	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	3
XQZU67DR-FFRE1156	3	5	9	18	31	55	1	1	1	1	1	1	1	1	1	1	3

Notes:

1. Applicable for standalone V_{CCINT} for -2LI (0.72V) and -1LI (0.72V) speed grades; and applicable for combined $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$ for -2I (0.85V), -2LI (0.85V), -1I (0.85V), -1M (0.85V), and -1LI (0.85V) speed grades. The capacitors listed are the total number of capacitors for each scenario.
2. Applicable for combined V_{CCINT_IO} and V_{CCBRAM} for -2LI (0.72V), -2LE (0.72V), and -1LI (0.72V) speed grades. The capacitors listed are the total number of capacitors for the combined rail.
3. V_{CCAUX} and V_{CCAUX_HDIO} must share the same plane on the PCB. The capacitors listed are the total number of capacitors for the combined rail.
4. The 22 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 38: **V_{CCINT_VCU} Decoupling Capacitor Recommendations for XQ Zynq UltraScale+ MPSoC EV Devices**

	V_{CCINT_VCU}			
	47 µF	22 µF	2.2 µF	0.47 µF
XQZU5EV-SFRC784	2	3	4	5
XQZU5EV-FFRB900	2	3	4	5
XQZU7EV-FFRB900	2	3	4	5
XQZU7EV-FFRC1156	2	3	4	5

Table 39: **PS Decoupling Capacitor Recommendations for XQ Zynq UltraScale+ Devices**

$V_{CC\_PSINTFP}$		$V_{CC\_PSINTLP}$		V_{CC_PSAUX}		V_{PSPLL}		$V_{PSINTFP\_DDR}$		V_{CCO_PSIOx} (Each)[1]		V_{CCO_PSDDR}		V_{CC_PSBATT}	
22 µF	10 µF	22 µF	10 µF	10 µF	2.2 µF	22 µF	10 µF	22 µF	10 µF	22 µF	10 µF	22 µF	2.2 µF	22 µF	2.2 µF
1	2	1	1	1	1	1	1	2	2	1	1	1	1	1	1

Notes:

1. Can combine 22 µF at one per every four shared VCCO_PSIO banks.
2. For $V_{PS\_MGTRAVCC}$ and $V_{PS\_MGTRAVTT}$, use one 22 µF each.

Table 40: **$V_{CCSDFEC}$ Decoupling Capacitor Recommendations for XQ Zynq UltraScale+ RFSoC Devices**

	$V_{CCSDFEC}$			
	330 µF	47 µF	22 µF	2.2 µF
XQZU28DR	1	1	3	7
XQZU48DR	1	1	3	7

Table 41: **V_{CCINT_AMS} and ADC Decoupling Capacitor Recommendations for XQ Zynq UltraScale+ RFSoC Devices**

RFSoC	V_{CCINT_AMS}			V_{ADC_AVCC}				$V_{ADC\_AVCCAUX}$	
	47 µF	10 µF	2.2 µF	330 µF	47 µF	22 µF	2.2 µF	47 µF	22 µF
XQZU28DR-FFRE1156	2	4	6	1	1	3	4	1	1
XQZU28DR-FFRG1517	2	4	6	1	1	3	4	1	1
XQZU29DR-FFRF1760	3	7	10	1	1	4	8	1	1
XQZU48DR-FFRE1156	1	3	4	1	1	3	5	1	1
XQZU48DR-FSRG1517	2	4	6	1	1	3	5	1	1
XQZU49DR-FSRF1760	2	4	6	1	1	4	8	1	1
XQZU65DR-FFRE1156	1	2	2	1	1	3	5	1	1
XQZU67DR-FFRE1156	1	3	4	1	1	4	7	1	1

Table 42: **DAC Decoupling Capacitor Recommendations for XQ Zynq UltraScale+ RFSoC Devices**

RFSoC	V_{DAC_AVCC}				$V_{DAC\_AVCCAUX}$		V_{DAC_AVTT}		
	330 µF	47 µF	22 µF	2.2 µF	47 µF	22 µF	47 µF	22 µF	2.2 µF
XQZU28DR-FFRE1156	1	1	3	5	1	1	1	1	1
XQZU28DR-FFRG1517	1	1	3	5	1	1	1	1	1
XQZU29DR-FFRF1760	1	1	4	8	1	1	1	1	1
XQZU48DR-FFRE1156	1	1	3	6	1	1	1	1	1
XQZU48DR-FSRG1517	1	1	3	6	1	1	1	1	1

Table 42: **DAC Decoupling Capacitor Recommendations for XQ Zynq UltraScale+ RFSoC Devices** *(cont'd)*

RFSoC	V_{DAC_AVCC}				$V_{DAC\_AVCCAUX}$		V_{DAC_AVTT}		
	330 µF	47 µF	22 µF	2.2 µF	47 µF	22 µF	47 µF	22 µF	2.2 µF
XQZU49DR-FSRF1760	1	2	5	10	1	1	1	1	1
XQZU65DR-FFRE1156	1	1	2	5	1	1	1	1	1
XQZU67DR-FFRE1156	1	1	3	6	1	1	1	1	1

Estimating Power

The Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) does not report separate power estimates for V_{CCAUX_HPIO} and V_{CCAUX_HDIO}. The power consumption for a device operating in LVAUX mode with V_{CCAUX_HPIO} at 1.2V is the same as using the device in standard operating mode with V_{CCAUX_IO} at 1.8V. However, the current drawn from the device in LVAUX mode is higher. This section describes how to estimate the power and current consumption when a device is configured using LVAUX mode. The methodology involves obtaining separate power estimates for HP I/O banks and HD I/O banks using XPE. From these estimates. you can calculate the current needed to operate the device and use this value to choose your V_{CCAUX_HPIO} and V_{CCAUX_HDIO} power supplies.

Methodology

1. Fill in XPE as if you are designing in standard operating mode: Using the *Xilinx Power Estimator User Guide* (UG440), configure XPE. You should populate as many of the settings and sheets as possible to get an accurate estimate.

   IMPORTANT! *You cannot change the V_{CCAUX_IO} power supply to 1.2V in the summary sheet. Leave the cell as 1.8V.*

   When populating the I/O sheet, you cannot select the LVAUX I/O standards. Instead, use the counterpart to the LVAUX I/O standard you intended to use as shown in Table 19: LVAUX and Non-LVAUX I/O Standards.

2. Estimate the power consumption of HP I/O (only): Configure XPE with values for HP I/O banks only.
   - Keep the number of *HP* I/O input pins, output pins, and bidirectional pins to their current values.
   - Set the number of *HD* I/O input pins, output pins, and bidirectional pins to zero.
   - Record the total power drawn for V_{CCAUX_IO}. This is the total static and dynamic power drawn from the HP I/O banks.
   - Divide this number by the voltage of the V_{CCAUX_HPIO} power supply (nominally 1.2V) to get the current (A) estimate for the HP I/O banks.

3. Estimate the power consumption of HD I/O (only): Configure XPE with values for HD I/O banks only.
   - Set the number of *HD* I/O input pins, output pins, and bidirectional pins back to their correct values.
   - Set the number of *HP* I/O input pins, output pins, and bidirectional pins to zero
   - Record the total power drawn for V_{CCAUX_IO}. This is the total static and dynamic power drawn from the HD I/O banks.
   - Divide this number by the voltage of the V_{CCAUX_HDIO} power supply (nominally 1.8V) to get the current (A) estimate for the HD I/O banks.

Chapter 4

Vivado Tools Requirements and Design Guidelines

Vivado Design Suite Versions

The LVAUX I/O standards and DDR4 SDRAM (MIG) in the IP catalog are fully supported by Vivado Design Suite 2019.2 or later for XQ ruggedized UltraScale+ devices only.

I/O Buffer Information Specification Models

I/O buffer information specification (IBIS) models for the LVAUX I/O standards are not supported. For simulating LVAUX I/O behavior, you can use the IBIS models for the non-LVAUX I/O standards listed in the Table 19: LVAUX and Non-LVAUX I/O Standards.

DDR4 SDRAM Memory Interface Generator

Only the DDR4 SDRAM memory interface is supported with the LVAUX I/O standards. The SFRA484 package does not support PL memory interfaces. The following steps are used to enable LVAUX for DDR4 on the PL side using the Vivado Design Suite:

1. Using the *Design Flow Steps* described in *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150), generate the IP for DDR4 SDRAM (MIG).
2. In the *Generate Output Products* dialog, do not select **Generate**, instead select **Skip**. By clicking **Generate**, RTL is generated and the Tcl command in the next step is ignored.
3. In the Tcl console, run the following command:

```
set_property -dict [list CONFIG.C0.DDR4_Enable_LVAUX {true}] [get_ips <ddr4_ip_name>]
```

4. Right-click the DDR4 IP file in the `Design Sources` folder and select **Generate Output Products**. Click **Generate** to create the output files. The I/O standard changes made using the Tcl command are applied in the generated files.
5. Confirm that the DDR4 ports are set to the LVAUX I/O standards in the following file.

```
<project_name>.srcs\sources_1\ip\<ddr4_ip_name>\par\<ddr4_ip_name>.xdc
```

I/O Interface Attributes and Constraints

See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for a full list of attributes and constraints that can be applied to the I/O standards. To operate in LVAUX mode, additional considerations need to be taken into account if using the following attributes and constraints:

- **IOSTANDARD Attribute:** DC I/O Levels contains the specifications of the LVAUX IOSTANDARDs.
- **IBUF_LOW_PWR Attribute:** IBUF_LOW_PWR must be explicitly set to FALSE to operate in LVAUX mode.

```
set_property IBUF_LOW_PWR FALSE [get_ports port_name]
```

- **Output Drive Strength Attribute:** LVCMOS12_LVAUX is only allowed to have a drive strength of 8 mA.

Memory Interface Guidelines

The LVAUX I/O standards only support DDR4 component memory. The following tables provide the maximum data rates for the DDR4 memory standard using the XQ ruggedized UltraScale+ device memory PHY.

Table 43: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	Packages	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2I	-2LE	-1I/-1M	-1LI	-2LE	-1LI	
XQ Ruggedized Kintex UltraScale+ FPGAs									
DDR4	FFRB676 FFRA1156 FFRE1517	Single rank component	2133	N/A	1866	1866	N/A	1600	Mb/s
	SFRB784	Single rank component	1866	N/A	1600	1600	N/A	1333	Mb/s
XQ Ruggedized Virtex UltraScale+ FPGAs									
DDR4	FFRC1517 FLRA2104 FLRB2104 FLRC2104	Single rank component	2133	2133	1866	N/A	1866	N/A	Mb/s
XQ Ruggedized Zynq UltraScale+ MPSoCs[1]									
DDR4	FFRB900 FFRC1156 FFRC900 FFRB1156 FFRC1760 FFRB1517	Single rank component	2133	N/A	1866	1866	N/A	1600	Mb/s
	SFRC784	Single rank component	1866	N/A	1600	1600	N/A	1333	Mb/s
XQ Ruggedized Zynq UltraScale+ RFSoCs									
DDR4	FFRD1156 FFRE1156 FFRG1517 FFRF1760	Single rank component	2133	N/A	1866	1866	N/A	1600	Mb/s

Notes:

1. The SFRA484 package does not support PL memory interfaces.

Appendix A

Additional Resources and Legal Notices

Finding Additional Documentation

Technical Information Portal

The AMD Technical Information Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Technical Information Portal, go to https://docs.amd.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help → Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

***Note*:** For more information on DocNav, refer to the *Documentation Navigator User Guide* (UG968).

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the Design Hubs web page.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

These documents provide supplemental material useful with this guide:

1. UltraScale+ device data sheets:
   - *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895)
   - *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922)
   - *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
   - *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
   - *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
2. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
3. *UltraScale Architecture PCB Design User Guide* (UG583)
4. UltraScale+ device packaging and pinout user guides:
   - *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575)
   - *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075)
5. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
6. Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power)
7. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
8. *UltraScale Architecture GTY Transceivers User Guide* (UG578)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
05/03/2024 Version 1.1	
Chapter 1: Introduction	Added reference to *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895) for available XQ UltraScale+ devices and ruggedized packages.

Section	Revision Summary
UltraScale+ Device SEL	• Corrected result of FIT calculation at 125°C T_j. • Added Ruggedized Packages column to Table 2. • Added XQZU48DR, XQZU49DR, XQZU65DR, and XQZU67DR to Table 2.
SEL Impact, Power Guidelines, Decoupling Capacitors	Added Zynq UltraScale+ RFSoC XQZU48DR, XQZU49DR, XQZU65DR, and XQZU67DR devices throughout.
LVAUX Mode Overview, Special Considerations for XQ Ruggedized FPGAs	Added clarification that XQ Virtex UltraScale+ devices do not have HD I/O pins and their packages use the VCCAUX_IO name for pins that supply the auxiliary power to the HP I/O. Whereas, XQ Kintex UltraScale+ and Zynq UltraScale+ ruggedized packages use the VCCAUX_HPIO pin name for pins that supply the auxiliary power only to the HP I/O.
SelectIO Resources, Summary of LVAUX Mode versus Standard Operating Mode, LVAUX Mode Checklists, I/O Guidelines, Rules for Combining I/O Standards in the Same Bank	Added notes throughout that system monitor external analog inputs are not supported in LVAUX mode HP I/O banks.
DC I/O Levels, IOB High Performance Switching Characteristics, LVDS12_LVAUX	Added clarifications that LVDS12_LVAUX is compatible with some LVDS standards.
PCB Design Guidelines	Revised decoupling capacitor recommendations to maintain alignment to revision in Decoupling for Defense Grade XQ Devices in *UltraScale Architecture PCB Design User Guide* (UG583). The capacitor values and part numbers have been updated taking into account the latest product offerings from various vendors because some of the part numbers from the previous versions of this user guide have reached end of life. The new guidelines also incorporate capacitors with a wider temperature range (X7R) compared to the previous part numbers. The prior capacitor tables and specifications are still valid for existing designs, but for new designs, the current tables and specifications are recommended.
12/16/2019 Version 1.0	
Initial release.	N/A

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