Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits

WP286 (v2.1) April 12, 2023

Abstract

Hardness to atmospheric neutrons continues to improve as process architectures as small as 7 nm have come online. Longer beam test times have therefore been implemented.

The September 2005 issue of *IEEE Transactions on Device and Materials Reliability* featured an article entitled *The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs* [Ref 1]. The article described real-time experiments that evaluated large AMD FPGAs for their sensitivity to radiation-induced single event upsets (SEUs).

This white paper clarifies some open issues from the original AMD Rosetta experiments conducted in 2005.

The devices under test represent several CMOS technologies, from 150 nm, current at the time of this white paper's original publication (v1.0), to 7 nm, current at the time of publication of this revision (v2.1). Detailed experimental results derived from simulation, beam testing, and atmospheric testing are presented.

AMD Adaptive Computing is creating an environment where employees, customers, and partners feel welcome and included. To that end, we're removing non-inclusive language from our products and related collateral. We've launched an internal initiative to remove language that could exclude people or reinforce historical biases, including terms embedded in our software and IPs. You may still find examples of non-inclusive language in our older products as we work to make these changes and align with evolving industry standards. Follow this link for more information.

Introduction

The Stone of Rosette by Ulrich Schade and Richard Wäsch [Ref 2] defines Rosetta as follows:

Rosetta refers to the crucial breakthrough in the research regarding Egyptian hieroglyphs. It especially represents the "translation" of "silent" symbols into a living language, which is necessary in order to make the whole content of information of these symbols accessible."

Just as the Rosetta Stone enabled researchers to decode the unsolvable and mysterious Egyptian hieroglyphs by comparing them to the same text written in a known language, the AMD Rosetta experiments link two prior known and well-documented techniques of estimating atmospheric neutron single event upsets (SEUs) with the real effects of atmospheric neutrons on integrated circuits. The known techniques are accelerated testing in a neutron or proton beam and software simulation of the circuit to determine the critical charge a particular node or latch can handle before it changes state. These AMD experiments determine the actual upset rate of AMD FPGAs due to an atmospheric neutron cascade, which resulted from a cosmic ray. With a good understanding of the real effect(s) that these atmospheric neutrons have on today's integrated circuits, AMD can validate the design and technology choices being used to mitigate these effects.

Predicting atmospheric neutron flux is not an exact science. In the JEDEC89A standard, there is a methodology that uses models and magnetic latitude data to predict the flux at any given location on the earth. The 2005 Rosetta results clearly did not agree with the original JEDEC89 standard, and the committee worked in collaboration with AMD to resolve this issue. Three corrections were made to the JEDEC89A standard:

- Realization that the proton flux is not insubstantial (it is approximately an additional 7% in San Jose and as much as an additional 32% at Mauna Kea).
- The attenuation by the building must be more accurately calculated (28% of the flux is lost to the ground floor of a typical Silicon Valley, two-story, tilt-up, concrete structure).
- A more automated model can be developed to aid investigators (a new prototype web-based tool): http://www.seutest.com/cgi-bin/FluxCalculator.cgi.

The JEDEC89A revision also proposes a new atmospheric spectral model, based on work done by Goldhagen, et al. [Ref 3].

Thermal neutrons were not considered at the time to have sufficient energy to upset devices. Since the 28 nm technology node, thermal neutrons are now considered, because they do contribute to the overall upset rate.

Alpha particles (contamination) to fabrication and packaging have led to ultra-low alpha manufacturing processes utilized by AMD, and verified by below-ground (shielded) testing.

Experiments

Each Rosetta experiment consisted of multiple sets of 100 of the largest available AMD FPGAs using differing technologies, located at different altitudes. All tested components were fabricated by AMD foundry partners, using their planar or FinFET technologies.

The following table lists the locations of the experiments. Table 2 and Table 3 list the device type, technology, and quantity.

Table 1: **Locations of AMD Rosetta Experiments**

Location	Altitude (Feet)	Adjusted Altitude Factor[1]
Lead, SD	–5800[2]	0.00
Rustrel, France	–1600[2]	0.00
San Jose, CA	257	0.75
Marseilles, France	359	1.08
Longmont, CO	4958	4.11
Albuquerque, NM	5145	3.34
Pic du Bure, France	8196	6.00
Pic du Midi, France	9298	8.62
Leadville, CO	10200	12.22
Echo Lake, CO	10600	13.02
Aiguille du Midi, France	11289	12.45
White Mountain, CA	12442	19.48
Mauna Kea, HI	13000	11.35

Notes:

1. Adjustments have been made for the influence of minimum solar sunspots on cosmic ray flux.
2. Underground facilities.

Table 2: **Devices Previously Tested (WP286 v1.x)**

Device Family	Device Number	Technology	Quantity
Kintex™ 7 FPGAs	XC7K325T	28 nm	300
Virtex™ 7 FPGAs	XC6VLX240T	40 nm	300
Spartan™ 6 FPGAs	XC6SLX150	45 nm	200
Virtex 4 FPGAs	XC4VLX25	90 nm	400
Virtex 4 FPGAs	XC4VLX60	90 nm	300
Spartan 3 FPGAs	XC3S1500	90 nm	200
Virtex-II FPGAs	XC2V6000	150 nm	300
Virtex-II Pro FPGAs	XC2VP50	130 nm	600

Table 3: **Devices Presently Under Test (WP286 v2.x)**

Device Family	Device Number	Technology	Quantity
Kintex UltraScale™ FPGAs	XCKU040	20 nm	400
Kintex UltraScale+™ FPGAs	XCKU9P	16 nm	400
Versal™ devices	VC1902	7 nm	300

Over the years, the Rosetta program has changed to include prediction of error rates using TCAD modeling, fabrication and beam testing of test devices, beam testing of production devices, and testing using the atmospheric placement of arrays, as well as underground arrays.

In the IC design of the AMD FPGAs, the individual memory cells (implemented as static latches) used for configuration, look-up tables, and block RAM were all simulated for their sensitivity to single event upsets.

To detect alpha contamination in packaging and assembly, the experimental groups were rotated through the three altitudes in addition to using the underground facility. Any evidence of a constant upset rate due to alpha particles would be observed as a non-altitude, non-latitude dependent factor in the resulting upsets, or measured directly underground.

Atmospheric Test Results

All atmospheric and alpha information is present in the *Device Reliability Report* (UG116), which AMD updates twice per year. The report summarizes the atmospheric and beam test results for all FPGA device technologies. The error rate is stated either in failures in time (FIT) per billion hours or in mean time between events in hours, days, or years. A functional failure of the user data due to the single event upset rate then becomes mean time between functional failure in hours, days, or years. *Estimation of Single Event Upset Probability Impact of FPGA Designs* [Ref 4] describes the relationship between the mean time between failure (MTBF) configuration bit and mean time between functional failure, which is based in estimating the Device Vulnerability Factor (DVF). Not every upset results in a functional failure because upsets can be masked in either time or space by a user's design. The DVF factor has been shown to be commonly from 2%, to no more than 10%, in actual device beam testing. A reasonable DVF estimate when the design is not known is 5%.

Since on average, it takes from 10 to 50 upsets to actually cause a functional failure, determining the field failure rate of any design needs to be appropriately derated. The recommended worst-case estimate is to use a factor of ten (10) as the derating factor.

An essential bits feature of the AMD bitstream generation tools provides a design-specific estimate of the derating for any design. In addition to the *Device Reliability Report*, AMD also provides a pre-design failures-in-time (FIT) estimator that helps customers determine if SEU mitigation is needed, given their design specifications.

Q_{CRIT} Simulation

The AMD IC design group uses models and methods from AMD fabrication partners to estimate the potential sensitivity of the memory cells to upsets. These models and methods have been used in their production of other standard products. Their prediction of Q_{CRIT} to atmospheric upsets is used to compare with AMD observations in the Rosetta experiment.

AMD then models candidate layouts because they differ in some cases from the foundry layout. After that, AMD fabricates test devices so that beam testing can be done to confirm predictions prior to making a selection of a candidate cell for use in an AMD product.

LANSCE Results

Testing is performed at LANSCE on a regular basis. See the *Device Reliability Report* (UG116).

Conclusion

As the hardness to atmospheric neutrons improves, fewer upsets in the beam testing also occur, which affect the accuracy of the results, requiring longer beam exposures or resulting in higher statistical uncertainty.

It is not possible to make a statement about foundry, process, voltage, or temperature effects without side-by-side experiments in the same beam, at the same time, with a few thousand upsets on each. All data in the *Device Reliability Report* (UG116) meets these criteria.

For more information, go to: Reliability

References

These documents provide supplemental material useful with this guide:

1. Lesea, Austin, Saar Drimer, Joseph Fabula, Carl Carmichael, and Peter Alfke. *The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs*. IEEE Transactions on Device and Materials Reliability, Volume 5, Number 3, September 2005.
2. Schade, Ulrich and Richard Wäsch, *The Stone of Rosette*. October 23, 1996.
3. Goldhagen, Paul, J.M. Clem, and J.W. Wilson, *Recent Results from Measurements of the Energy Spectrum of Cosmic-Ray Induced Neutrons Aboard an ER-2 Airplane and on the Ground*. Preprint: Advances in Space Research 32 (1) pp. 35-40 (2003), Proceedings of the 34th COSPAR Scientific Assembly, Houston, TX, October 10-19, 2002.
4. Sundararajan, Prasanna, Scott McMillan, Brandon Blodget, Carl Carmichael, and Cameron Patterson. *Estimation of Single Event Upset Probability Impact of FPGA Designs*. MAPLD 2003.

Related Reading

1. Roche, Philippe and Gilles Gasiot. *Impacts of Front-End and Middle-End Process Modifications on Terrestrial Soft Error Rate*. IEEE Transactions on Device and Materials Reliability, Volume 5, Number 3, September 2005.
2. Castellani, Karine. *3-D Modeling of Bulk and Multi-gate Transistors and SRAM* (summary of research), Laboratoire Matériaux et Microélectronique de Provence (L2MP), UMR/CNRS.
3. Howe, Christina L., Robert A. Weller, Robert A. Reed, Marcus H. Mendenhall, Ronald D. Schrimpf, Kevin M. Warren, Dennis R. Ball, Lloyd W. Massengill, Kenneth A. LaBel, Jim W. Howard, Jr., and Nadim F. Haddad. *Role of Heavy-Ion Nuclear Reactions in Determining On-Orbit Single Event Error Rates*. IEEE Transactions on Nuclear Science, Volume 52, Issue 6, December 2005.

Acknowledgments

AMD extends appreciation to these facilities for their assistance with this document:

- **The Los Alamos Neutron Science Center at the Los Alamos National Laboratory:** This facility is funded by the U.S. Department of Energy under Contract W-7405-ENG-36.

- **The California Institute of Technology Submillimeter Observatory:** Mauna Kea, Hawaii

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
4/12/2023 Version 2.1	
Experiments	Added Leadville, CO to Table 1: Locations of AMD Rosetta Experiments.
	Updated devices in Table 2: Devices Previously Tested (WP286 v1.x) and Table 3: Devices Presently Under Test (WP286 v2.x).
3/22/2016 Version 2.0	
General	Updated document to reflect additional technology nodes to 16 nm and clarify historical versus ongoing experiments.
10/13/2011 Version 1.1	
General	Updated document to reflect 40 nm technology node and added Virtex-6 and Spartan-6 FPGA data. Updated Introduction, Table 2, Experiments, Atmospheric Test Results, QCRIT Simulation, Accelerator Test Facilities, Conclusion, Acknowledgments, and References sections.
5/22/2009 Version 1.0.1	
General	Changed footnote 1 on page 3. Was: FIT/Mb = failures per million hours per Megabit. Is: FIT/Mb = failures per billion hours per Megabit.
3/10/2008 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions, and typographical errors. The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. Any computer system has risks of security vulnerabilities that cannot be completely prevented or mitigated. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes. THIS INFORMATION IS PROVIDED "AS IS." AMD MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE CONTENTS HEREOF AND ASSUMES NO RESPONSIBILITY FOR ANY INACCURACIES, ERRORS, OR OMISSIONS THAT MAY APPEAR IN THIS INFORMATION. AMD SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL AMD BE LIABLE TO ANY PERSON FOR ANY RELIANCE, DIRECT, INDIRECT, SPECIAL, OR OTHER CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF ANY INFORMATION CONTAINED HEREIN, EVEN IF AMD IS EXPRESSLY ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright

© Copyright 2008–2023 Advanced Micro Devices, Inc. AMD, the AMD Arrow logo, Kintex, Spartan, Versal, Virtex, and combinations thereof are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.