WP446 (v1.0.1) April 18, 2014

Comprehensive JESD204B Solution Accelerates and Simplifies Development

By: Tom Hill

The JESD204B standard offers key advantages over LVDS, including higher bandwidth, fewer device pins, reduced board area, and lower power. For these reasons, it is expected to be quickly adopted for wireless, medical, SDR, and radar applications that require high bandwidth, a large number of channels, or robust, easy-to-use configurability.

Complete solutions are available from Xilinx and its ecosystem partners that allow users to quickly bring up JESD204B systems using standard Xilinx development boards and software tools. The Vivado® Interactive Logic Analyzer leverages dedicated silicon hardware in each transceiver to generate 2D Eye Scans and BER results in real time. This 2D Eye Scan logic not only simplifies board debug but enables constant BER calculations to monitor the integrity of the link once deployed to the field. It is a unique capability that enables pre-emptive link degradation and failure capability to any system using Xilinx devices.

An Overview of JESD204B

JESD204B is a rapidly emerging standard for interfacing analog data converters to FPGAs using high-speed serial transceivers. This standard is expected to replace the use of LVDS interfaces in many of today's wireless, medical, and aerospace and defense applications. JESD204B, a multi-gigabit serial data link between the data converter and FPGA, is the second revision of the original JESD204 specification first ratified by IEEE in 2006. The original version supported a single lane between 312.5 Mb/s to 3.125 Gb/s.

Two years later, the JESD204A standard was introduced to add the ability to support multiple aligned serial lanes with multiple converters, while leaving the data rate unchanged at 3.125 Gb/s.

Both the original JESD204 and the revised JESD204A standards offered higher performance than existing LVDS interfaces, but they were not widely adopted by analog vendors, FPGA vendors, or customers because they did not provide deterministic latency. This made it difficult to maintain synchronization between the analog and digital representations of a signal. To address this limitation, a second revision, JESD204B, was introduced in 2011. JESD204B (see Figure 1) provides deterministic latency and increases the highest supported data rate from 3.125 Gb/s to 12.5 Gb/s.

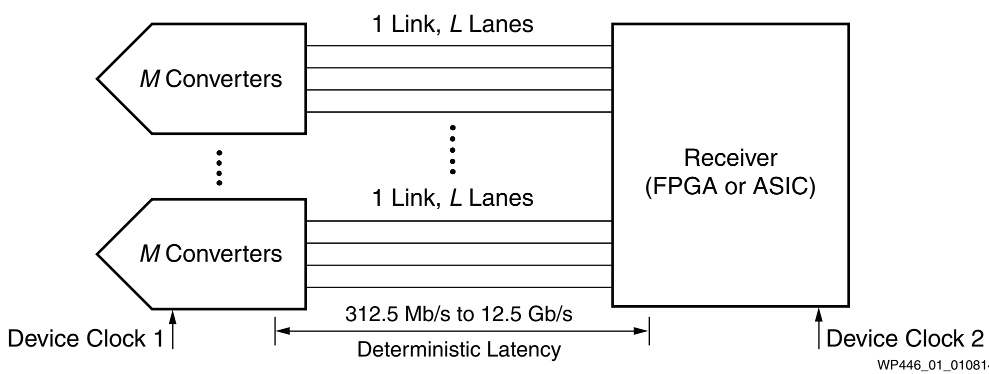

Figure 1: **JESD204B Standard**

The JESD204B protocol stack consists of seven functional blocks in the transmit path and seven functional blocks in the receive path, as shown in Figure 2.

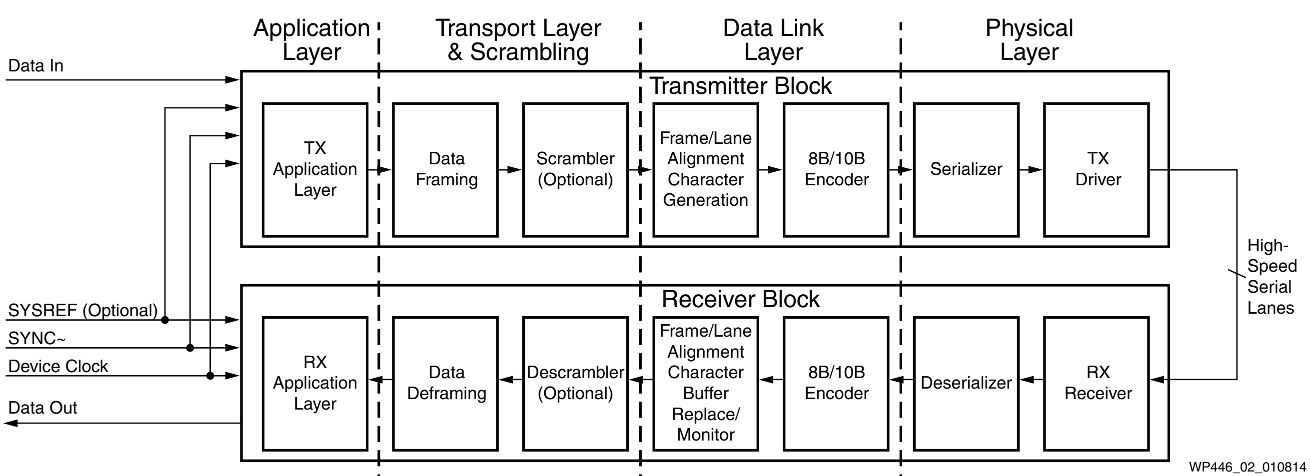

Figure 2: **JESD204B Protocol Stack**

The JESD204B Advantage

JESD204B is poised to take over as the technology of choice for interfacing high-speed data converters to FPGAs in much the same way as the LVDS interface began overtaking its predecessor, CMOS. LVDS offers the flexibility to support very high bandwidth interfaces, but at the cost of high FPGA pin usage. The JESD204B interface standard supports the high bandwidth necessary to keep pace with high-performance, high-speed, multi-channel applications, while greatly reducing the number of digital I/Os needed, thus easing board layout congestion. Very high speed (>1 GSPS) ADCs that would have previously required a complex interface design using large numbers of FPGA I/Os can now be implemented with just a few pins. The total bandwidth of the JESD204B interface can also be separated into multiple channels based on the requirements of the application — again, without requiring additional pins.

Table 1 compares the pins required by LVDS and JESD204B interfaces to a 14-bit ADC across a variety of channel counts:

Table 1: **I/O Pin Count for LVDS vs. JESD204B**

Number of Channels	Resolution	LVDS Pin Count	JESD204B Pin Count
1	14	14	4
2	14	28	4
4	14	56	6
8	14	112	6

Because of these obvious implementation benefits, the following is just a sampling of the many use cases that are rapidly migrating to JESD204B:

- **Wireless Infrastructure:** OFDM-based technologies, such as the evolving LTE family of standards, must perform highly complex signal processing in the FPGA. JESD204B interfacing supports the demand for high-bandwidth throughput with less power and fewer pins than LVDS.
- **Software Defined Radios (SDRs):** Cutting-edge SDR designs utilize advanced modulation schemes that are on-the-fly reconfigurable. The high flexibility of the JESD204B standard enables dynamic changes in the number of channels being used *and* their bandwidths — all with a lower power requirement than past solutions. This is especially important in battery-powered radio applications.
- **Medical Imaging System:** Medical imaging systems, including ultrasound, computational tomography (CT), magnetic resonance imaging (MRI), and others require high numbers of ADC channels (often 64 or more) that must be interfaced to the FPGA. JESD204B provides a more efficient interface technology that requires far fewer pins, resulting in simpler board designs and smaller FPGA packages.
- **Radar:** Increasingly sophisticated pulse-radar receivers are pushing signal bandwidths beyond 1 GSPS in multi-channel configurations. JESD204B is required to support this high bandwidth between the data converters and FPGA.

With data synchronization now addressed, JESD204B is gaining support from high-speed analog vendors, who are quickly introducing new data converter families with JESD204B interfaces. This next generation of high-speed ADCs and DACs can be interfaced to a wide variety of Xilinx® UltraScale™ Kintex, UltraScale Virtex, Artix®-7, Kintex®-7, Virtex®-7, Virtex-6, and Spartan®-6 FPGAs, as well as

Zynq®-7000 All Programmable SoCs (AP SoCs)— all of which are available with on-chip serial transceivers to take full advantage of the JESD204B serial bandwidth.

The JESD204B Design Challenge

JESD204B offers better interface efficiency than LVDS due to the use of high-speed serial transceivers. For many designers, this migration from LVDS to JESD204B can present new, operationally subtle design challenges.

High-Speed Serial Challenges

There are challenges with using high-speed serial transceivers. The high transmission frequencies used by these transceivers demand that designers pay close attention to signal integrity issues to avoid unacceptable error rates. This often involves the use of analog simulations and more complex bypassing schemes. Designs also need to consider the impedance of the circuit board traces and vias, purpose-designed high-speed connectors, and various types of interconnecting cables.

Here is another challenge. The high-speed serial transceivers in JESD204B implementations operate at speeds of 3 Gb/s, 5 Gb/s, or even in excess of 10 Gb/s, leveraging multiple clock phases (0°, 90°, 180°, and 270°) to direct the data into four sets of flip-flops during serialize and deserialize operations. During serialization, the efficient communication protocols used in such high-speed schemes can create “gaps” in the encoded analog signal stream caused by long runs of consecutive zeros or ones. These can negatively impact the receiver's ability to stay in sync and continue to decode correctly. Breaking up such transition-free gaps in the received signal is often accomplished by embedding an appropriate polynomial in the scrambler block near the receiver’s front end before decoding is attempted.

Serial Signal Distortion Challenges

An eye *waveform* (Figure 3, left) expresses the time-domain accuracy of the serial data stream. It shows how bit jitter is affecting the performance of a serial transceiver. An eye *mask* (Figure 3, right) is a definition provided for JESD204B that specifies how open an eye pattern needs to be for the receiver to operate with an adequately low bit-error ratio (BER). In an ideal data stream, bit level transitions are instantaneous, with no overshoot, undershoot, or ringing. The inherent limitations of the transmission conduit (which has its own characteristic impedance and loss profile at various frequencies) makes achieving an ideal eye pattern impossible in a real-world system.

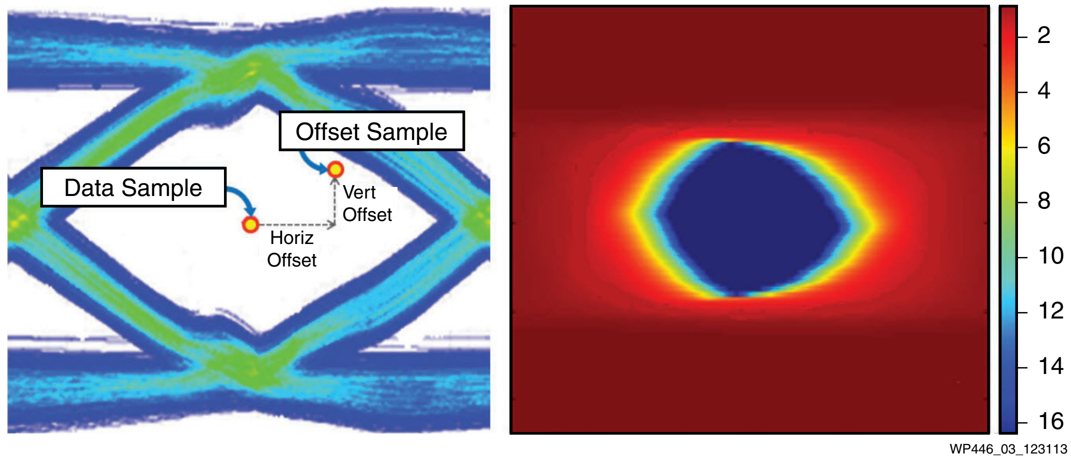

Figure 3: **Serial Transceiver Eye Diagrams**

Successfully designing a JESD204B interface requires not only the fundamental ability to design successful implementations of high-speed serial transceivers, but also an intimate knowledge of the JESD204B standard and its many options.

The Xilinx JESD204B Solution

Xilinx offers a complete working solution that simplifies the adoption of JESD204B, including best-in-class serial transceivers, IP, design tools, reference designs, and ecosystem partners.

- **GTH Transceiver Architecture:** Reducing the BER in serial transceiver transmissions directly correlates to the peak bandwidth that can be achieved through the serial link. Xilinx FPGAs offer industry-leading jitter performance, achieved through a unique capability called Adaptive Receiver Equalization. This improves the performance of the decision feedback equalizer (DFE) block, significantly reducing BER. See Figure 4.

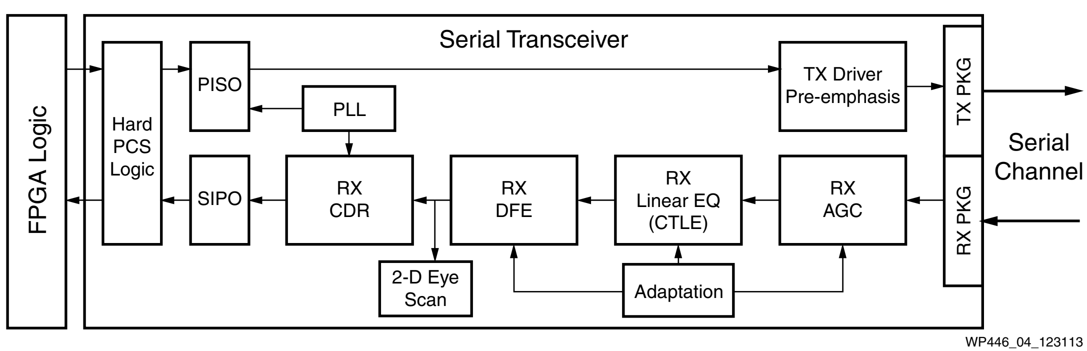

Figure 4: **Xilinx Serial Transceiver Block Diagram**

All Xilinx receiver equalization techniques — e.g., automatic gain control (AGC), continuous time linear equalization (CTLE), and DFE — are available in three modes: manual, one-time calibration, and continuous adaptation. (Continuous adaptation can also be used to adjust for voltage and temperature changes that impact transceiver performance.)

- **Xilinx JESD204B IP Core:** Xilinx offers the industry's first fully JESD204B-compliant IP core for programmable logic. This core (see Figure 5) supports the full JESD204B bandwidth specification of 12.5 Gb/s over one to eight lanes. It can be configured as both a transmitter for interfacing to a DAC and as a receiver for interfacing to an ADC. The core also includes support for scrambling and initial lane alignment.

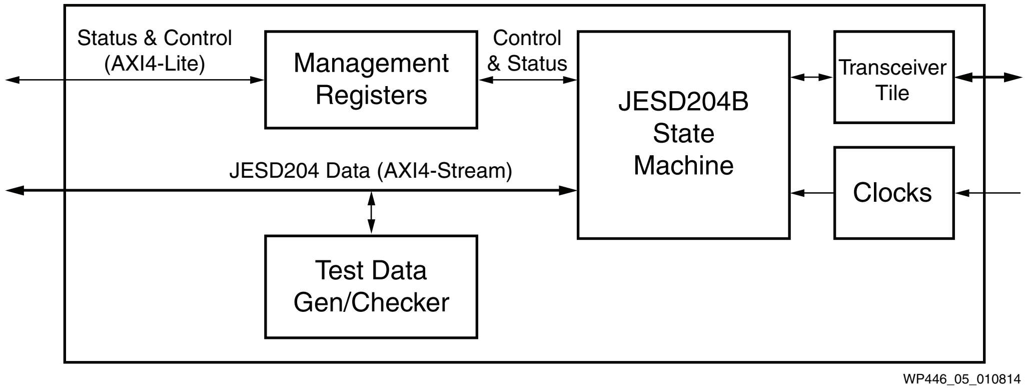

Figure 5: **Xilinx JESD204B IP Core Block Diagram**

- **Vivado Serial I/O Analyzer:** The Vivado serial I/O analyzer provides a fast, easy, interactive setup-and-debug environment for serial I/O channels in high-speed FPGA designs. The serial I/O analyzer allows the user to take BER measurements on multiple channels and adjust high-speed serial transceiver parameters in real time while the serial I/O channels interact with the rest of the system. The Vivado Serial I/O Analyzer can measure BER on multiple channels simultaneously.

  In addition, a new RX Margin Analysis tool takes advantage of the eye scan feature in 7 series and UltraScale FPGA transceivers to provide a full 2-D scan of all horizontal and vertical offset sampling points within the "eye" (see Figure 6). Also supported is a 1D bathtub curve, as well as scans of all horizontal sampling points through the 0 vertical-row offset.

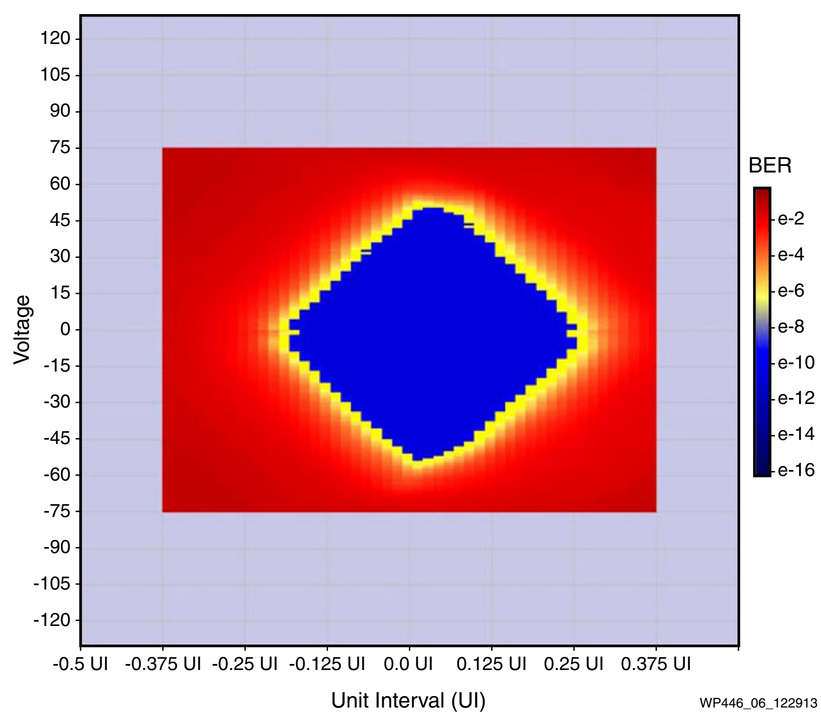

Figure 6: **Vivado Serial I/O Analyzer Eye Scan Diagram**

Xilinx also provides an IBERT IP core. IBERT includes pattern generators and checkers implemented using FPGA logic that provide access to the ports and the dynamic reconfiguration port attributes of the transceivers.

- **FMC Ecosystem for High-Speed Analog:** The FPGA Mezzanine Card (FMC) standard has proven to be highly popular with over 100 total FMC cards now available from a variety of partners. Over 30 of these FMCs specifically support high-speed data converters. The FMC provides a way for customers to quickly configure their standard Xilinx development boards with real-world analog interfaces; Xilinx partners have been providing many easy-to-use (and to re-use) reference designs that save customers weeks or even months of development time. Building on this success are the first high-speed analog FMC cards supporting JESD204B from industry-leading analog providers such as Analog Devices, IDT, 4DSP, NXP, and others.
- **JESD204B Reference Designs:** Complete JESD204B reference designs are provided for Xilinx development boards by a variety of third-party analog vendors, such as Analog Devices, Texas Instruments, IDT, and Intersil. Giving users a known, proven design starting point, these designs are available for development boards with devices that provide serial transceivers. This gives designers an immediate, high-confidence solution for rapid prototyping, making the move from LVDS to serial transceivers virtually seamless.

The reference design illustrated in Figure 7 supports the Analog Devices JESD204B Xilinx Transceiver Debug Tool. This tool provides on-chip 2-D statistical eye scan diagrams; verification of system signal integrity is possible without need of external test equipment, giving it tremendous value for use in remote locations.

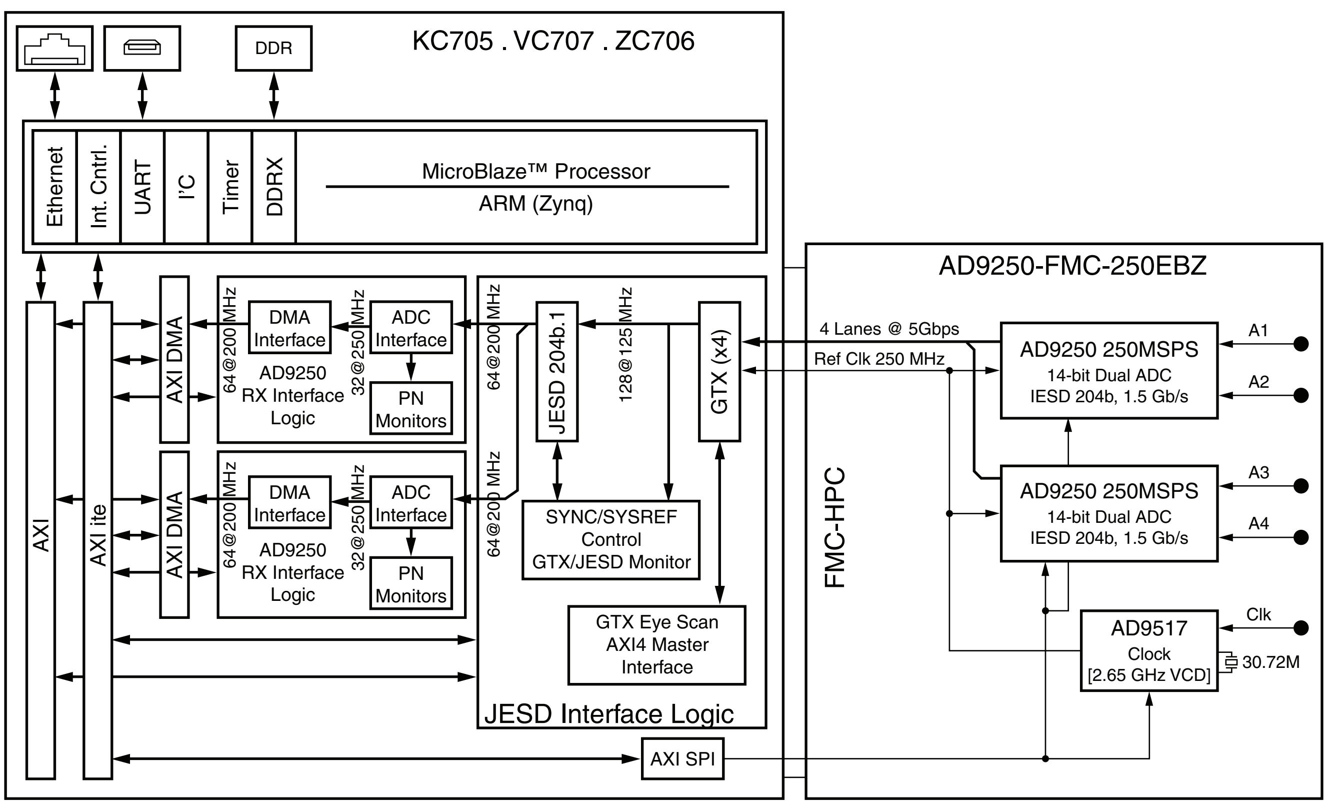

Figure 7: **Analog Devices FMC AD-FMCJESDADC1 ZC706 Reference Design Block Diagram**

Summary

JESD204B is a rapidly emerging standard for interfacing high-speed analog data converters to FPGAs using high-speed serial transceivers. JESD204B is expected to replace the use of LVDS interfaces in many current and newly developing applications; its full 12.5 Gb/s bandwidth can be separated into up to eight channels using a very small number of pins.

Xilinx simplifies the adoption of JESD204B by offering a complete working solution: best-in-class serial transceivers, IP cores, design tools, reference designs, numerous Xilinx ecosystem partners, and the ground-breaking Vivado Serial I/O Analyzer for fast, easy, interactive setup and debug.

For more information about JESD204B and Xilinx products, go to:

http://www.xilinx.com/JESD204B

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/18/2014	1.0.1	Typographical edits.
04/08/2014	1.0	Initial Xilinx release.

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