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# UltraScale Devices Maximize Design Integrity with Industry-Leading SEU Resilience and Mitigation

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*UltraScale™ architecture provides extraordinary SEU resilience and mitigation through its industry-leading offering of robust soft-error solutions.*

## ABSTRACT

Xilinx introduced the UltraScale architecture, the industry's first ASIC-class fully programmable architecture, to enable ultra-high performance applications beyond the capabilities of prior generations and competing programmable solutions.

- Rapid process technology scaling and architectural innovations allow UltraScale devices to achieve levels of system performance, capacity, and power efficiency that make FPGAs an increasingly compelling alternative to ASICs. As such, UltraScale FPGAs can be expected to be found at the heart of systems that demand high availability, high reliability, and adherence to the strictest functional safety requirements.
- To maximize the integrity of UltraScale architecture-based designs, Kintex® UltraScale and Virtex® UltraScale devices offer industry-leading resilience in the presence of single-event upsets (SEUs) through product innovations that, in many applications, reduce or eliminate the need for additional soft-error mitigation solutions. UltraScale devices exhibit up to 3X lower SEU failure-in-time (FIT) per Mb and 2X faster detection and correction of soft errors than prior-generation Xilinx devices.
- For systems that require the highest availability and reliability, Xilinx complements its UltraScale architecture innovations with analysis tools, IP, design techniques, and verification flows.

Xilinx stands as the industry leader with its offering of the complete package — the most robust, flexible, and comprehensive SEU mitigation solution available.

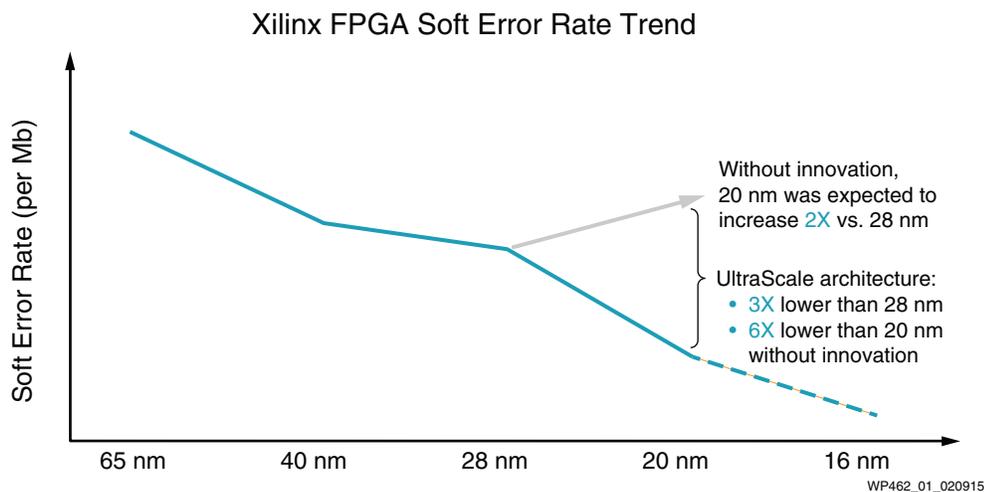
# Introduction

The benefits of advanced process technologies for increasing device capacity, system performance, system integration, and power efficiency cannot be overstated. FPGAs, in particular, are a beneficiary of the ongoing migration to ever smaller process geometries. At the 20 nm node, process scaling, coupled with major architectural innovations, has enabled Xilinx UltraScale FPGAs to deliver unprecedented ASIC-class capabilities in a programmable device. Meanwhile, traditional ASIC solutions continue to struggle with escalating development costs and the risks of committing to a fixed solution in an increasingly dynamic, rapidly changing marketplace.

Along with the many benefits of process scaling, shrinking geometries require increased attention to mitigating various effects that, left unchecked, work to reduce design integrity. Single-event upsets (SEUs) represent one type of effect that requires ongoing diligence and increased levels of innovation to manage in advanced process technologies. SEUs are caused by ionizing radiation sources that send charged particles through transistor junction regions, causing a change in the state of storage elements such as memory cells.

If specific efforts are not made to reduce susceptibility to SEUs, an *increase* in the device's intrinsic soft-error rate as a consequence of process technology scaling is expected. While the transistor cross-section that is sensitive to charge injection is reduced with process scaling, the charge required to change the state of a storage element ( $Q_{CRIT}$ ) is also reduced, and the density of susceptible elements (e.g., configuration memory cells) tends to increase significantly.

Xilinx has multiple generations of experience in design and layout techniques to reverse this trend, with lower SEU FIT/Mb in each successive process node. For instance, as shown in [Figure 1](#), without additional innovation at the 20 nm node, the expectation would be a 2X increase in soft error rate per megabit as compared to the 28 nm node. The UltraScale architecture utilizes over 40 proprietary, patented circuit design and layout techniques to reduce the intrinsic SEU FIT/Mb of the device's configuration memory. As a result, UltraScale devices are targeted to have up to 3X lower SEU FIT/Mb than 28 nm devices, a 6X improvement relative to the expected path for the 20 nm node without such innovation.

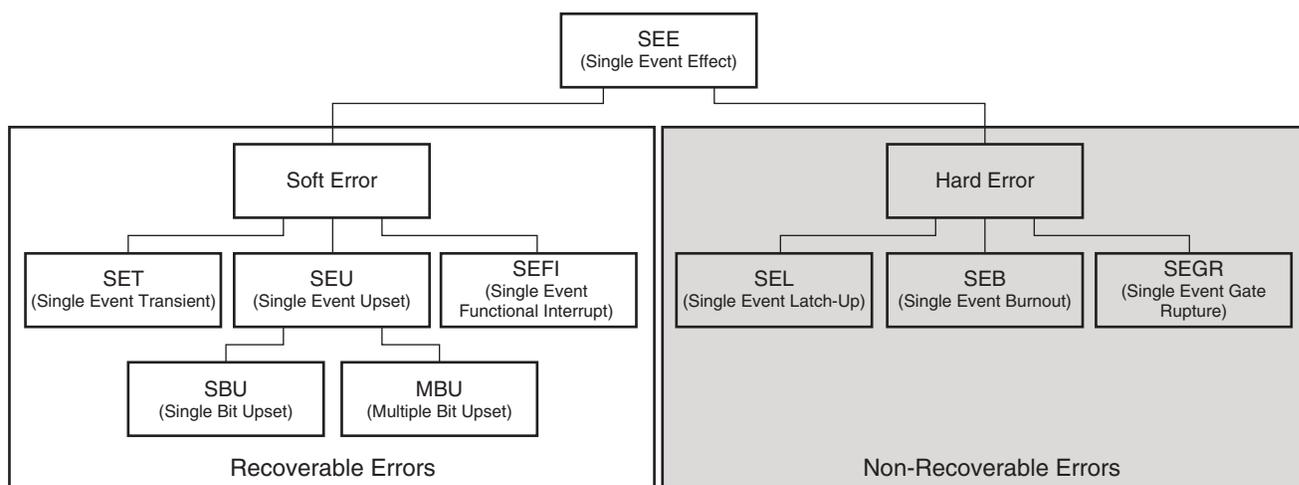


**Figure 1: Xilinx FPGA Soft Error Rates vs. Process Technology Node**

# Single-Event Upsets in FPGAs

As shown in Figure 2, SEUs represent one category of soft error-related events that are part of a broader classification of single-event effects (SEEs). Unlike competing solutions, Xilinx has a proven and public record, rigorously validated by 3rd parties, of immunity to *hard errors*; consequently, those effects are not considered here. With regard to *soft errors* (fully correctable, nondestructive events), the main sources for terrestrial applications originate from indirect ionization, such as neutron-induced upsets from the environment, and direct ionization, such as alpha particle-induced upsets from contaminants in device packaging.

While all forms of soft errors in Xilinx devices are extremely rare, the contribution of single-event transients (SETs) and single-event functional interrupts (SEFIs) to the device SEU FIT is very low. This is attributable to the quantity, design, and layout of user-accessible storage elements, such as CLB flip-flops, DSP registers, and I/O registers. Therefore, SEUs that impact the device configuration RAM (and, to some extent, the on-chip block RAM memory elements) are the primary sources of soft errors that require mitigation in Xilinx FPGAs.



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Figure 2: Single-Event Effect Classifications

## Applications Requiring SEU Mitigation

The significant intrinsic SEU FIT/Mb reduction for UltraScale FPGAs expands the already broad application space that can benefit from these improvements without the need for additional SEU mitigation efforts. For example, a fully utilized Kintex KU040 device can be expected to experience a soft error that impacts design functionality only once every 325 years or so (benchmark location: New York).

UltraScale devices are designed to be at the heart of systems requiring high availability, high reliability, and functional safety. Some examples of such applications are shown in Table 1. For these areas, Xilinx offers the most robust, flexible, and comprehensive solutions available when additional SEU mitigation is required.

Table 1: Example Applications Where Additional SEU Mitigation Should Be Considered

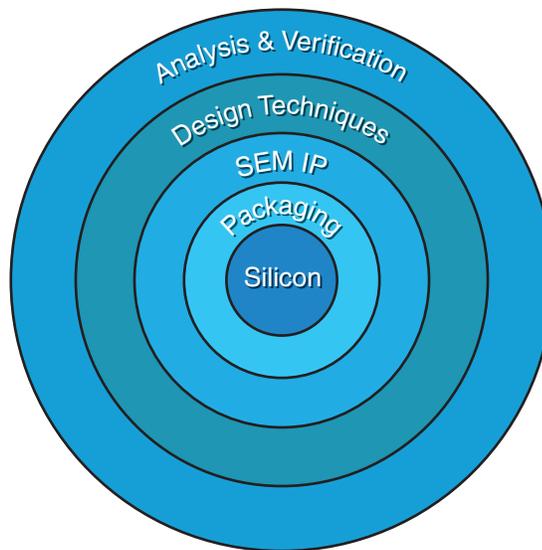
High Availability	High Reliability	Functional Safety
Wired communications	Servers	Medical
Wireless communications	Data Storage	Avionics

## SEU Solution Overview

Figure 3 illustrates Xilinx's multi-layered approach to SEU resilience and mitigation. *The comprehensive Xilinx UltraScale architecture SEU management solution is unmatched by ASICs or competing FPGA offerings.*

The three primary objectives of the UltraScale architecture SEU solution are:

- Lower the intrinsic SEU FIT/Mb for devices through innovative silicon and packaging techniques.
- Provide additional design-specific SEU mitigation, when needed, through readily available IP, integrated tool flows, and dedicated design techniques.
- Enable design-specific analysis and verification to validate the mitigation solution.



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Figure 3: Multi-layered SEU Resilience and Mitigation Solutions for UltraScale Devices

The last objective is of particular interest when evaluating other device options, such as ASICs. The unique programmable structure of Xilinx FPGAs enables testing and verification of the device and system behavior due to SEUs—which is not feasible in an ASIC solution. Techniques such as targeted fault injection into critical circuits to characterize functional impact allows for the development and testing of appropriate system responses to soft errors.

Given that soft errors cannot be eliminated in any device, understanding how the system responds *and* having the ability to efficiently develop system-level mitigation methodologies is just as important as reducing susceptibility to SEUs.

# Increased Reliability through Innovation

To deliver on the objective of significantly lowering the intrinsic SEU FIT/Mb for UltraScale devices, Xilinx has implemented multiple innovative solutions in circuit design, physical device layout, and materials management to deliver FPGAs with 3X lower SEU FIT/Mb. The foundation of these efforts starts with silicon innovations and continues with deliberate processing and packaging methods to deliver a complete physical product with industry-leading SEU resilience.

## Silicon

To counteract the tendency of SEU susceptibility to increase with shrinking process geometries, the UltraScale architecture configuration RAM cell (the largest contributor to device SEU FIT) is implemented with *over 40 circuit and layout improvements* to substantially increase its  $Q_{CRIT}$  value. In other words, the configuration RAM cell is designed and laid out to be very difficult to flip in the event of a particle strike. Xilinx uses silicon test vehicles with configuration RAM array structures to validate predicted simulation results before actual device implementation.

Furthermore, configuration RAM cells are interleaved to ensure that physically adjacent cells are not contained in the same configuration frame. The device's built-in error detection and correction logic calculates ECC values on a frame-by-frame basis. Interleaving the configuration RAM cells in this manner significantly reduces the likelihood of a multiple-bit upset occurring in a single configuration frame as the result of one SEU event. This, in turn, increases the effectiveness of the error detection and correction logic such that UltraScale devices will be able to correct over 99.9% of SEUs, whether they result in single- or multiple-bit upsets.

Finally, Xilinx devices typically have about 40% fewer configuration RAM cells compared to competing FPGAs of equivalent density, resulting in an inherently lower device SEU FIT beyond the silicon benefits already described.

As the second most significant contributor to total device SEU FIT, user memory cells in the device's block RAM also benefit from SEU mitigation. As with the configuration RAM, Xilinx has been improving the intrinsic SEU FIT/Mb of the block RAM with each successive process node through innovative circuit design and layout techniques. In addition, every block RAM has built-in single-error correct, double-error detect (SECCDED) logic that can be enabled through a parameter associated with each block RAM primitive.

## Packaging

To significantly reduce alpha particle-induced upsets from contaminants in device packaging, UltraScale devices use only ultra-low alpha (ULA) packaging with strict controls on all materials used in the assembly process. Materials used in the package underfill, microbumps, C4 bumps, and molding compound are carefully specified and monitored to minimize alpha particle contributions to the device SEU FIT.

# Increased Availability through Design Methodology

While all applications benefit from the significantly lower intrinsic SEU FIT/Mb of UltraScale devices, some applications have reliability, availability, or functional safety requirements that need additional SEU mitigation. Xilinx meets the objective of providing additional mitigation for such applications through built-in device capabilities, IP, and design techniques.

Figure 4 shows how the intrinsic SEU FIT/Mb of UltraScale devices already contributes to very high availability by minimizing total system downtime. This example assumes that 100k units of a Kintex KU040 device have been deployed in systems at sea level. By applying additional elements of the UltraScale architecture SEU mitigation solution to such a design, system availability can be further increased to meet the requirements of even the most demanding applications.

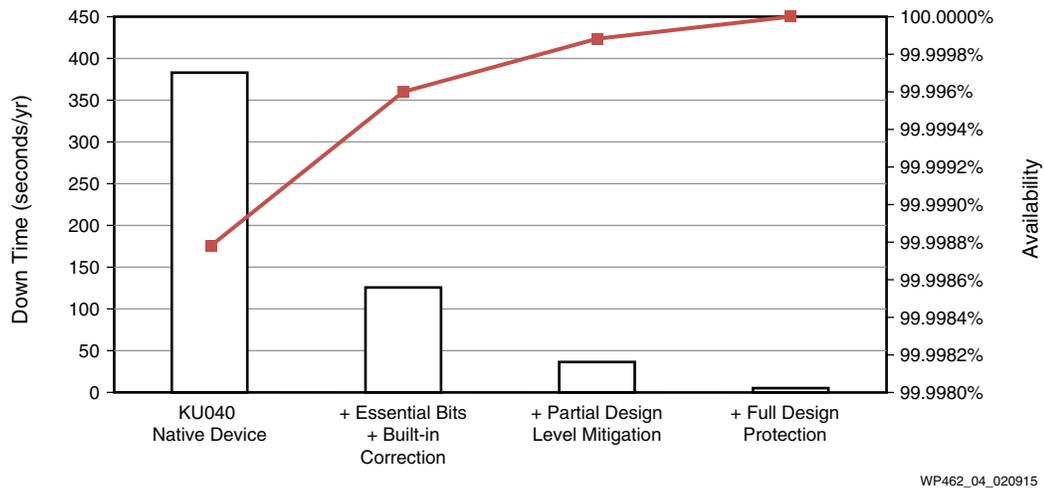


Figure 4: Increasing Device Availability through Additional SEU Mitigation

## Built-In Detection and Correction

To enhance the SEU mitigation capabilities of UltraScale devices, the configuration logic includes a built-in function that continuously scans the device configuration RAM to detect and correct single- or multiple-bit upsets. Detection and correction of soft errors in UltraScale devices is 2X faster than prior generation FPGAs, allowing upsets to be corrected in just a few milliseconds while the device continues operating in user mode.

Enhanced ECC is embedded in each configuration frame, enabling up to 8-bit error detection and 4-bit error correction per frame. Coupled with the physical frame interleaving mentioned previously, this means a device can *detect* a multiple-bit upset up to 16 bits and *correct* up to 8 bits. UltraScale devices are designed to ensure complete and robust coverage. In addition to the frame ECC capabilities, a 32-bit CRC is calculated for the entire device configuration RAM, which can reliably detect up to 31 randomized bit errors. The error detection capabilities of UltraScale devices are exceptionally strong.

Improving the error detect and correct scan time by 2X minimizes system impact in the unlikely event of an SEU event that results in a functional change to the design. SEU correction occurs transparently, leveraging Xilinx's proven glitch-free partial reconfiguration technology, with no impact to the user design other than the restoration of the intended functionality.

The error mitigation clock that determines the scan time can be provided by the built-in clock source or externally from the user design. The built-in mitigation logic also outputs a heartbeat signal. This ensures the built-in function itself is functioning properly.

## Soft Error Mitigation IP

To expand on the capabilities of the built-in detection and correction logic, Soft Error Mitigation (SEM) IP is freely available to UltraScale FPGA customers. This small footprint IP core adds advanced mitigation and verification capabilities to the solution, including:

- Essential bits error classification and reporting
- Fault injection for validating device and system response
- Enhanced correction capabilities

Essential bits are defined as the set of configuration RAM bits in a given design that have any possibility of creating a functional change to the design in the event of a change in state. In a typical design that utilizes 70% or more of the FPGA resources, only 25% to 50% of configuration RAM bits fall into the essential bits classification.

The Vivado® Design Suite allows for the creation of an essential bits mask file, which can be stored in an off-chip flash memory. The SEM IP can use this mask file to compare detected configuration RAM upsets against the known essential bits to classify and report the impact of the event. If no essential bits are impacted, the user can choose to simply correct the configuration RAM bit and continue system operation without further mitigation. This reduces the design-specific SEU FIT by 50% or more, compared to the intrinsic device SEU FIT.

The essential bits technology is intentionally conservative in its classification of configuration RAM bits that might affect the design. Testing has shown that, in practice, even upsets to essential bits have only a 10% to 30% probability of affecting design functionality.

Validation of system response to SEUs can be time consuming and costly. The UltraScale SEM IP includes fault injection features to assist designers in determining system response to SEUs. Using this knowledge, users can develop and verify fault mitigation algorithms at the system level. In addition, essential bit masking technology can be combined with fault injection to target those areas of the configuration RAM that could potentially affect the design functionality, thus further reducing verification time.

As with previous generation devices, SEM IP remains in pre-production status until it has fully passed accelerated radiation testing to ensure its robustness, at which time Xilinx provides test data and analysis reports upon request.

## Design Techniques

For applications requiring the very highest levels of design integrity, additional design-specific SEU FIT reduction can be achieved with various design techniques to reduce or even eliminate changes in device functionality from SEUs. These techniques generally involve building some form of partial or total redundancy into the design to ensure that there is no single point of failure in critical design modules.

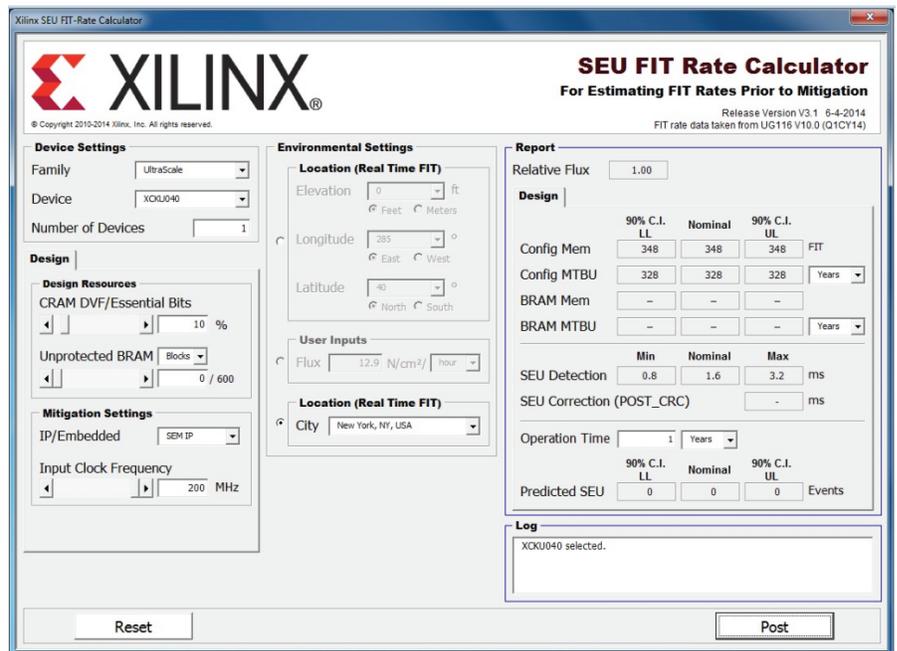
When redundancy is not required, it is valuable to use Vivado Design Suite's hierarchical design flow to restrict the placement of logic and routing as a means of separating critical design modules. This methodology eliminates the possibility of an SEU event impacting multiple design modules and allows designers to effectively analyze modules in isolation through focused fault injection on only the applicable device area.

## Analysis and Verification

Xilinx is the only vendor to openly publish SEU FIT/Mb data. This information is reported in [UG116, Device Reliability Report](#). Xilinx also assists third parties interested in validating the reported results. In addition to this published information on SEU FIT/Mb for each device family and process node, Xilinx provides tools and unique device capabilities to analyze and verify SEU mitigation requirements specific to each customer's design.

## Design Analysis

See [Figure 5](#). For analysis in the early stages of a new design, Xilinx offers an SEU FIT Rate Calculator to help designers assess device SEU FIT and plan for appropriate device and system-level mitigation methods.



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Figure 5: SEU FIT Rate Calculator for Early-Stage Estimation

When techniques such as partial triple module redundancy (pTMR) are used to protect critical design modules, the Vivado Design Suite preserves the redundant modules while also performing cross-clock domain timing analysis to assure the validity of the pTMR solution.

Designers can also assign an identifying tag to design modules, nets, primitives, or any other type of design element. This identifying tag can be used in conjunction with essential bits technology to enable different system responses, depending on how the design element impacted by a soft error is classified. With this methodology, users can customize their SEU mitigation solutions to identify and respond to SEUs in the most appropriate manner for a given application.

## Design and Device Verification

After a design has been analyzed to determine the level of SEU mitigation required, and the appropriate design techniques have been implemented to achieve the system requirements, a thorough verification methodology must be implemented to validate the solution.

The UltraScale architecture SEU mitigation solution provides means of device and system validation that are generally not possible in other technologies, such as with ASICs. UltraScale devices provide an open platform for users to perform fault injection testing via the SEM IP or through custom methods specific to a given design. This enables testing the response of the device and system to soft errors, and offers the ability to validate the applied mitigation techniques without the expense of costly accelerated radiation testing.

Xilinx actively assists customers with testing and validation of mitigation techniques implemented in Xilinx devices. Through multiple product generations of experience, Xilinx has developed the expertise to accurately predict real world SEU FIT/Mb for each new generation of products. This effort begins with simulation modeling and silicon test vehicles prior to manufacturing the first actual device.

After the first devices are received, verification of the expected device behavior is confirmed with accelerated radiation testing. Xilinx takes this process one step further by collecting real world data through real-time *Rosetta testing* (see [WP286](#), *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits*) of hundreds of devices at different latitudes, longitudes, and altitudes around the world. This allows Xilinx to correlate the results from multiple testing methodologies and provides customers with the highest confidence in the capabilities of the products and the designs implemented in these products.

## Conclusion

UltraScale devices offer industry-leading SEU resilience and mitigation through the most robust and comprehensive solutions available to manage the effects of soft errors. Through proprietary circuit and layout techniques, advanced mitigation IP, integrated tool flows, and the most complete and open verification methodology in the industry, UltraScale FPGAs offer:

- 3X lower SEU FIT/Mb than prior generation devices
- 2X faster detection and correction of upsets
- 99.9% upset correction
- Fault injection for design and test of device and system level mitigation
- Built-in ECC on block RAM to protect on-chip user data

Xilinx is the leader in SEU mitigation and is the only SRAM FPGA vendor repeatedly shown to be capable of supporting applications requiring the highest reliability, availability, and functional safety standards. UltraScale devices are the next step in Xilinx's continuing efforts to offer the most robust and comprehensive solutions available.

## Related Reading

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2. P. Rech, C. Aguiar, R. Ferreira, M. Silvestri, A. Griffoni, C. Frost, and L. Carro: *Neutron-Induced Soft Errors in Graphic Processing Units*. Retrieved [date unavailable] from: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6353714>
3. Michael Santarini: *Cosmic Radiation Comes to ASIC and SOC Design*. Retrieved May 12, 2005 from: <http://www.edn.com/design/integrated-circuit-design/4324957/Cosmic-radiation-comes-to-ASIC-and-SOC-design>
4. [WP402](#), *Considerations Surrounding Single Event Effects in FPGAs, ASICs, and Processors (Xilinx White Paper)*

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/26/2015	1.0	Initial Xilinx release.

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