WP489 (v1.1) February 20, 2019

An Adaptable Direct RF-Sampling Solution

The integration of direct RF-sampling data converters with Xilinx's Zynq UltraScale+ RFSoC technology offers the most flexible, smallest footprint, and lowest power solution for a wide range of radio applications.

ABSTRACT

To achieve the performance required of the latest generation of wireless access, DOCSIS, and a range of Aerospace and Defense applications, direct RF-sampling technology holds the promise of increased adaptability and higher performance. Direct RF-sampling enables a new level adaptability by moving much of the RF signal processing into the digital domain, thereby eliminating much of the analog signal processing[Ref 1][Ref 2].

However, there is immense market pressure to reduce the power and footprint of these systems. The solution is to integrate RF-sampling data converters with VLSI devices using advanced CMOS technology.

Xilinx has long provided a highly flexible digital signal processing solution for a range of radio applications[Ref 3][Ref 4]. Integrating direct RF-sampling data converters enables a highly adaptable platform for radio development that also addresses many of the challenges associated with current discrete direct RF-sampling solutions.

Challenges for Next-Generation Radio Systems

Meeting the challenges of future wireless access[Ref 5], DOCSIS, and radar systems involves significant changes to existing radio architectures. New architectures will leverage the latest innovations to better utilize existing spectrum and improve the capacity of networks using techniques like carrier aggregation (CA)[Ref 6], massive MiMO[Ref 7], and digital beam forming (DBF) to implement adaptive arrays[Ref 8].

The cost associated with moving data between these new RF front ends (RFFE) and the digital front end (DFE) is one of the key challenges that must be resolved to make these new technologies commercially viable. Another key requirement is increased adaptability and programmability of the RFFE to reduce time to market and provide a platform that addresses the wide range of emerging next-generation radio requirements.

The Increasing Bandwidth Problem

The Shannon-Hartley theorem defines the amount of information that can be transmitted over a wireless channel, as shown in Equation 1:

$$C = BW \times \log_2(1 + SNR) \qquad \textit{Equation 1}$$

Simply stated, C = B x log2 (1 + SNR) where C is the capacity, B is the signal bandwidth, and SNR is the signal-to-noise ratio in the channel. The information capacity (*C*) is directly proportional to the bandwidth (*BW*) of the channel. With the amount of data being transmitted over mobile wireless networks increasing by approximately 50% every year[Ref 9] and forecast to reach 30 exabytes by 2020, the demand for bandwidth is increasing at pace.

The same bandwidth pressure exists in other networks using similar radio technologies, like DOCSIS 3.1. New cable architectures like Remote PHY (R-PHY)[Ref 10], and the move to fully digital optical networks enables fully symmetrical residential data rates >1Gb/s.

In all these use cases, the basic radio must be able to support very wide bandwidths. For mobile communications in the sub-6GHz bands, RFFEs must support up to (and sometimes exceed) 400MHz of signal bandwidth for carrier aggregation, and wider contiguous bandwidth allocations becoming available above 3GHz. On the transmit and observation feedback paths used for digital pre-distortion (DPD), bandwidths over 1GHz must be supported to linearize the RF power amp (RFPA). Similar bandwidth requirements are needed to support emerging fully symmetrical DOCSIS standards, as mentioned previously. When discrete data converters send large amounts of sampled data to and from the DFE for processing, multi-gigabit sample rates on the I/O interfaces must be supported.

Figure 1 illustrates the high power cost of simply moving the data from a wideband (1GHz) 2x2 RFFE into the DFE for processing using discrete RF-sampling data converters. Even with integrated digital down-conversion (DDC) or digital up-conversion (DUC) in the data converters, large amounts of data still need to be sent to and from the DFE. The I/O power number shown for each quad transceiver (1W per, four lanes) includes the power associated with implementing the JESD204 protocol on the latest 16nm devices from Xilinx.

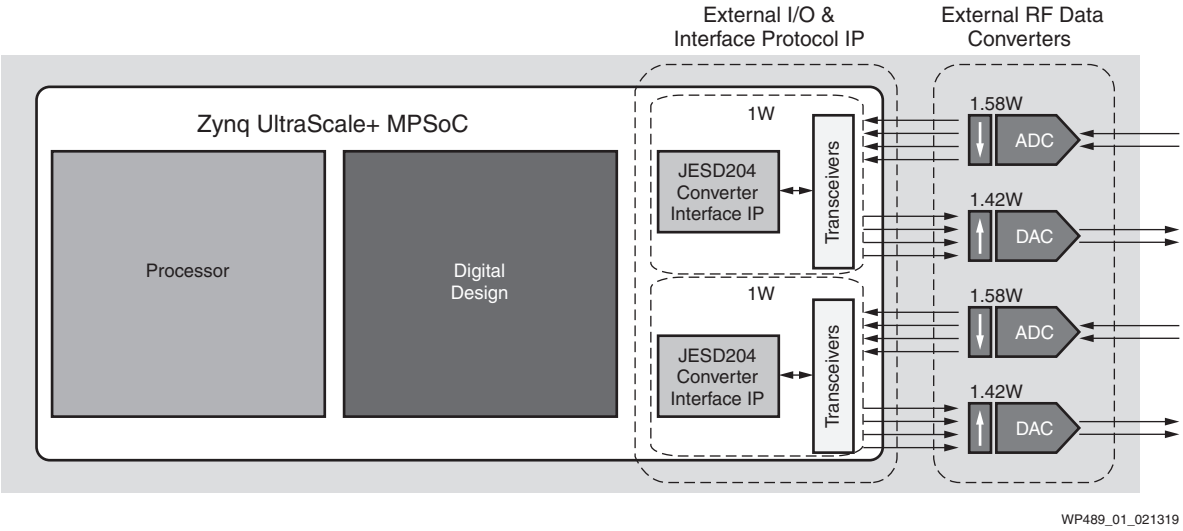

Figure 1: **Interfacing to External Wideband Data Converters Using JESD204**

In addition to the power of the interface, the power consumption of the high-sample-rate converters also needs to be addressed to lower overall system power consumption. The power of external gigasample data converter solutions remains stubbornly high. DFE signal processing has leveraged the latest deep-submicron CMOS technologies to reduce power, while RF and other analog components have traditionally leveraged older-process technology. The older CMOS and even BiCMOS technology offered the required performance at the right costs for these predominately analog ("Big A") discrete components. However, as described in Moore Digital is the Key, the move to a more digitally dominated SoC ("Big D") means that it is now commercially viable to build data converters on the latest advanced CMOS technologies, allowing huge power and cost savings.

Increasing Antenna Counts

The Shannon-Hartley theorem refers to the bandwidth of the channel as the biggest driver of wireless channel capacity. The other limiting factor is the signal-to-noise ratio (SNR) in the channel. A promising technique that can dramatically improve SNR and thus the capacity of the channel is the use of active phased arrays. This technique is sometimes referred to as *array gain* and involves the use of a large number of antennas to effectively boost the signal and minimize interference or noise. The higher antenna count can also be used to increase the capacity of the channel using MIMO techniques. This effectively increases the bandwidth without the need to allocate more spectrum[Ref 11].

Figure 2 illustrates the challenge of deploying direct RF-sampling using discrete converters in an 8-antenna system. The move to RF-sampling has already reduced the footprint by removing the analog components typically found in heterodyne radio[Ref 12]. However, for the 8T8R implementation shown, the interfacing alone (in terms of power and PCB routing) is cost-prohibitive for many applications.

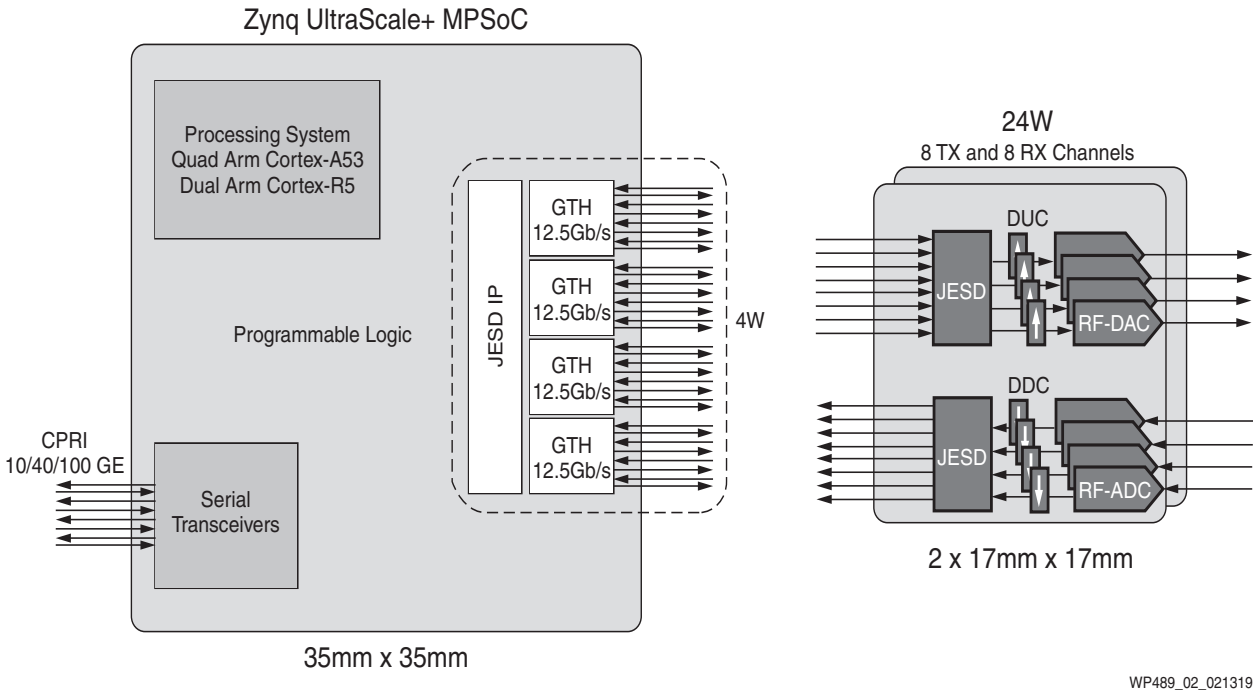

Figure 2: **Interfacing of a 8x8 RFFE to the DFE**

The implementation shown in Figure 2 assumes a discrete analog front-end solution with integrated four-channel RF-sampling ADC and DAC in a single 17mm x17mm package. This integration helps reduce the footprint of the discrete data converters; however, it does little to reduce the complexity or power of the interface. In fact, the integration of more converters into a single package can add additional layers to the PCB to route a high number of serial transceiver lanes to a more localized area on the PCB. In the example, up to four watts of power are dissipated just to move data between the DFE and RFFE. Again, as in Figure 1, the power cost of a single quad transceiver plus JESD204 IP is approximately 1W. As the number of channels grows in applications like phased array radar, which can use 100s or 1000s of channels, the discrete solution is no longer viable. Another drawback is that the discrete analog front-end data converter device requires the JESD204 interface for FPGA communication, which limits the maximum RF signal bandwidth and thus cannot employ the full Nyquist bandwidth of the data converters.

The Need for Ever-Increasing Adaptability

Future radio architectures will need platform technologies that can address a wide range of requirements with the same basic hardware. The ability to leverage the same hardware to address diverse requirements and emerging standards allows vendors to react quickly to new market opportunities. In the case of 5G systems, for example, it is becoming clear that no one type of radio will address the diverse needs of next-generation radio access networks (RANs). Consequently, the number of different radio types can be expected to increase significantly[Ref 13].

Xilinx's adaptable SoCs and FPGAs have provided very flexible solutions for implementing the DFE and interfacing requirements for recent radio generations. The same level of flexibility and programmability must be pushed closer to the antenna in the next generation of radios to move towards the goal of software-defined radio (SDR). Direct RF-sampling, integrated with highly optimized RF digital signal processing engines (i.e., DDC and DUC), offers a much more flexible

approach to traditional analog frequency translation and filtering. By leveraging advanced CMOS technology, RF signal processing, with excellent power and cost efficiency, can be implemented in the digital domain. As a result, the RF-sampling solutions deliver a very flexible RF front end with the ability to deal with very wide bandwidths—up to 2GHz—at a much lower power consumption than analog technologies. By pushing data converter sample rates and analog bandwidth higher, the data converters can be moved closer to the antenna, enabling much of the signal processing to be done in the digital domain, thus moving closer to Mitola's vision of a fully software-defined radio[Ref 14], as shown in Figure 3.

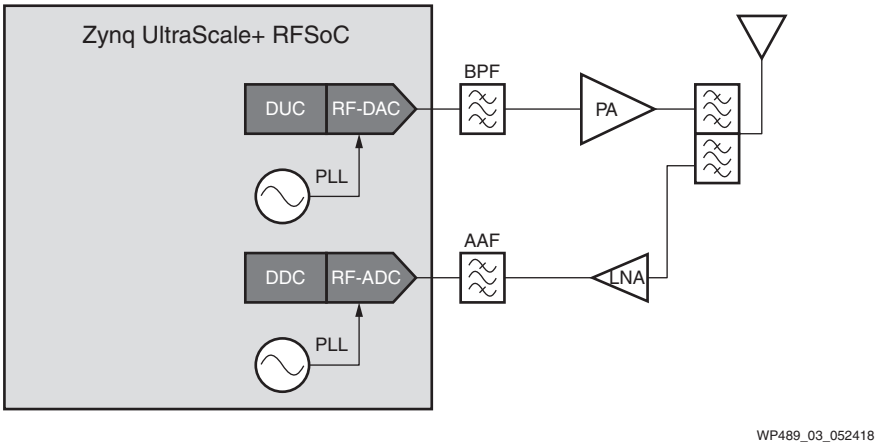

Figure 3: **Software Defined Radio Using Zynq UltraScale+ RFSoC**

Moore Digital is the Key

Direct RF-sampling data conversion enables the application of Moore's Law to analog. It allows analog/RF signal processing to be moved into the digital domain, where advantage can be taken of advanced CMOS technology; the same functionality can be then delivered in a much smaller area at lower power[Ref 1]. Advanced FinFET process technologies are enabling new digitally assisted analog techniques that greatly improve the power efficiency of these circuits versus complex analog components[Ref 15].

The integration enabled by these technologies addresses the key challenges of power reduction and increasing channel counts. Also, by moving much of the signal processing into the digital domain, the path to a more flexible or adaptable solution is realized. Xilinx's portfolio of FPGAs and SoCs have provided a uniquely flexible radio development platform for a number of generations[Ref 3]. As such, Xilinx devices are a natural platform for the integration of direct RF-sampling data converters.

Advantages of RF-Sampling ADCs and DACs

Other direct RF-sampling benefits include the reduced complexity of the RFFE (see Figure 4). The higher sample rates supported by these RF-ADCs and RF-DACs greatly simplifies the analog filtering requirements and also allows a better trade-off between dynamic range (SNR) and signal bandwidth in the digital domain by decimating and filtering the ADC output to extract only the signal bandwidth of interest[Ref 1]. The large unused portions of the Nyquist bandwidth of the converter can also be used to inject band-limited dither to improve the converter linearity.

Implementing the signal conditioning in the digital domain also yields better performance and ease of use. Some of the traditional RF impairments in the intermediate frequency (IF) approach are greatly reduced or eliminated, e.g., passband ripple, group delay variation, matching, local oscillator (LO) leakage issues, etc.

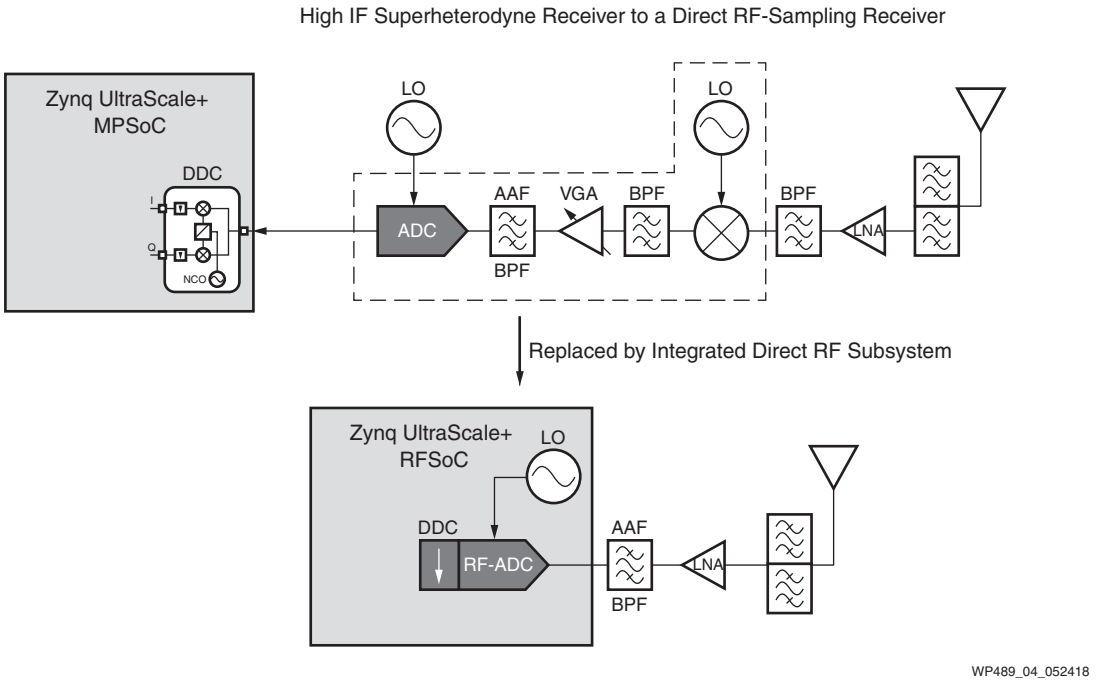

Figure 4: **Comparison of Superheterodyne and Direct Sampling Receivers**

A widely used metric of converter performance is the effective number of bits (ENOB). It is often cited to suggest that lower sample rate converters or using the data converters in the first Nyquist zone with IF or zero intermediate frequency (ZIF) architectures is the optimal approach from a receiver performance and power efficiency point of view.

However, ENOB can be misleading. It is much more useful to evaluate the noise spectral density (NSD) of the converter. For example, the ADC full scale NSD is a better measure of the receiver blocker tolerance and dynamic range[Ref 16][Ref 17]. The problem with ENOB is that it combines noise and all distortion artifacts into a single metric. But these non-idealities affect receivers in different ways and thus need to be treated separately[Ref 18].

A Fully Integrated RF Signal-Processing Front End

The integration of direct RF-sampling ADCs and DACs into Xilinx devices addresses many of the challenges associated with current SDR platforms based on ZIF or heterodyne architectures. The Xilinx devices offer a feature-rich platform that includes DSPs, general purpose processor (GPPs), programmable logic, and optimized RF signal-processing blocks (i.e., DDCs and DUCs).

While the primary goal is to provide a more flexible (software programmable) radio, the integration also eliminates the need for external I/O interfaces, which can consume a significant amount of power, as shown in Figure 1. Eliminating external I/O also removes:

- A significant bottleneck in existing SDR solutions[Ref 19].
- The large number of clocks needed to drive the JESD204 interfaces.

- The complexity of routing the clocks on the PCB and synchronizing all the links.

The elimination of the external interfaces also greatly reduces system power. Recent direct RF-sampling implementations on the latest CMOS technology have also been shown to produce very favorable benchmarks in terms of power and cost when compared to traditional integrated heterodyne implementations[Ref 17]. Figure 5 shows how the RF-sampling converters can be implemented in 9W versus 36W using discrete solutions.

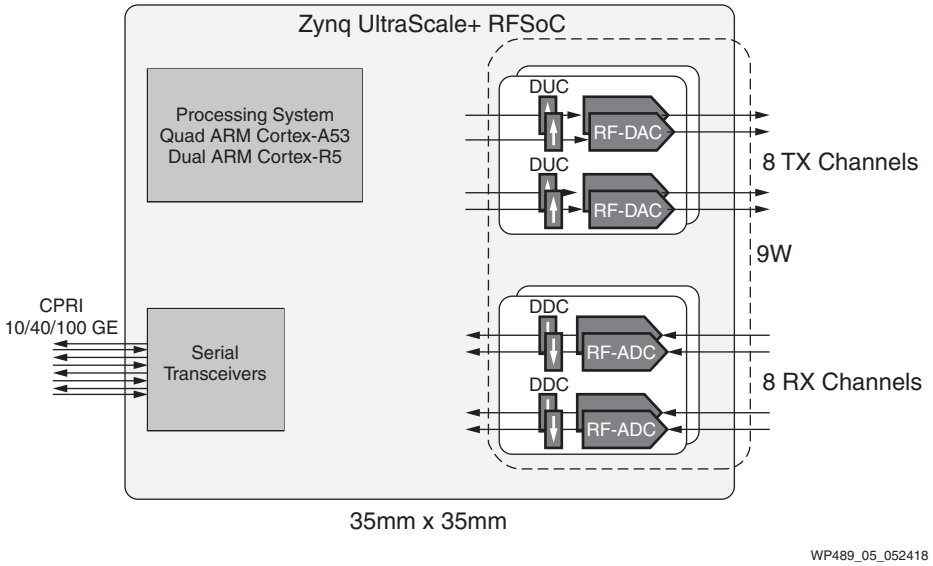

Figure 5: **RF Front End Based Zynq UltraScale+ RFSoC**

It is clear from Figure 5 that the impact this level of integration brings is very disruptive when compared to Figure 2. The integration of a large number of converters enables the deployment of increased channel counts within a much smaller footprint, enabling many of the advanced transmission technologies like massive MIMO and digital beam-forming described in Challenges for Next-Generation Radio Systems to become commercially viable. It also enables phased array radar systems to leverage full or partial digital beam forming techniques or even multi-function radars that address both weather and aviation applications for example. The integration of the RF-sampling data converters can reduce the power and footprint of these multi channel system by 50% or more.

Xilinx Implements High Performance Data Converters in 16nm FinFET Technology

Xilinx has made significant investments in the area of high-performance data converters built on advanced 16nm FinFET CMOS technology. The Zynq UltraScale+ RFSoC family(1), which has entered full production, integrates state-of-the-art direct RF-sampling data converters using digitally assisted techniques and low-phase noise PLLs for on-chip sample clock synthesis [Ref 20][Ref 21][Ref 23]. The data converters are arranged in tiles that contain two or four converters along with low phase noise clocking and dedicated digital signal processing blocks. Figure 6 illustrates one of the RF-DAC tiles and Figure 7 one of the RF-ADC tiles integrated into the RFSoCs. The larger devices contain 16 RF-DACs and 16 RF-ADCs.

1. See http://www.xilinx.com/rfsoc.

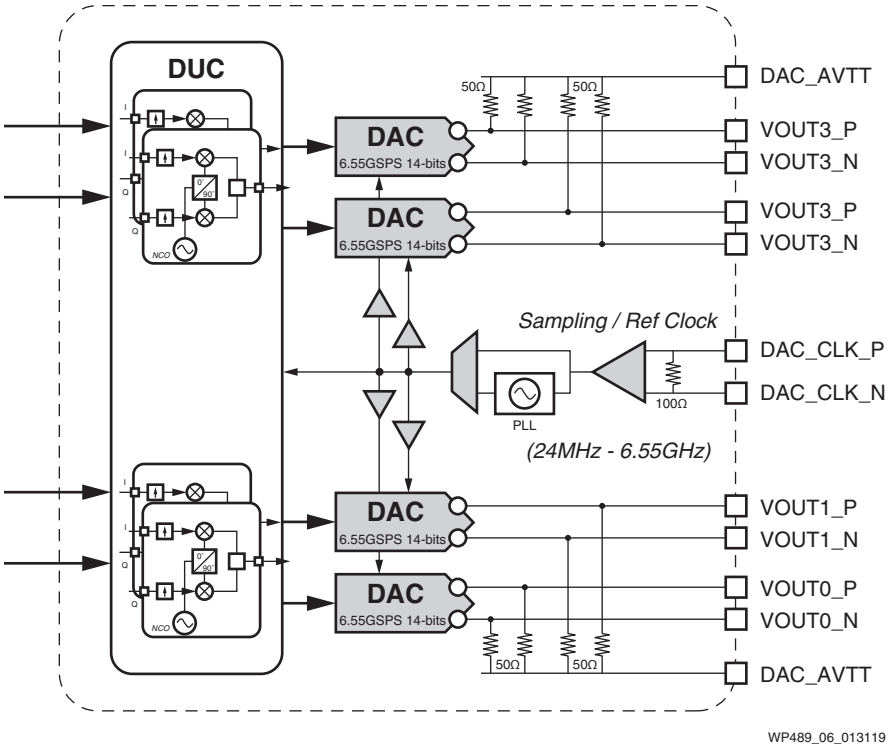

Figure 6: **A Single 6.55GSPS RF-DAC Tile**

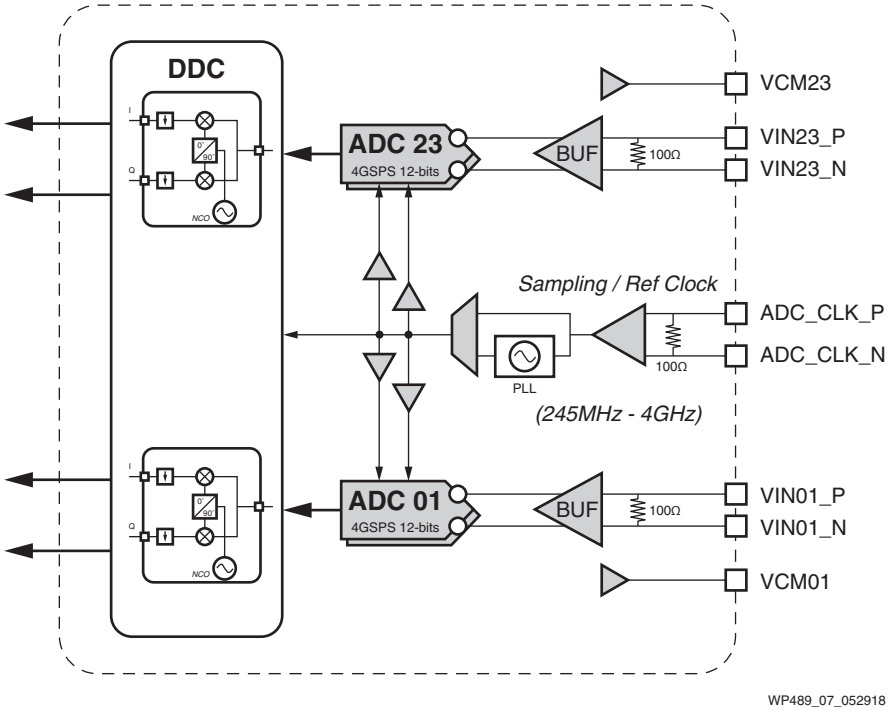

Figure 7: **A Single 4GSPS RF-ADC Tile**

The RF-DACs are 14-bit, 6.55GSPS converters and support an RF output bandwidth of 4GHz. The RF-DAC achieves an NSD of typically -160dBm/Hz with a output carrier frequency of 3.5GHz. The RF-ADCs are 12-bit, 4GSPS and support an RF input bandwidth of 4GHz. The RF-ADC achieves an

NSD of typically -153dBm/Hz with a 3.5GHz input tone. The Zynq UltraScale+ RFSoC supports an 8T8R configuration (16 data converters) of these tiles at a power consumption of ~9W at full sample rate including digital up/down conversion.

Next-Generation Products

Xilinx continues to build on this first generation of data converter technology to offer significant improvements in both performance and reduced solution cost.

The Zynq UltraScale+ RFSoC Gen 2 extends the RF analog bandwidth to 5GHz while meeting the development time lines for 5G NR bands in Asia.

The Zynq UltraScale+ RFSoC Gen 3 family pushes RF analog BW to 6 GHz with the RF-DACs sample rates of 10GSPS and the RF-ADCs sample rates up to 5GSPS and 14-bit resolution. The data converters support direct RF sampling for all of the new sub 6GHz 5G bands and provide more complete coverage for L, S, and C bands for radar applications. The higher bandwidth supports higher IFs for emerging 5G mmWave bands to reduce the cost and complexity of the RF line up.

In addition to enhanced analog/RF performance of the converters, the Zynq UltraScale+ RFSoC Gen3 devices include additional dedicated digital signal processing (i.e., digital down conversion and digital up conversion) to further reduce the solution cost and power consumption. The clocking requirements are also greatly simplified to reduce the number of external high frequency sampling clocks or reference clocks required in most systems. This has a significant impact on the power and cost of clock generation and distribution in high channel count systems.

A Comprehensive Platform for Radio Development

The silicon, while important, is only half of the platform solution. A fully integrated tool flow for the design and verification of the radio solution is critical. Xilinx offers a comprehensive tool flow that encompasses logic design, embedded software development, and simulation. Figure 8 illustrates how the complexity of adding a data converter subsystem with up to 32 RF sampling converters to a design is greatly reduced. An easy to use GUI provides an intuitive interface to configure and instantiate the converters with guaranteed timing and interfacing. No FPGA / HDL design experience is required to quickly configure and add the converters to a design. If run-time configuration is required, the supplied API and SW drivers allow this to be easily accomplished.

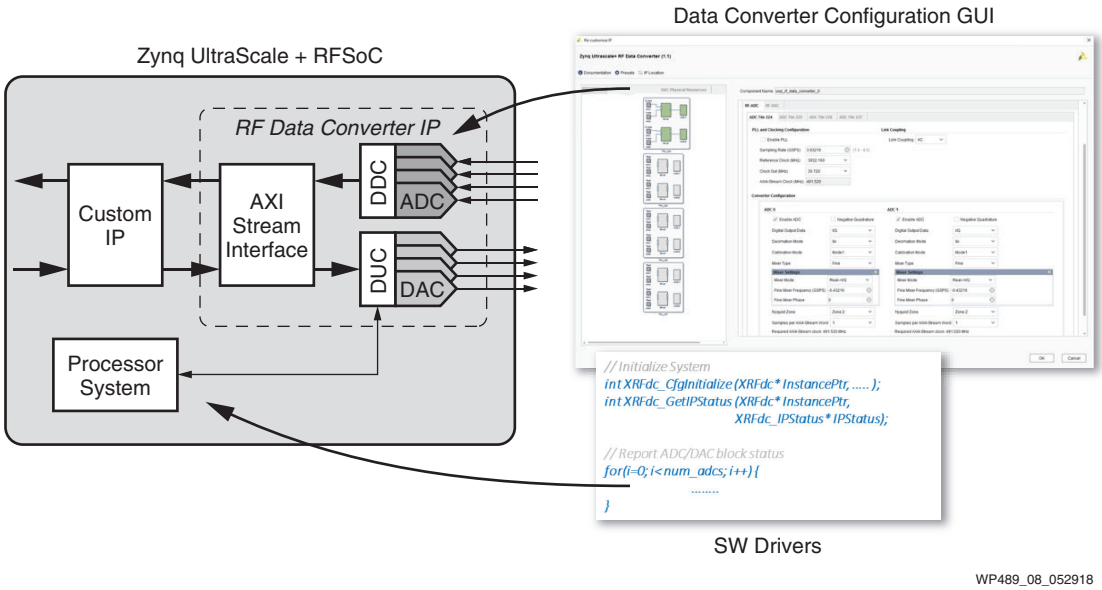

Figure 8: **RF Data Converter Vivado Tool Support**

For an overview of Xilinx's comprehensive development tools, go to the Developer Zone[Ref 24] on the Xilinx website. Xilinx's SoC and FPGA technology is becoming increasingly accessible to a wider range of engineers, including software engineers and architects working at the system level. High levels of abstraction in the tools allow design entry using C/C++[Ref 25] and at even higher levels of abstraction by using tools like MATLAB® and Simulink® from the Mathworks[Ref 25].

One of the key benefits of developing on a programmable platform is the ability to verify and validate the design including the RFFE on the same silicon that will be used in production. The co-verification of the DFE and RFFE can now be accomplished in a much more seamless and effortless way using a common design platform. Xilinx also supplies evaluation and prototyping platforms, which are fully integrated into the development tools. For example, the ZCU111 evaluation board for the Zynq UltraScale+ RFSoC is an ideal platform on which to prototype a design or just evaluate the data converter performance.(1)

Summary

Deploying next-generation radio solutions has its challenges. Due to the combination of wider bandwidths and higher channel counts, it is clear that the interface between the DFE and RFFE must be eliminated. At the same time a wide range of radio types needs to be supported. A single flexible platform to reduce time to market and development costs is required.

A platform based on Xilinx's new Zynq UltraScale RFSoC family with integrated RF-sampling data converters is a compelling solution that can satisfy these challenges. This disruptive technology is the closest solution yet to a true SDR implementation on a single device.

For more information, go to: www.xilinx.com/RFSoC.

1. Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit

References

1. Umesh Jayamohan, Technical Article, *Analog Devices*: "Not Your Grandfather's ADC: RF Sampling ADCs Offer Advantages in Systems Design".
2. Tommy Neu, *Texas Instruments*, White Paper, May 2015: "Direct RF conversion: From vision to reality".
3. IEEE, *Proceedings of the IEEE,* Vol. 103, No. 3, March 2015: "Software-Defined Radio: Bridging the Analog–Digital Divide".
4. Xilinx White Paper WP445, "Enabling High-Speed Radio Designs with Xilinx FPGAs and SoCs".
5. Xilinx White Paper WP476, "Toward 5G Xilinx Solutions and Enablers for Next-Generation Wireless Systems".
6. Jeanette Wannstrom, *3GPP The Mobile Broadband Standard,* website page accessed January 2017: "Carrier Aggregation Explained".
7. Ove Edfors, Lund University, (YouTube video published August 2015), accessed January 2017: "Understanding Massive MIMO in Roughly Two Minutes".
8. *Wikipedia,* article accessed January 2017: "Phased Array".
9. Cisco White Paper, "Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2015–2020".
10. CableLabs Remote PHY Specification, https://apps.cablelabs.com/specification/CM-SP-R-PHY.
11. Lipfert, Hermann (August 2007). MIMO OFDM Space Time Coding – Spatial Multiplexing, Increasing Performance and Spectral Efficiency in Wireless Systems, Part I Technical Basis (Technical report). Institut für Rundfunktechnik.
12. Maxim Integrated Application Note 6063, *LTE-LTE-A Release 12 Transmitter Architecture: Analog Integration*, https://www.maximintegrated.com/en/app-notes/index.mvp/id/6063
13. METIS Deliverable 6.6, "Final report on the METIS 5G system concept and technology roadmap".
14. Joe Mitola, *IEEE Communications Magazine, May 1995:* "The Software Radio Architecture".
15. Boris Murmann, *IEEE Micro*, Volume: 26, Issue: 2, March-April 2006: "Digitally Assisted Analog Circuits".
16. Gabriele Manganaro and David H. Robertson, *Analog Devices*, Use Noise Spectral Density to Evaluate ADCs in Software-Defined Systems.
17. Ramon Gomez, *IEEE Transactions on Circuits and Systems,* Vol. 63, No. 8, August 2016: "Theoretical Comparison of Direct-Sampling versus Heterodyne RF Receivers".
18. Scott Kulchycki, *National Semiconductor*, reprinted by *EETimes RF & Microwave Designline,* "Software Defined Radio: Don't Talk to Me about ENOBs, Part 1" and [op. cit.] "Part 2".
19. George Sklivanitis et al., *IEEE Communications Magazine,* January 2016: "Addressing Next-Generation Wireless Challenges with Commercial Software-Defined Radio Platforms".
20. Bruno Vaz et al., *ISSCC 2017:* "A 13b 4GS/s Digitally-Assisted Dynamic 3-Stage Asynchronous Pipeline-SAR ADC".
21. Christophe Erdmann et al., *ISSCC 2017:* "A 330mW 14-bit 6.8GS/s dual-mode RF-DAC in 16nm FinFET achieving -70.8dBc ACPR in a 20MHz channel at 5.2GHz".
22. Didem Turker et al. *ISSCC 2018* "A 7.4-to-14GHz PLL with 54fsrms jitter in 16nm FinFET for integrated RF-data-converter SoCs".
23. Xilinx website page: Hardware Optimization
24. Xilinx website page: Vivado® High-Level Synthesis
25. Xilinx website page: System Generator

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/20/2019	1.1	Updated title, abstract, and made updates throughout to include details of the Zynq UltraScale+ RFSoC portfolio. Updated Figure 1 and Figure 2.
04/27/2017	1.0.1	Typographical edits to Figure 2.
02/17/2017	1.0	Initial Xilinx release.

Disclaimer

Automotive Applications Disclaimer