XAPP1307 (v1.0.1) June 23, 2017

1G to 10G Ethernet Dynamic Switching Using High-Speed Serial I/O Solution in the UltraScale Architecture

Author: Haris Akkool, Srini Gaddam

Summary

This application note targets the Ethernet designs that require dynamic switching between 1Gb/s to 10Gb/s using high-speed serial I/O links. The design uses the Xilinx® Ethernet Solution Suite along with a Xilinx GTH/GTY Transceiver to form the Ethernet interface. The same GT is used to interface with the gigabit Ethernet Physical Coding Sublayer/Physical Media Dependent (PCS/PMA) and the 10G Ethernet PCS/PMA IP core. The rate switching is handled using the Dynamic Reconfiguration Port (DRP) of GTs.

The design targets the evaluation boards listed in Table 1.

Table 1: **Supported Devices and Kits**

Product Family	Device	Kit	Design Support	
			Simulation	Board
UltraScale™	Kintex® UltraScale	KCU105	Yes	Yes
	Virtex® UltraScale	VCU108	Yes	Yes
UltraScale+™	Virtex® UltraScale+	VCU118	Yes	Yes
	Zynq UltraScale+™ MPSoC	ZCU102-ES2	Yes	Yes

Download the reference design files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design.

Reference Design

Ethernet is the Media Access Control (MAC) specification that has been defined in the IEEE 802.3 standard specification and is a widely used universal standard deployed in network solution suite. Ethernet has found wide applicability due to its scalability across generations. As Ethernet is evolving from the earlier 10/100/1000 Mb/s speed to 10 Gb/s and 100 Gb/s physical media speed, the network equipment that is already deployed across multiple network stations requires an upgrade.

To comply with the legacy Ethernet devices, Ethernet infrastructure must retain legacy Ethernet interfaces. The Ethernet interface (MAC) does not depend on physical media as long as the target speed is supported by the physical interface. For example, 1G and 10G Ethernet can use a common optical interface for transporting Ethernet traffic to the end point. To support both

the legacy and the 10 Gb/s Ethernet interface using the same physical interface, dynamic switching capability is required in the Ethernet PHY device.

Xilinx offers a vast portfolio of Ethernet IP cores including the 1G and 10G Ethernet MAC, and 1G and 10G Ethernet PCS/PMA. The Ethernet MAC has an AXI4-Stream compliant user interface and the MAC IP encapsulates the user payload in the form of Ethernet frames and transfers the data over to the PCS/PMA core. The PCS/PMA core uses physical layer encoding to convert the Ethernet frames to the specification defined encoded frames and sends the data over to the GT block. The PCS/PMA core performs GT initialization and the PHY housekeeping function.

The GT interface implements the serialization and deserialization functionality. The serial bit period of the serialized data depends on the reference clock used in the GT and the GT PLL's clock dividers. To enable switching from 1G to 10G line rates, the PLL multipliers and dividers must be changed. The 1G and 10G links require different physical encoding schemes to be performed. These are primarily implemented in the GT. The transceiver attributes used to configure protocol specific settings can be modified during runtime with the DRP interface. The DRP sequence is followed by a reset sequence of the GT which brings the transceiver back to normal operating condition.

This application note presents a solution to control the design using the DRP interface while switching from a 1G to 10G line rate. Download the reference design files for this application note from the Xilinx website.

Hardware

Figure 1 displays the reuse of the same transceiver for both 1G and 10G protocols. The GT channel (hard block) is separated from the PCS/PMA IP core and is configured using the DRP controller.

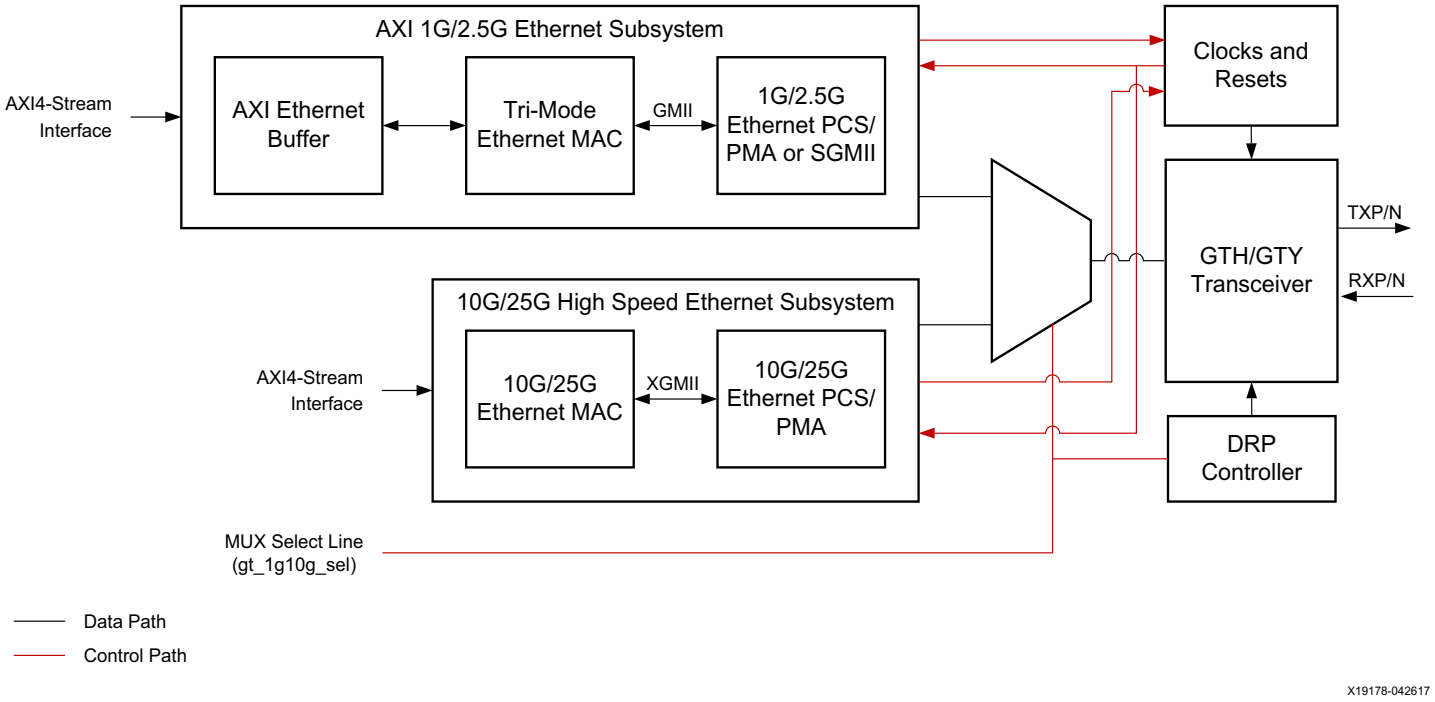

Figure 1: **Hardware Block Diagram**

The 1G/10G Ethernet Subsystem reference design supports a throughput up to 10 Gbps by varying its attributes. The DRP controller is designed to write suitable values in the appropriate register locations of the GT channel. This function enables configuration from 1G to 10G protocols and vice versa according to user input (select line to the 2:1 MUX).

The Ethernet packet is transferred via 1G MAC - 1G PCS/PMA and arrives at input 1 of the 2:1 MUX, while the 10G packet arrives at input 0 of the MUX. The user-driven select line of the MUX controls the routing of the Ethernet packet to the GT interface.

The DRP controller also takes in a select line as input to determine the configuration of the GT. Appropriate values are written to the corresponding registers through the DRP interface of the GT based on the select line input. The addresses and values to be written to the GT registers are fixed, and they are hard-coded in the DRP controller. This allows the DRP controller to dynamically reconfigure the GT.

AXI 1G/2.5G Ethernet Subsystem

The AXI Ethernet Subsystem represents a hierarchical design block containing multiple infrastructure cores that become configured and connected during the system design session. Infrastructure cores for this subsystem are the Xilinx Tri-Mode Ethernet MAC (TEMAC) and 1G/2.5G Ethernet PCS/PMA or Serial Gigabit Media Independent Interface (SGMII) cores.

See *AXI 1G/2.5G Ethernet Subsystem Product Guide* (PG138) [Ref 1] for more information.

Tri-Mode Ethernet MAC

The Ethernet MAC is defined in IEEE 802.3-2012 specification clauses 2, 3, and 4. The MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can be connected to, any type of physical layer. Ethernet speed is configured for 1 Gbps and enabled by the AXI buffer and drivers.

See *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051) [Ref 2] for more information.

1G/2.5G Ethernet PCS/PMA or SGMII

The 1G/2.5G Ethernet PCS/PMA or SGMII core provides a flexible solution for connection to an Ethernet MAC or other custom logic. It supports the 1000 BASE-X PCS and PMA operation, as defined in the IEEE 802.3-2012 standard. The Physical interface is configured to support the 1000 BASE-X standard. The shared logic and GT are configured to be included in the example design.

See *1G/2.5G Ethernet PCS/PMA or SGMII LogiCORE IP Product Guide* (PG047) [Ref 3] for more information.

10G/25G High Speed Ethernet Subsystem

The 10G/25G High Speed Ethernet Subsystem represents a hierarchical design block containing multiple infrastructure cores that become configured and connected during the system design session. Infrastructure cores for this subsystem are the 10G/25G Ethernet MAC and 10G/25G Ethernet PCS/PMA (10G/25G BASE-R) cores.

See *10G/25G High Speed Ethernet Subsystem Product Guide* (PG210) [Ref 4] for more information.

10G/25G Ethernet MAC

The 10G/25G Ethernet MAC core connects to the PHY layer through an external 10-gigabit media independent interface (XGMII). The PHY layers are managed through an optional Management Data Input/Output (MDIO) STA master interface. Configuration of the core is done through a configuration vector. The Ethernet MAC core performs the Link function of the 10G Ethernet standard. The core supports 802.3 in transmit and receive directions. Ethernet speed is configured for 10.3125G and the datapath interface is AXI4 Stream.

See *10G Ethernet MAC LogiCORE IP Product Guide* (PG072) [Ref 5] for more information.

10G/25G Ethernet PCS/PMA (10G/25G BASE-R)

10GBASE-R/KR is a 10 Gbps serial interface. It is intended to provide the PCS and PMA functionality between the XGMII interface on a 10 Gigabit Ethernet MAC and a 10 Gigabit Ethernet network PHY. PCS/PMA is configured to support the 10GBASE-R protocol with a 64-bit datapath and the shared logic and GT sub core are configured to be included in the example design.

See *10G Ethernet PCS/PMA LogiCORE IP Product Guide* (PG068) [Ref 6] for more information.

Clocking and Reset

The reference design uses a single 156.25 MHz reference clock for both 1G and 10G line rate selections. The reference design sources a 156.25 MHz reference clock from the Si570 on the ZCU102/KCU105 evaluation board. The Virtex UltraScale design (VCU108) sources a 156.25 MHz reference clock from Si570s on the XM107 FMC loopback board. The Virtex UltraScale+ design (VCU118) sources a 156.25 MHz reference clock from the Si570 on the FMC+ loopback board. The reference clock is connected as an input clock source to the GTH/GTY transceiver (GTHE3/4_CHANNEL and GTYE4_CHANNEL) block's channel PLL instance for a 1G line rate and to the Quad PLL instance for the 10G line rate.

The PLL multipliers and dividers set the output TXOUTCLK and RXOUTCLK frequency as the serial line rate/parallel datapath width. TXOUTCLK and RXOUTCLK are used to generate TXUSRCLK/TXUSRCLK2 and RXUSRCLK/RXUSRCLK2 in the FPGA general interconnect. Figure 2 shows the clocking strategy used for a GTH Transceiver (GTHE3/4_CHANNEL) in the Kintex® UltraScale™, Virtex® UltraScale™ and Zynq® UltraScale+™ MPSoC designs.

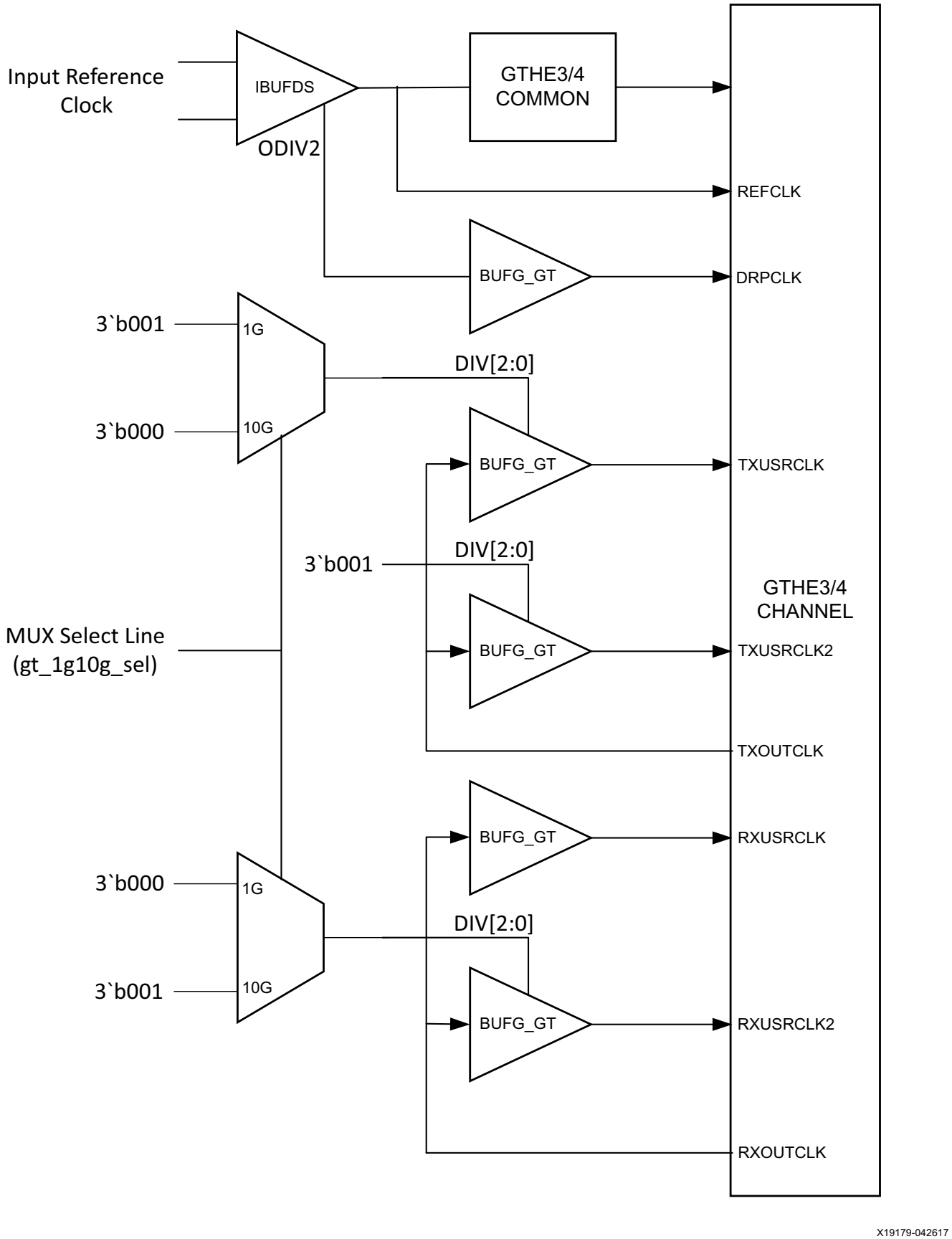

Figure 2: **Clock Strategy for 1G and 10G Line Rates**

The summary of clocking strategy used in the Kintex® UltraScale™, Virtex® UltraScale™, and Zynq® UltraScale+™ MPSoC designs is as follows:

- The 1G transceiver logic runs at TXUSRCLK/TXUSRCLK2 frequency which is a 62.5 MHz clock for the 20-bit parallel datapath width.
- The 1G Ethernet PCS/PMA core works on a 10-bit interface at the user clock frequency of 125 MHz.
- The 10G Ethernet transceiver logic works at 322.23 MHz with a parallel datapath width of 32-bits.
- The 10G Ethernet PCS/PMA core operates at 156.25 MHz with a parallel data width of 64-bits.

Figure 3 shows the clocking strategy used for the GTY transceiver (GTYE4_CHANNEL) in the Virtex® UltraScale+™ design.

The summary of the clocking strategy used in the Virtex® UltraScale+™ design is as follows:

- The 1G transceiver logic runs at TXUSRCLK/TXUSRCLK2 frequency which is a 62.5 MHz clock for the 20-bit parallel datapath width.
- The 1G Ethernet PCS/PMA core works on a 10-bit interface at the user clock frequency of 125 MHz.
- The 10G Ethernet transceiver logic works at 156.25 MHz with a parallel datapath width of 64-bits.
- The 10G Ethernet PCS/PMA core operates at 156.25 MHz with a parallel data width of 64-bits.

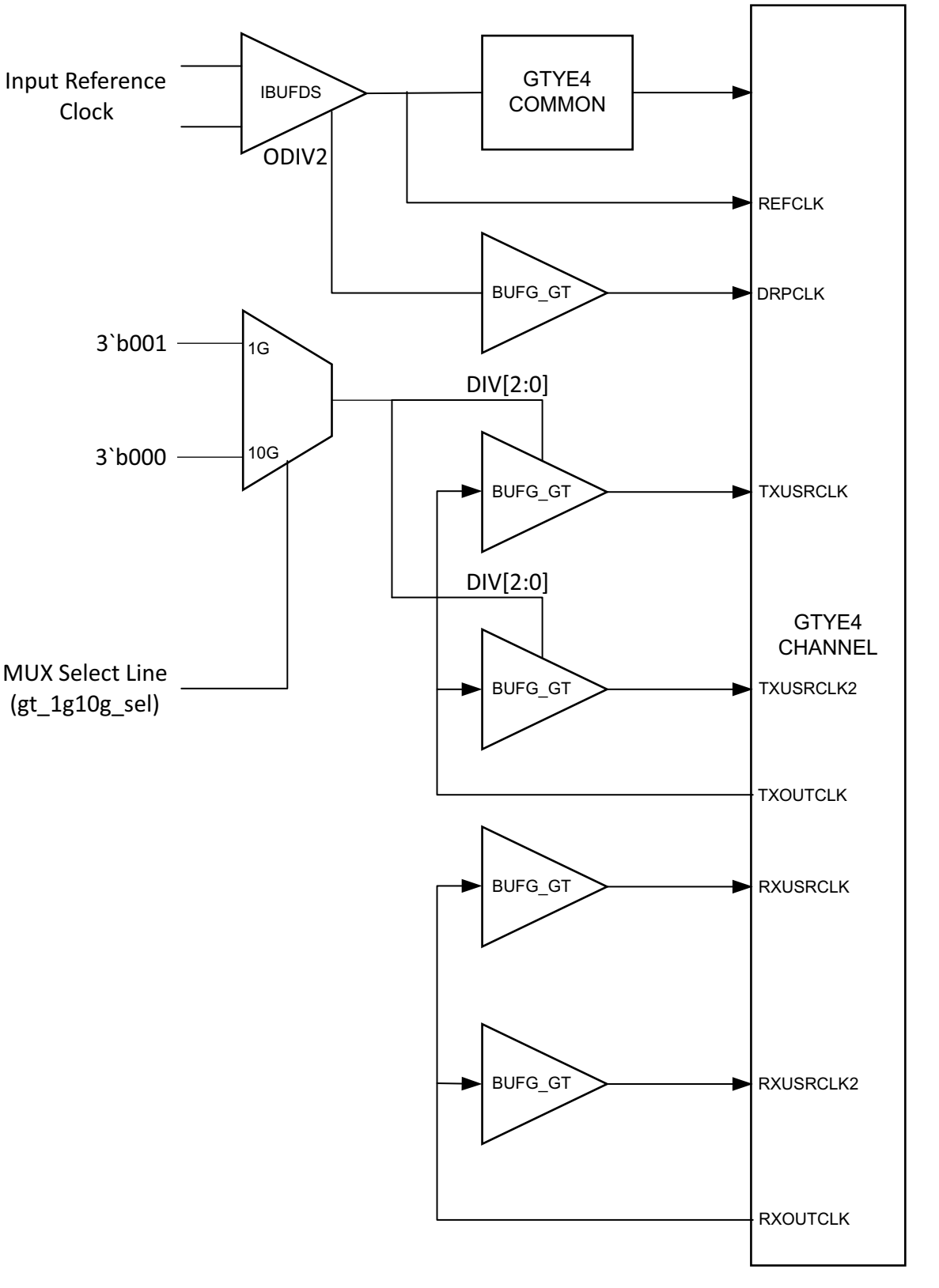

Figure 3: **Clock Strategy in Virtex UltraScale+ Design**

Resetting the GTH/GTY transceiver used in the design is controlled by the reset sequence that is generated from the 1G/10G Ethernet PCS/PMA reference design. After the DRP controller completes, the attribute configuration for the 1G to 10G rate change and vice-versa, it generates a reset to the 1G/10G Ethernet PCS/PMA reference design that drives the reset sequence for the GTH/GTY transceiver used in the design.

DRP Controller

The DRP controller implements the finite state machine (FSM) to write attribute values in the corresponding GT registers. The FSM is synchronized by a stable clock and is triggered by the MUX select line (user input). The attribute values of the GT for both 1G and 10G protocols are hard-coded and stored as a ROM in the DRP controller. The output of the DRP controller is mapped to the GT DRP interface. The implemented FSM follows the standard procedure to write or read the DRP registers of the UltraScale GTH/GTY transceiver, as mentioned in the *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 7] and *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 8]. The DRP controller FSM flowchart is shown in Figure 4.

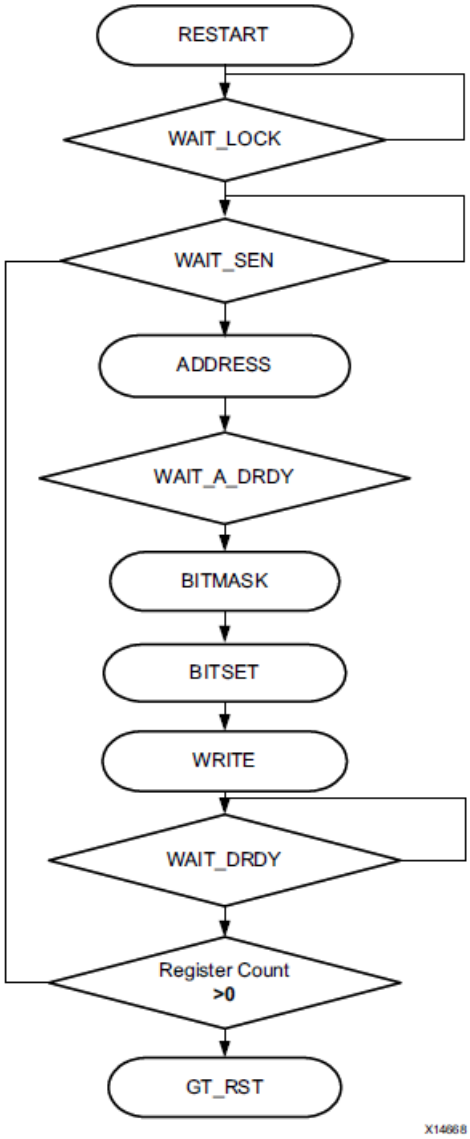

Figure 4: **Design Flow**

RESTART: The ROM starting address and the output values are initialized to zero.

WAIT_LOCK: The FSM polls for CPLL lock (for 1G) or QPLL (for 10G). After the PLL is locked, it moves to the next state.

WAIT SEN: The FSM waits in this state until the MUX select line value (user input) is toggled to select the 1G rate option from the previous 10G selection and vice versa. Based on this trigger, the starting address to fetch the attribute values from the ROM is assigned.

ADDRESS: In this state, a read from the GT registers is enabled and the attribute register address is set.

WAIT_A_DRDY: The logic implements a read to verify the write procedure. Thus, the attribute values are initially read and then altered. This state polls for the ready signal from the GT to be asserted.

BITMASK: The portions of bits of the attribute register which are not to be altered are masked in this state.

BITSET: The attribute register bits are set in this state.

WRITE: The new value of the attribute is written to the corresponding register location.

WAIT_DRDY: This state polls for the ready signal from the GT to be asserted as an acknowledgment to a successful write.

Register Count: In this state, the total number of the attribute registers to be changed is monitored. The FSM moves to the ADDRESS state until the register count becomes zero, indicating that all the registers are written.

GT_RST: The GT channel is reset to apply the new attribute values written. The FSM moves to the WAIT LOCK state and subsequently remains in the WAIT_SEN state until another SEN rising pulse is obtained.

Reference Design - Tool Flow and Verification

Download the reference design files for this application note from the Xilinx website. The checklist in Table 2 shows the reference design matrix.

Table 2: **Reference Design Matrix**

Parameter	Description
General	
Developer name	Xilinx
Target devices	UltraScale Architecture (UltraScale, UltraScale+, and Zynq UltraScale+ MPSoC) (xczu9eg-ffvb1156-2-i-es2, xcku040-ffva1156-2-e, xcvu9p-flga2104-2L-e-es1, and xcvu095-ffva2104-2-e)
Source code provided	Yes
Source code format	Verilog
Design uses code and IP from existing Xilinx application note and reference designs or third party	1G/2.5G Ethernet PCS/PMA or SGMII (Xilinx)
	Tri-Mode Ethernet MAC (Xilinx)
	10G/25G Ethernet MAC (Xilinx)
	10G/25G Ethernet PCS/PMA (10G/25G BASE-R) (Xilinx)
Simulation	
Functional simulation performed	Yes
Timing simulation performed	No
Test bench used for functional and timing simulations	Yes

Table 2: **Reference Design Matrix *(Cont'd)***

Parameter	Description
Test bench format	Verilog
Simulator software/version used	Vivado® simulator 2017.1
SPICE/IBIS simulations	No
Implementation	
Synthesis software tools/versions used	Vivado synthesis
Implementation software tools/versions used	Vivado implementation
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	ZCU102 Evaluation Board
	KCU105 Evaluation Board
	VCU108 Evaluation Board
	VCU118 Evaluation Board

Requirements

Hardware

- KCU105 board with the Kintex UltraScale XCKU040-2FFVA1156E FPGA
- VCU108 board with the Virtex UltraScale XCVU095-2FFVA2104E FPGA
- ZCU102 board with the Zynq UltraScale+ XCZU9EG-2FFVB1156I (ES2) MPSoC
- VCU118 board with the UltraScale+ XCVU9P-L2FLGA2104E FPGA
- Two USB cable, standard-A plug to micro-B plug
- Power Supply: 100 VAC-240 VAC input, 12 VDC 5.0A output
- One SFP+ 10GBASE-SR/SW transceiver modules (Avago Technologies)
- One SFP+ Loopback cable
- One XM107 FMC Loopback board
- One FMC+ Loopback board
- A laptop or a desktop with Microsoft Windows 7/Linux Operating System to run Vivado Design Suite and configure the FPGA

Design Tools and Software

- Vivado Design Suite 2017.1
- USB UART drivers (Silicon Laboratories CP210x VCP drivers)

Reference Design Files

The directory structure of all the designs is the same. Figure 5 shows the directory structure of the Kintex UltraScale (KCU105) design files.

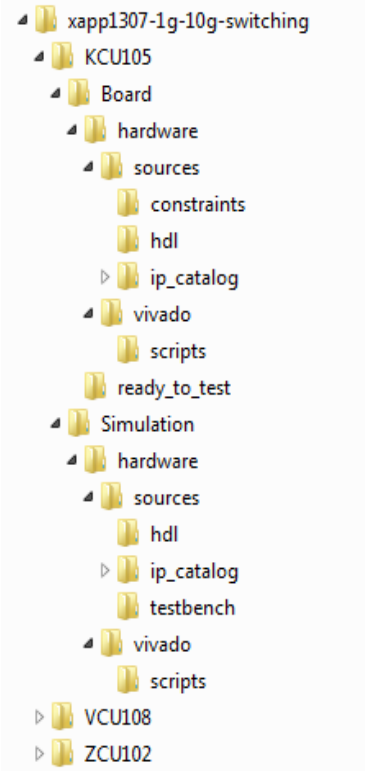

Figure 5: **Directory Structure**

The KCU105 folder contains the following hardware design deliverables:

- The `Board` folder contains all required scripts and a programming file for board test.
- The `Simulation` folder contains all required scripts and a test bench file for simulation.
- The `sources/constraints` folder contains the I/O and timing constraints file.
- The `sources/hdl` folder contains the source code deliverable files.
- The `sources/ip_catalog` folder contains the Xilinx IP cores required for this design.
- The `sources/testbench` folder contains the test bench files for simulation.
- The `vivado/scripts` folder contains the implementation and simulation scripts for the design for both Windows and Linux operating systems in command line and Vivado Design Suite IDE mode.
- The `ready_to_test` folder contains programming files to configure the KCU105 Evaluation Board.
- The `readme.txt` file provides the details on folder structure, tool version, and revision.

Licensing

See the following product pages for details about licensing the 10G/25G Ethernet Subsystem and AXI 1G/2.5G Ethernet Subsystem:

- 10G/25G Ethernet Subsystem
- AXI 1G/2.5G Ethernet Subsystem

Reference Design Steps

This section describes the 1G/10G switching reference design setup, execution, and results.

KCU105 Evaluation Board Setup

Figure 6 shows the KCU105 connection diagram to bring up the Kintex UltraScale design.

1. Connect the KCU105 board to the control computer and power supply.
2. Insert the SFP+ module into the SFP cage (SFP0) on the KCU105 board and connect the fiber optic cable.
3. Set the KCU105 board switches and jumpers as shown in Figure 6.
4. Switch ON SW1 to power the KCU105 board.

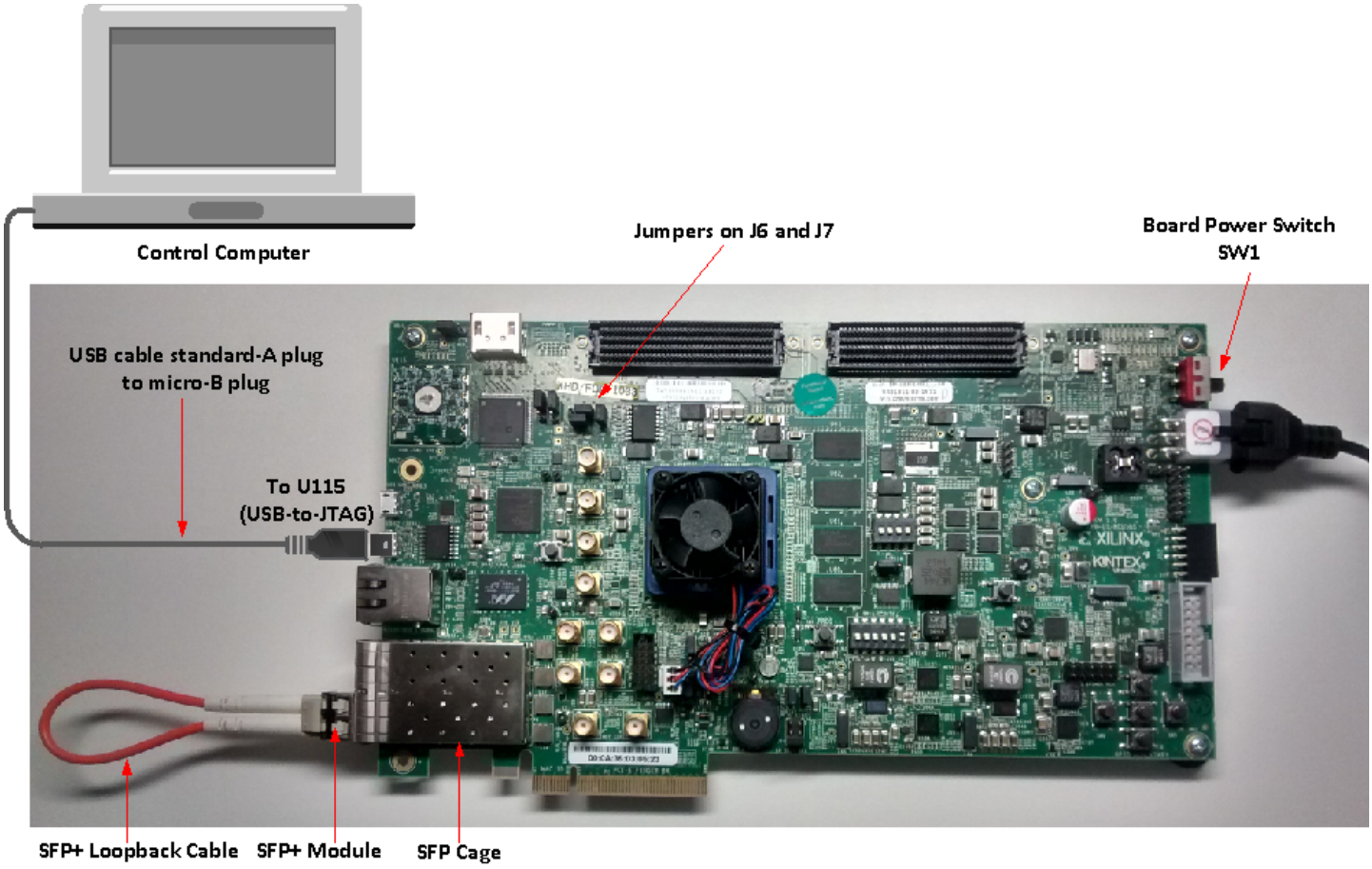

Figure 6: **KCU105 Board Setup for Reference Design**

ZCU102 Evaluation Board Setup

Figure 7 shows the ZCU102 connection diagram to bring up the Zynq® UltraScale+ MPSoC design.

1. Connect the ZCU102 board to the control computer and power supply.
2. Insert the SFP+ module into the SFP cage (SFP0) on the ZCU102 board and connects the fiber optic cable.
3. Set the ZCU102 board switches and jumpers as shown in Figure 7.
4. Switch ON SW1 to power the ZCU102 board.

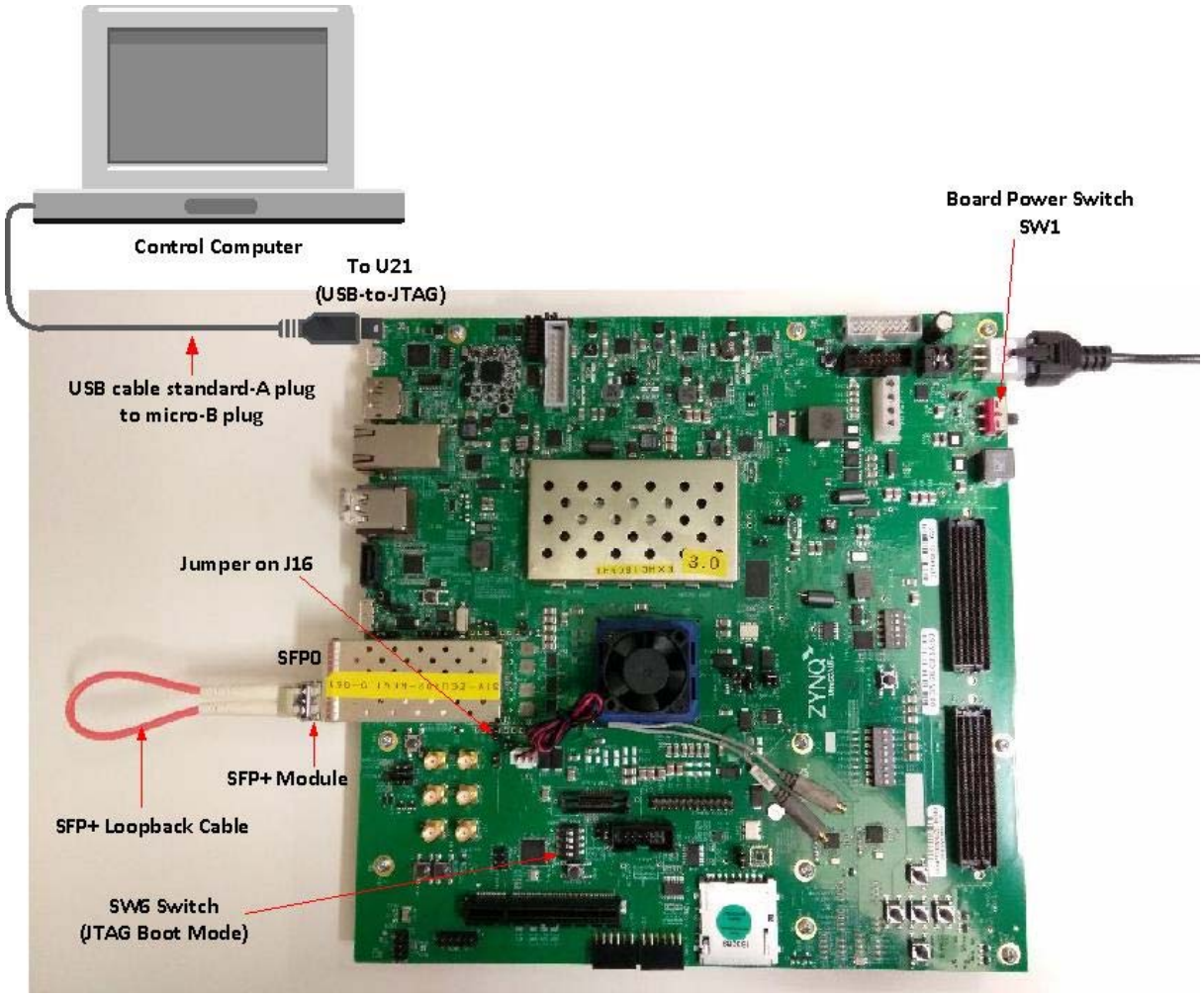

Figure 7: **ZCU102 Board Setup for Reference Design**

VCU108 Evaluation Board Setup

Figure 8 shows the VCU108 connection diagram to bring up the Virtex® UltraScale™ design.

1. Connect the VCU108 board to the control computer and power supply.
2. Insert the XM107 FMC loopback board into the FMC HPC1 connector (J2) on the VCU108 board.
3. Switch ON SW1 to power the VCU108 board.
4. Install the UART driver and terminal program. Refer to VCU108 Software Install and Board Setup (XTP368) [Ref 11] for details on installing and configuring the USB to UART drivers and Tera Term.

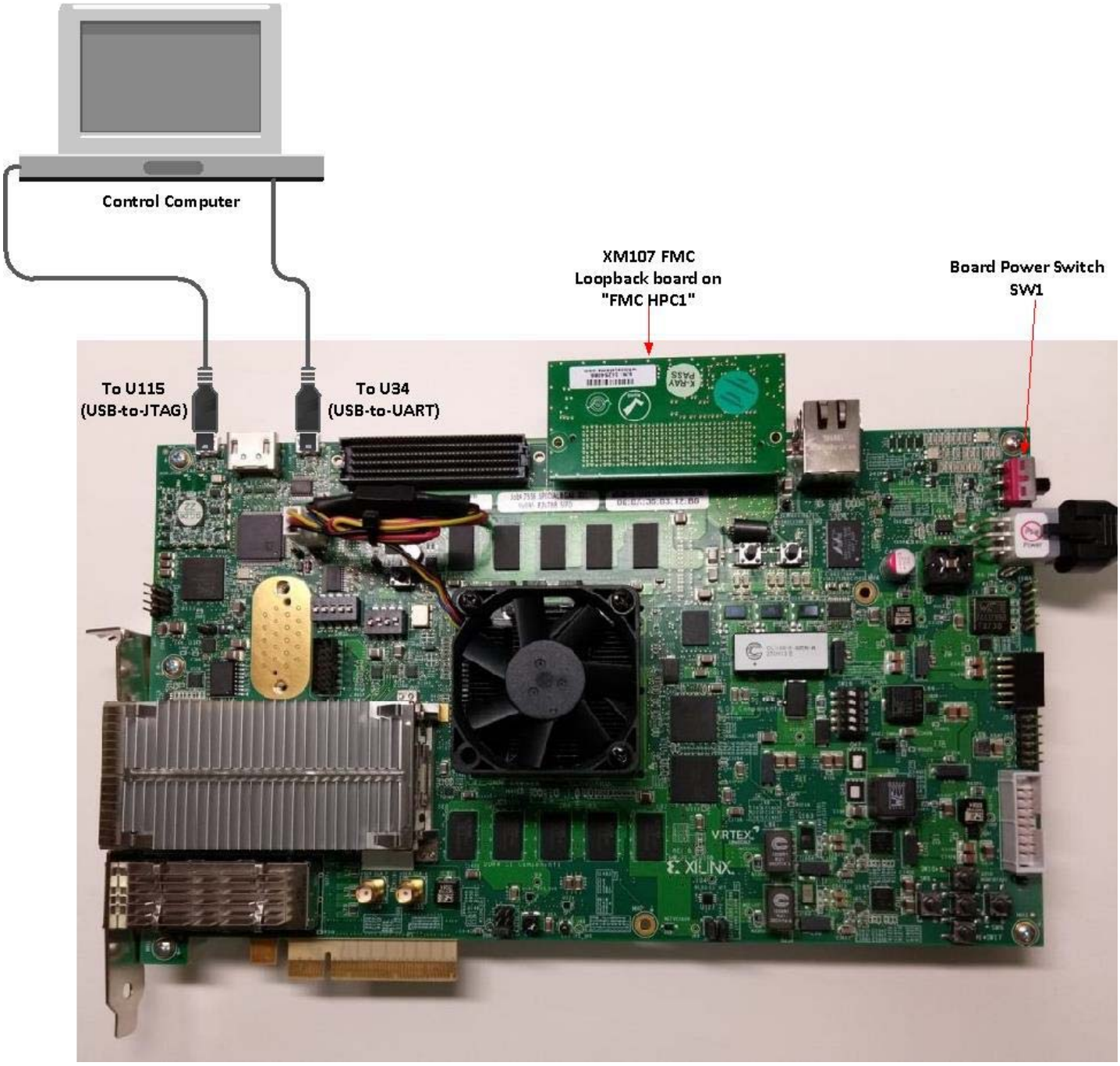

Figure 8: **VCU108 Board Setup for Reference Design**

Clock Setup

The reference design uses a single 156.25 MHz reference clock for both 1G and 10G line rate selections. The reference design sources a 156.25 MHz reference clock from Si570s on the XM107 FMC loopback board.

1. Open a terminal window for the Enhanced COM Port (System Controller COM Port).
2. Cycle board power and review system controller UART output (Press **Enter** after each entry)
3. Press **4**, **1**, **4**, and **2**, then **156.25** to set the XM107 on FMC HPC1 to 156.25 MHz. Figure 9 shows the FMC HPC1 clock setup in the terminal.

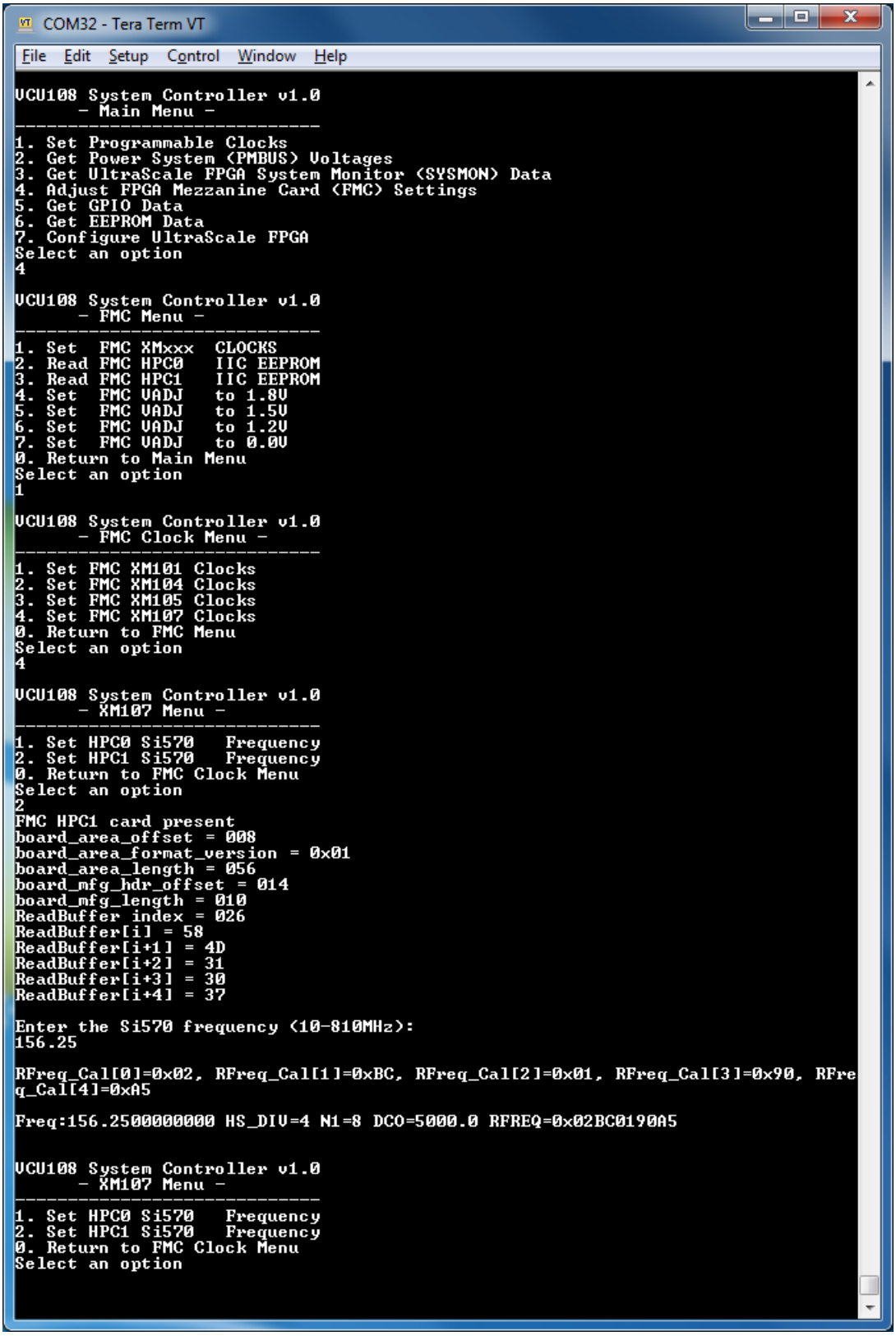

Figure 9: **Reference Clock Setup on XM107 FMC Loopback Board**

VCU118 Evaluation Board Setup

Figure 10 shows the VCU118 connection diagram to bring up the Virtex® UltraScale+™ FPGA design.

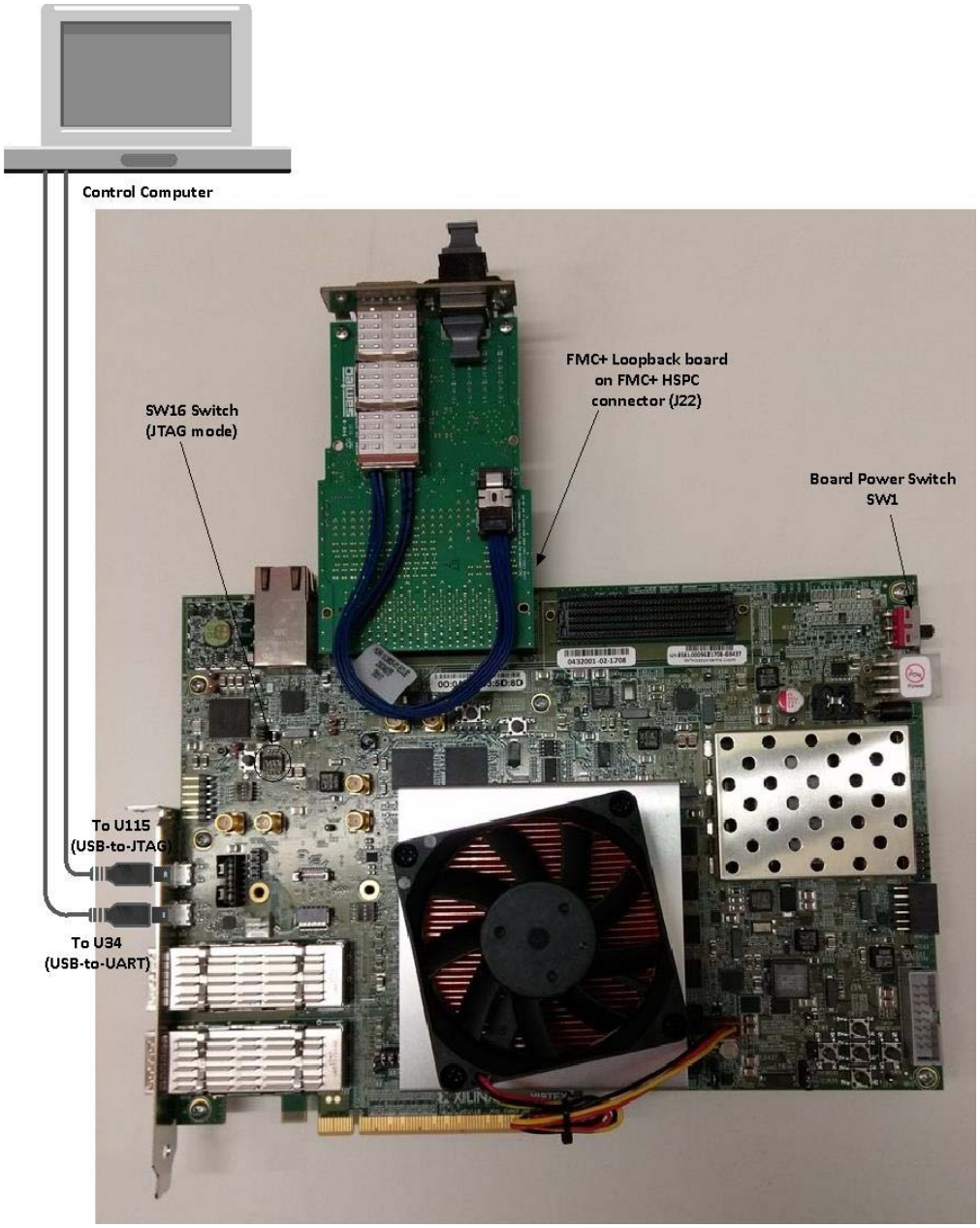

Figure 10: **VCU118 Board Setup for Reference Design**

1. Connect the VCU118 board to the control computer and power supply.
2. Insert the FMC+ loopback board into the FMC+ HSPC connector (J22) on the VCU118 board.
3. Set SW16 to 0101 (1 = ON, Position 1 to Position 4).
4. Power the VCU118 board by placing switch SW1 to the ON position.

5. Install the UART driver and terminal program. Refer to VCU118 Software Install and Board Setup (XTP449) [Ref 12] for details on installing and configuring the USB to UART Drivers and Tera Term.

Clock Setup

The reference design uses a single 156.25 MHz reference clock for both 1G and 10G line rate selections. The design sources a 156.25 MHz reference clock from the Si570 on the FMC+ loopback board. The System Controller User Interface (SCUI) is used to set up the reference clock. See *VCU118 System Controller – GUI Tutorial* (XTP447)[Ref 10] for details on using the System Controller GUI.

1. Select FMC > HPC0 > XM107 tab.
2. Set 156.25, and click Set SI570 button, as shown in Figure 11.

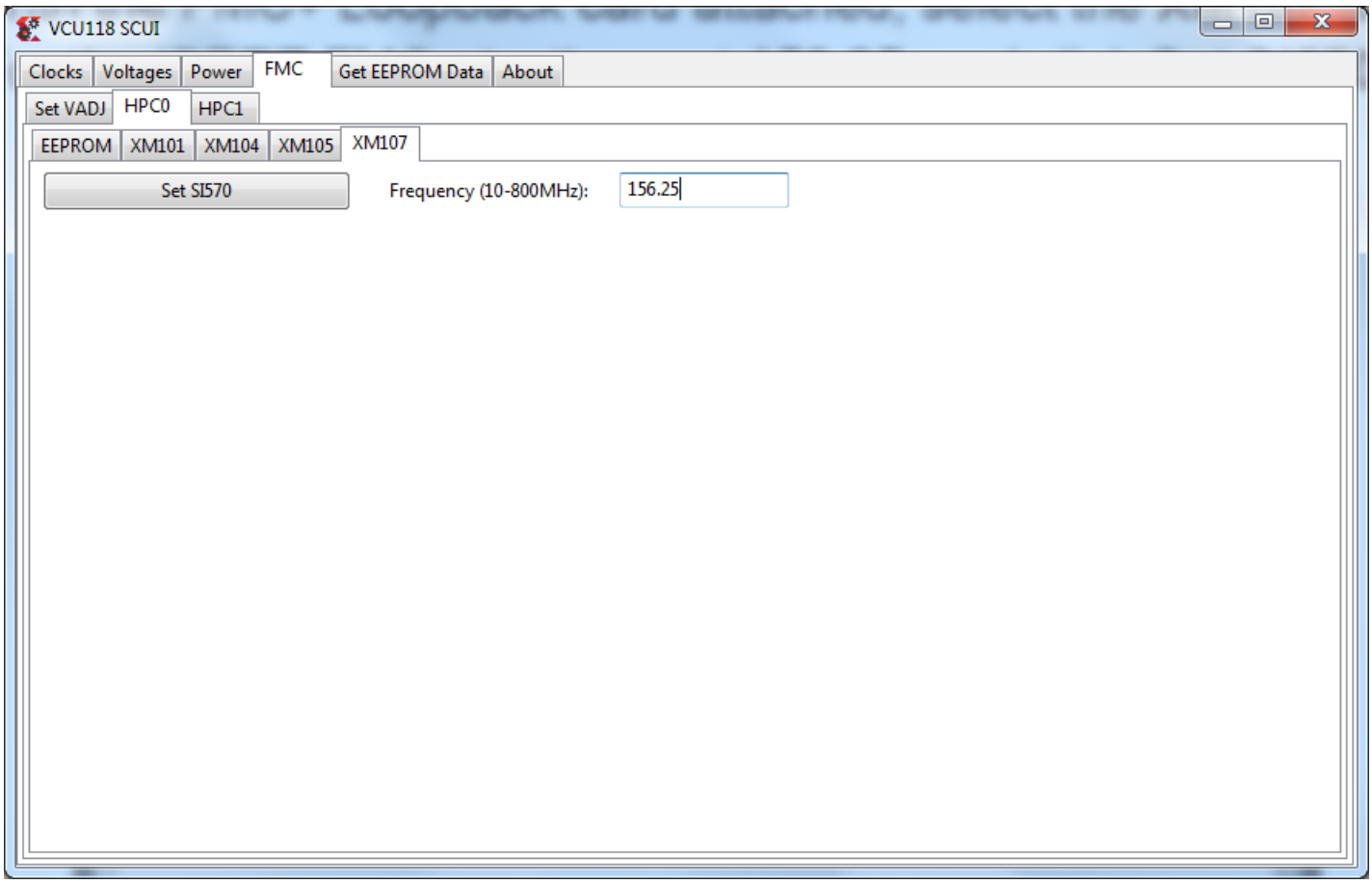

Figure 11: **Reference Clock Setup on FMC+ Loopback Board**

Executing the Reference Design

The procedures for simulating the design, programming the BIT file, and testing the design are the same for all the reference designs. Use the appropriate files for running the design. The following sections describe the steps to simulate, program and test the Kintex® UltraScale™ design on the KCU105 evaluation board.

Simulating the Design

1. Launch the Vivado Integrated Design Environment (IDE) on the control computer.

On Windows 7:

   a. Click **Start > All Programs > Xilinx Design Tools > Vivado 2017.1 > Vivado 2017.1**.

   b. On the getting started page, click on **Tcl Console**.

   c. In the Tcl console type:

```
cd <working_dir>/KCU105/Simulation/hardware/vivado/scripts
source kintex_ultrascale_1g_10g.tcl
```

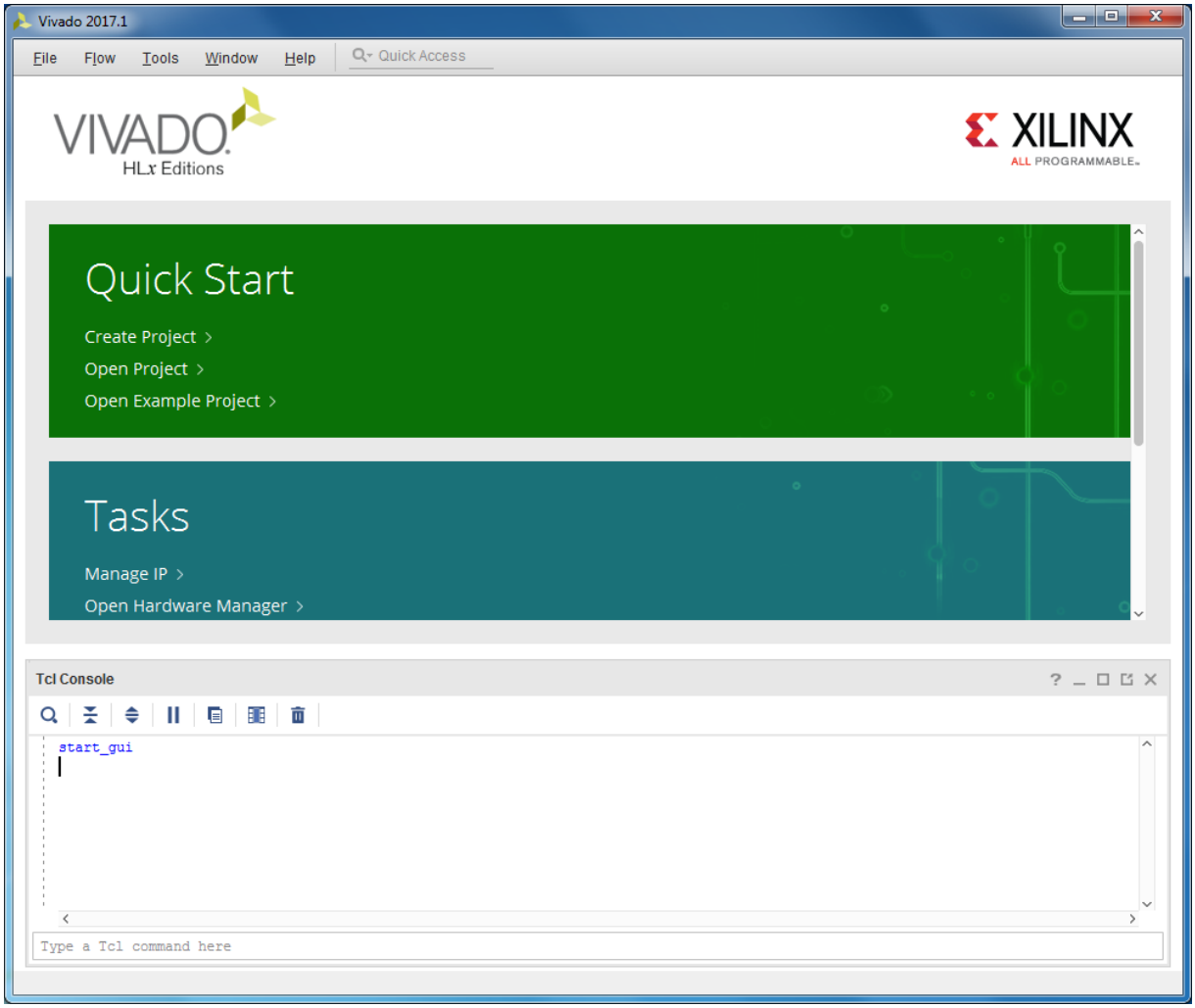

Figure 12: **Vivado IDE and Tcl Console**

On Linux:

a. On a terminal window, change the directory to the following location:

```
<working_dir>/KCU105/Simulation/hardware/vivado/scripts
```

b. At the command prompt, type:

```
vivado -source kintex_ultrascale_1g_10g.tcl
```

Programming the BIT File

1. Launch the Vivado Integrated Design Environment (IDE) on the control computer.
2. On the getting started page, click on Tcl Console.
3. In the Tcl console, type:

```
cd <working_dir>/KCU105/Board/hardware/vivado/scripts
source kintex_ultrascale_1g_10g.tcl
```

4. In the Tool Flow Navigator under Program and Debug, click **Open Hardware Manager**.
5. Open the connection wizard to initiate a connection to the KCU105 board. Click **Open Target > Open New Target** as shown in Figure 13.

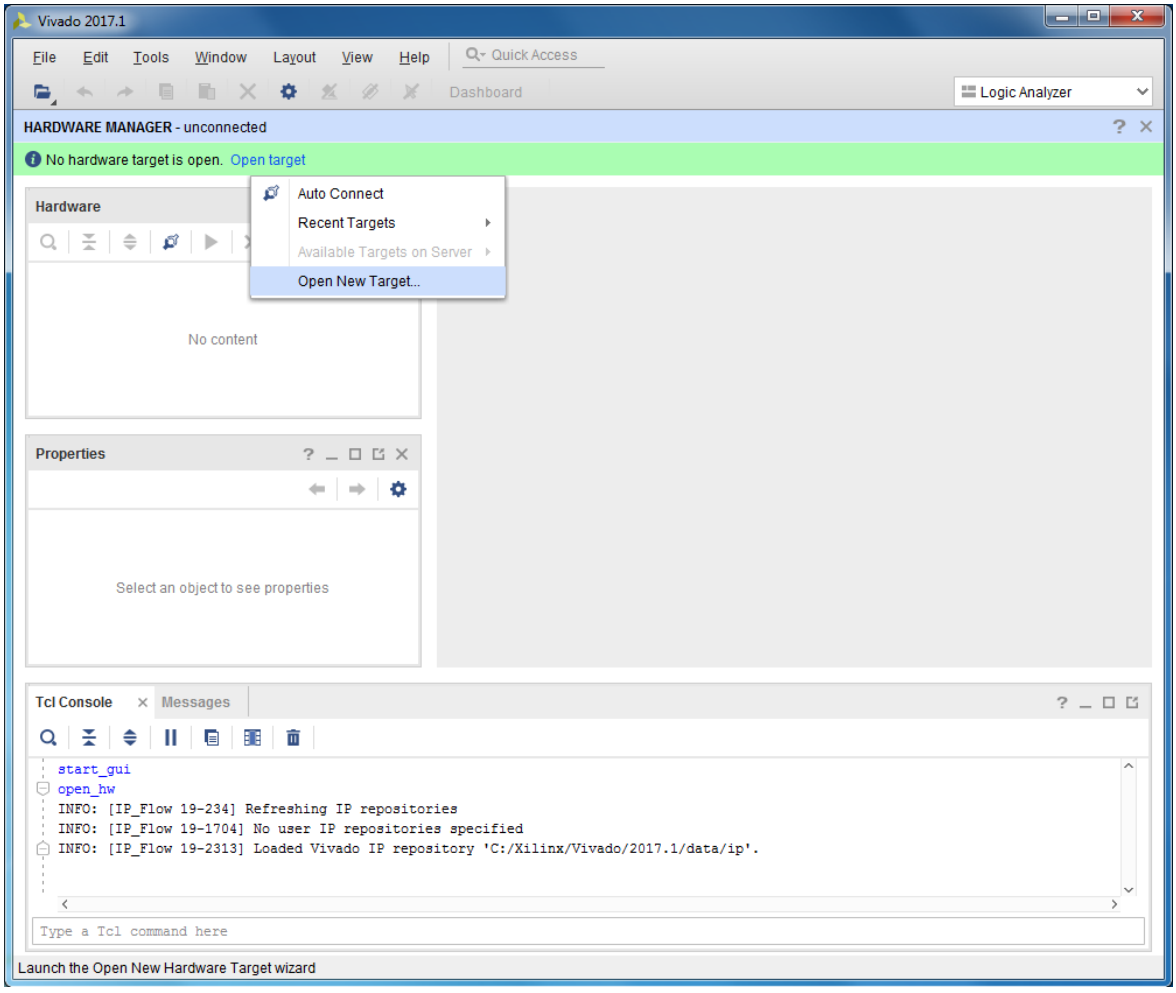

Figure 13: **Hardware Manager**

6. Configure the wizard to establish a connection with the KCU105 board by selecting the default value on each wizard page. Click **Next > Next > Next > Finish**.
7. In the hardware view, right-click **xcku040** and click **Program Device** as shown in Figure 14.

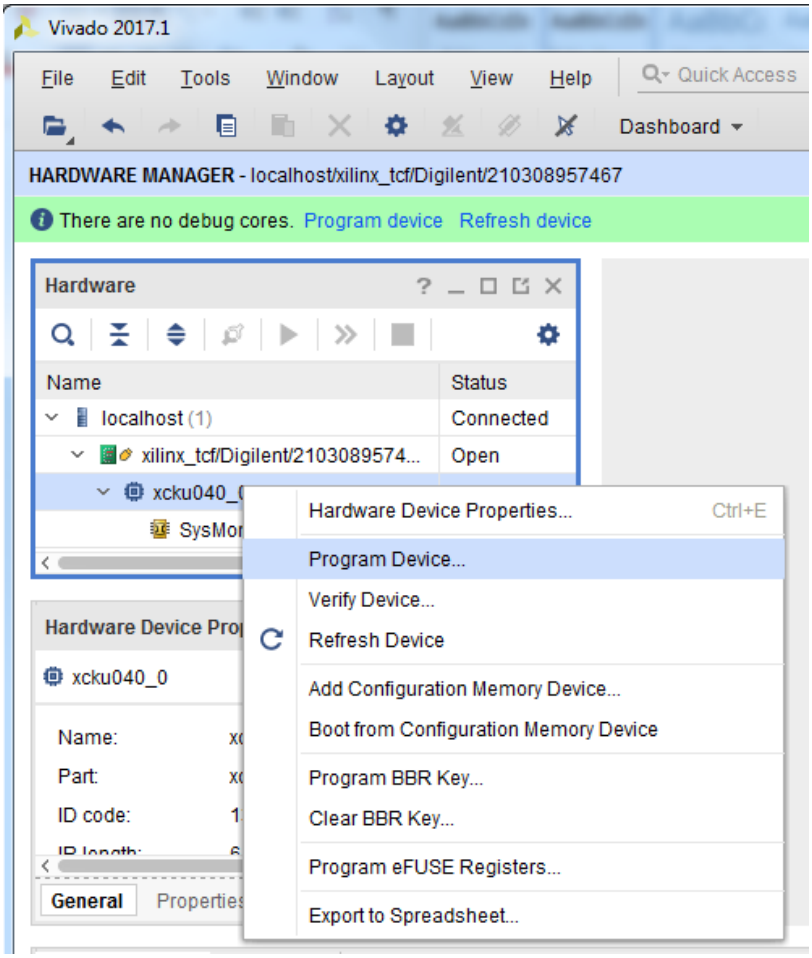

Figure 14: **Select Device to Program**

8. Browse to the location of the `top.bit` and `debug_nets.ltx` files and click **`Program`** as shown in Figure 15.

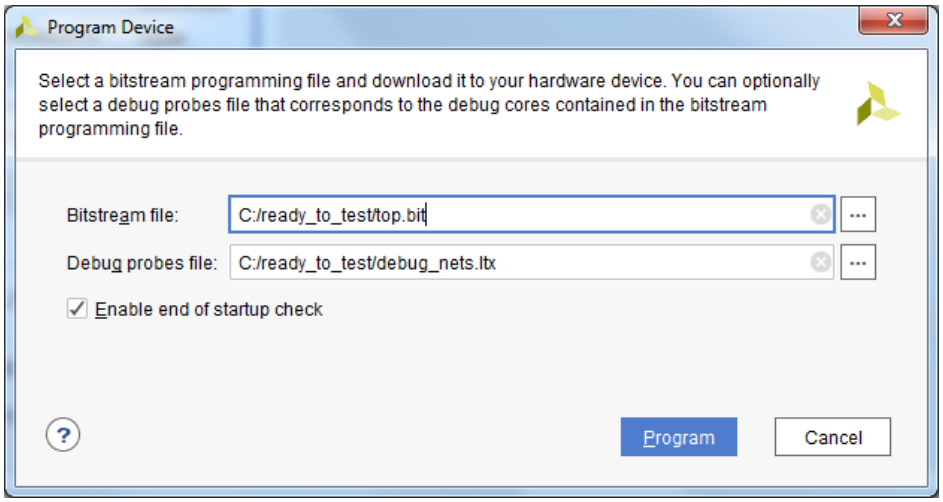

Figure 15: **Program Device Window**

The ILA and VIO debug cores are used in this reference design to test the design on the board. After the programming is completed, the ILA and VIO tabs are added to the Hardware Manager window as shown in Figure 16.

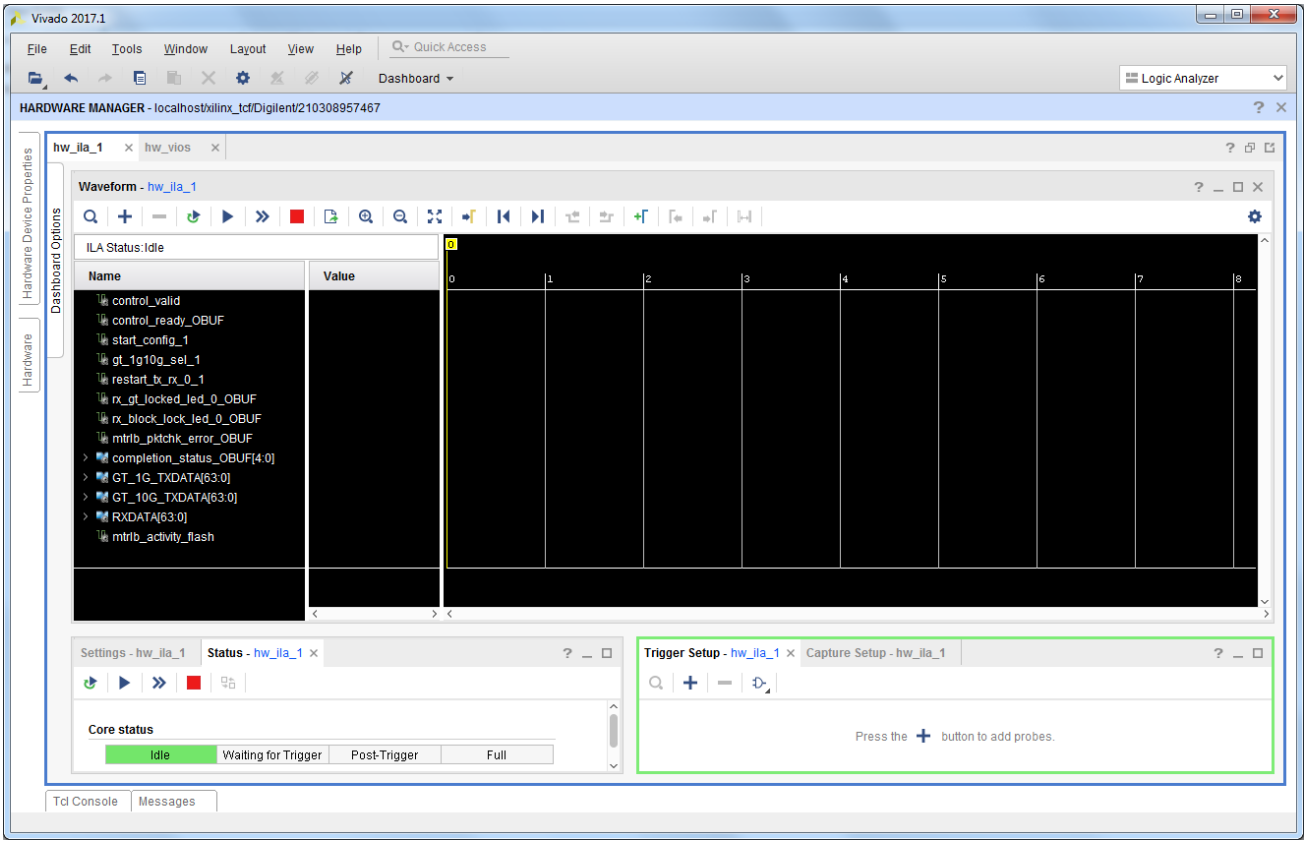

Figure 16: **Hardware Manager with ILA and VIO**

1G Testing

1. Add all available signals in the VIO window using the + symbol and configure as a toggle button as shown in Figure 17.

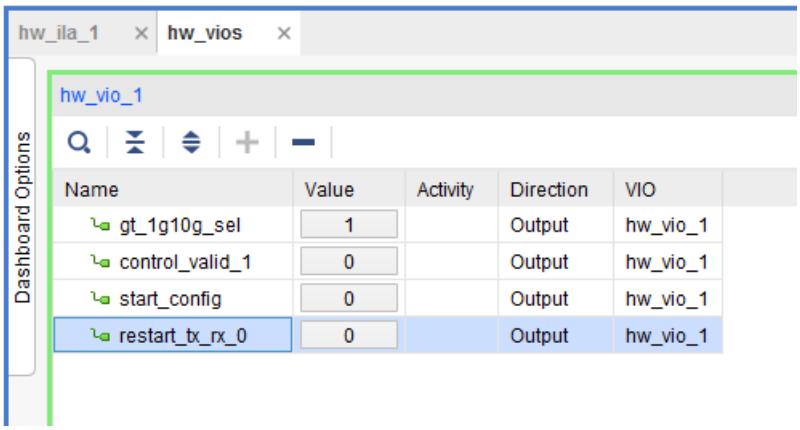

Figure 17: **1G - VIO Window**

2. Set the `gt_1g10g_sel` signal to 1 in VIO windows.
3. Toggle the `control_valid_1` signal (0 -> 1 -> 0).
4. Set the `start_config` signal to 1.
5. Click the **Run** trigger for this ILA core button in the ILA tab. The ILA waveform window is displayed as shown in Figure 18.

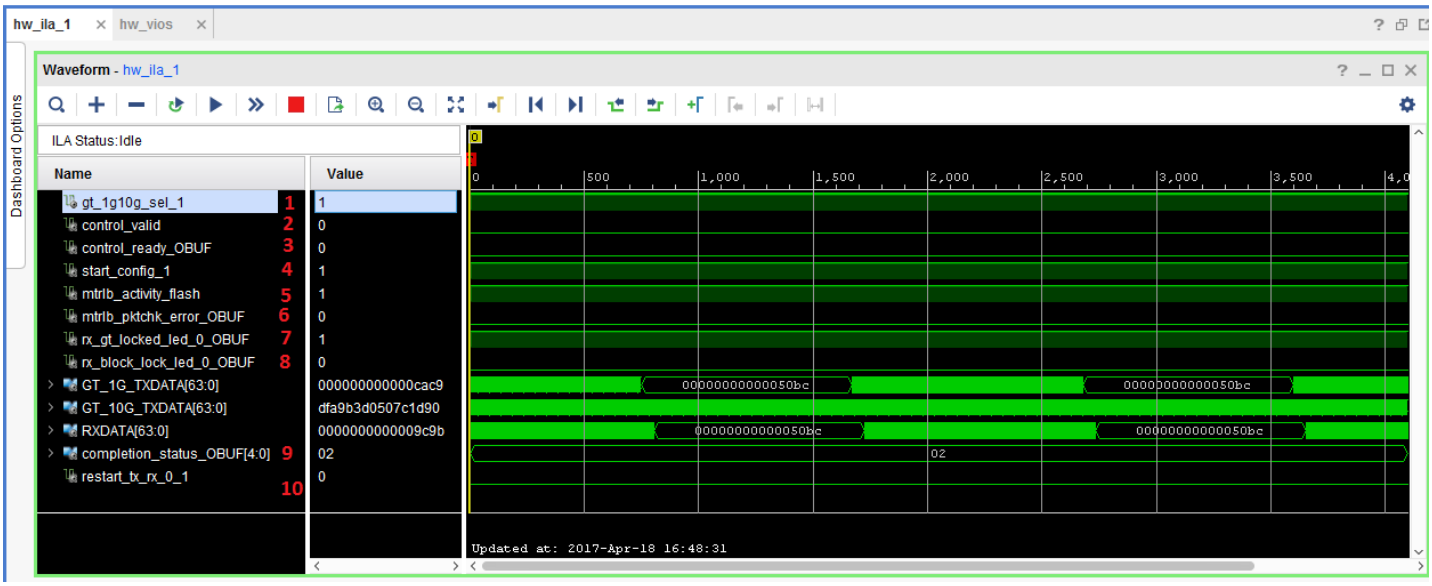

Figure 18: **1G - ILA Window**

6. Observe `rx_gt_locked_led_0` in ILA (see #7 in Figure 18). The value 1 indicates that the GT has been locked.
7. Observe `mtrlb_activity_flash` in ILA (see #5 in Figure 18). This signal toggles, which indicates that the pattern checker is receiving frames.

8. Observe `mtrlb_pktchk_error` in ILA (see #6 in Figure 18). If the value is 1, this indicates that the pattern checker has received an error packet.

10G Testing

1. Set the `gt_1g10g_sel` to 0 as shown in Figure 19.

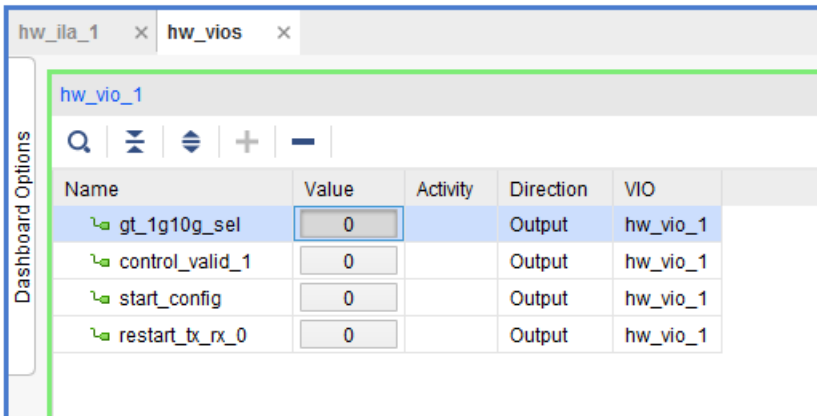

Figure 19: **10G - VIO Window**

2. Click the **Run trigger for this ILA core** icon in the ILA tab. The ILA waveform window is displayed as shown in Figure 20.

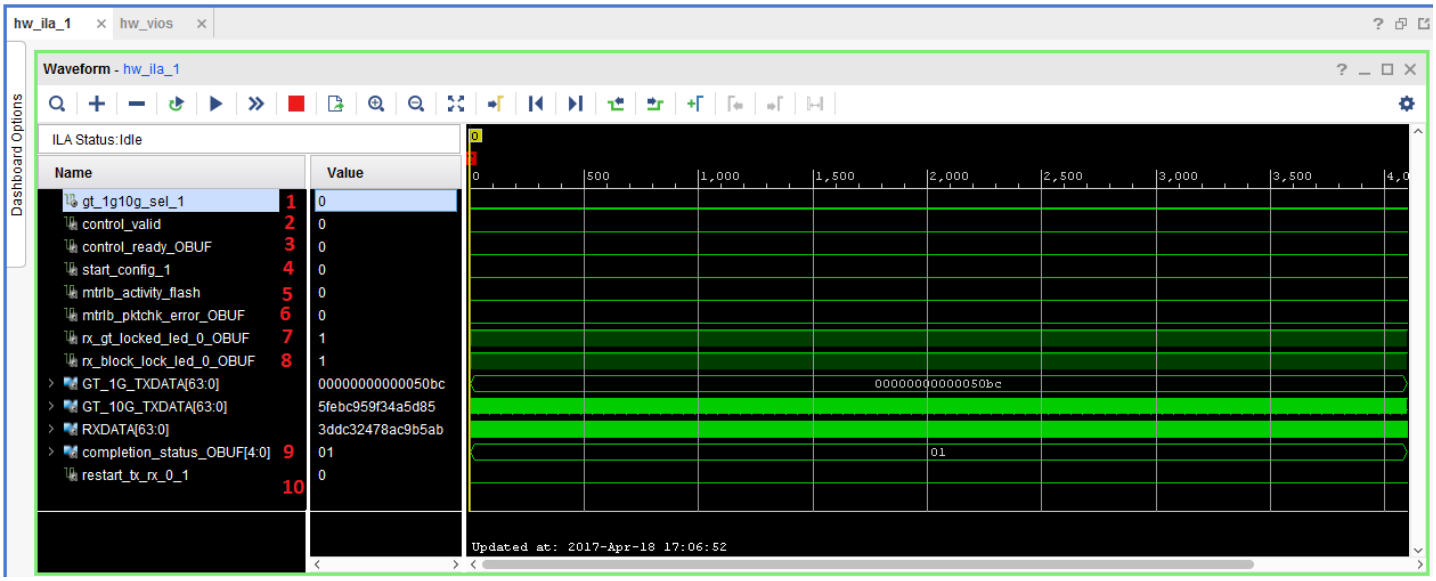

Figure 20: **10G - ILA Window**

3. Observe the `rx_gt_locked_led_0` in ILA (see #7 in Figure 20). The value 1 indicates that the GT has been locked.
4. Observe the `rx_block_lock_led_0` in ILA (see #8 in Figure 20). The value 1 indicates that the RX block lock has been achieved.
5. Observe the `completion_status` in ILA (see #9 in Figure 20). This signal represents the test status/result.
6. Toggle the `restart_tx_rx_0` (0 -> 1 -> 0) in VIO for restarting the test.

Note: Refer to the example design section of *AXI 1G/2.5G Ethernet Subsystem Product Guide* (PG138)[Ref 1] and *10G/25G High Speed Ethernet Subsystem Product Guide*(PG210)[Ref 4] and test bench in the design folder (Simulation\hardware\sources\testbench) to understand the test flow and signal status.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

1. *AXI 1G/2.5G Ethernet Subsystem Product Guide* (PG138)
2. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
3. *1G/2.5G Ethernet PCS/PMA or SGMII LogiCORE IP Product Guide* (PG047)
4. *10G/25G High Speed Ethernet Subsystem Product Guide* (PG210)
5. *10G Ethernet MAC LogiCORE IP Product Guide* (PG072)
6. *10G Ethernet PCS/PMA LogiCORE IP Product Guide* (PG068)
7. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
8. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
9. *Xilinx AXI Reference Guide* (UG761)
10. *VCU118 System Controller – GUI Tutorial* (XTP447)
11. *VCU108 Software Install and Board Setup* (XTP368)
12. *VCU118 Software Install and Board Setup* (XTP449)

13. *IEEE Standard 802.3-2005* (standards.ieee.org/getieee802)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/23/2017	1.0.1	Updated Author details
05/30/2017	1.0	Initial Xilinx release

Please Read: Important Legal Notices