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10G to 40G Ethernet Dynamic Switching Using AMD High-Speed Serial I/O Solution

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Summary

This application note targets Ethernet designs that require dynamic switching between 10 Gb/s and 40 Gb/s using high-speed serial I/O links. The reference design uses the AMD Ethernet solution suite along with an AMD GTH transceiver to set up the Ethernet interface. The transceiver used to interface with the 10G Ethernet physical coding sublayer/physical medium attachment (PCS/PMA) core is also used for one of the four transceivers required for the 40G Ethernet PCS/PMA IP core. The rate switching is handled using the dynamic reconfiguration port (DRP) of the transceiver.

Download the reference design files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design.

Reference Design

The reference design is based on these AMD Ethernet IP cores, which support 10 GbE and 40 GbE:

- 10G/25G High Speed Ethernet Subsystem
- 40G/50G High Speed Ethernet Subsystem

For more information on these IP cores, see the *10G/25G High Speed Ethernet Subsystem Product Guide v2.1* (PG210) [Ref 1] or the *40G/50G High Speed Ethernet Subsystem Product Guide v2.1* (PG211) [Ref 2].

The two interfaces are alternatives to each other, which means that the 10 GbE reuses one of the four SerDes used in the 40 GbE interface. The interface supports 1x 10 GbE, one lane at 10.3125 Gb/s and 1x 40 GbE, and four lanes at 10.3125 Gb/s. When working at 10 Gb/s, the unused transceivers are in power down to limit the power consumption. The active interface can be selected at any time by driving a single bit port. The complexity associated with change in real time is handled by the IP. All customization is in the transceiver wrappers and not in the IP cores generated from the IP catalog. Consequently, it is easy to port the entire IP to a different version of the tools. The switchable IP is simulated and tested for the Vivado™ design suite 2017.3 for the UltraScale™ and UltraScale+™ devices.

Download the reference design files for this application note from the Xilinx website. The checklist in Table 1 shows the reference design matrix.

Table 1: **Reference Design Matrix**

Parameter	Description
General	
Developer name	AMD
Target devices	UltraScale and UltraScale+ devices
Source code provided	Yes
Source code format	Verilog
Design uses code and IP from existing application note and reference designs or third party	10G/25G High Speed Ethernet Subsystem v2.1 40G/50G High Speed Ethernet Subsystem v2.1
Simulation	
Functional simulation performed	Yes
Timing simulation performed	No
Test bench used for functional and timing simulations	Yes
Test bench format	Verilog
Simulator software/version used	Vivado simulator 2017.3
SPICE/IBIS simulations	No
Implementation	
Synthesis software tools/versions used	Vivado synthesis 2017.3
Implementation software tools/versions used	Vivado implementation 2017.3
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	KCU105 and ZCU102 evaluation boards

Hardware Architecture

Figure 1 shows the high-level detail of the reference design.

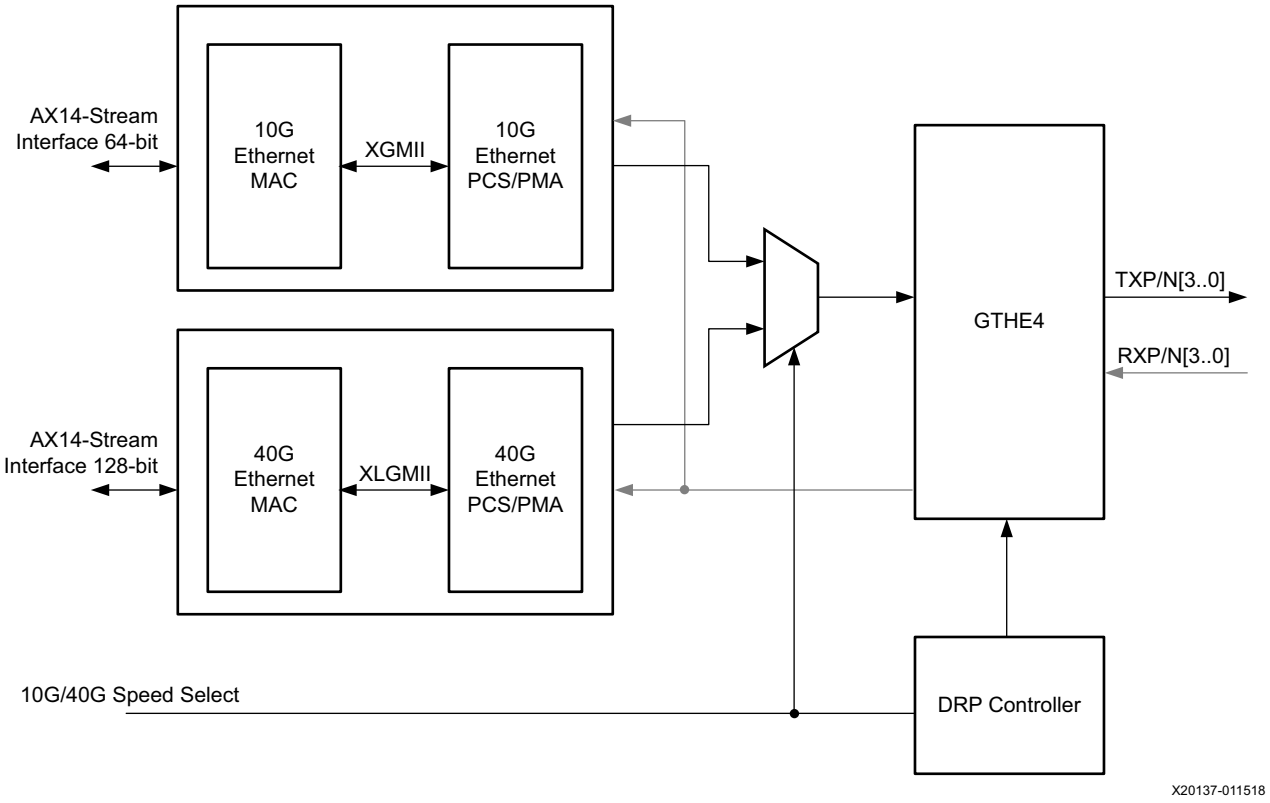

Figure 1: **Hardware Block Diagram**

The transceivers are extracted from the 10 GbE and 40 GbE IP cores to have a common PHY shared with the two cores. The logic for managing the clock, reset, and startup of the transceivers supports this structure.

The Ethernet cores are independent and the transmitter side is selectable via a 2:1 multiplexer. To support the correct rate, some attributes of the transceivers must be modified. This operation is managed by the DRP controller. The 2:1 multiplexer and the DRP controller use a common signal, driven by the user, to select the active Ethernet core and dynamically reconfigure the transceivers. The values of the attributes are defined by the design and stored in the DRP controller.

Clocking and Reset

The clocking architecture is not the same for the 10G and 40G because the datapath width of the two IP cores is different. The receiver and transmitter datapath width of the 10 GbE core is 64 bits and, consequently, the core frequency is 156.25 MHz (see Figure 2).

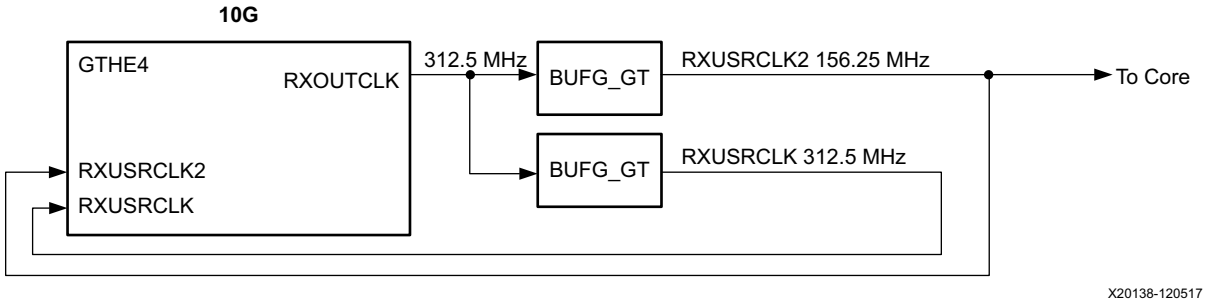

Figure 2: **10 GbE Clock Architecture**

The receiver and transmitter datapath of the 40 GbE core is 32 bits for the single transceiver, and, consequently, the core frequency is 312.5 MHz (see Figure 3).

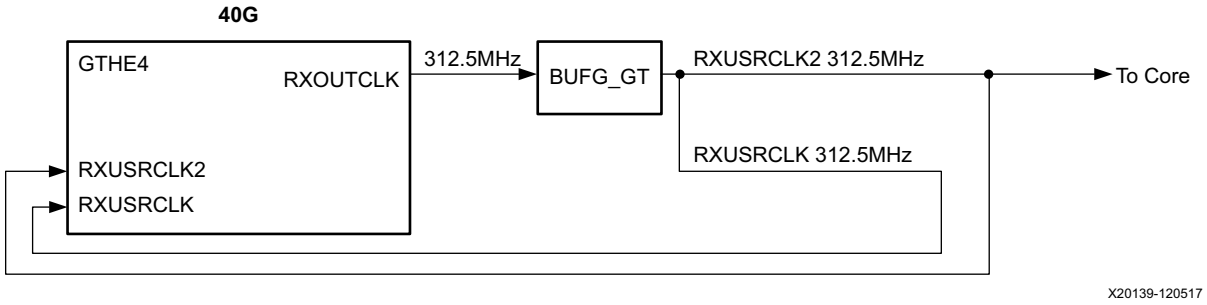

Figure 3: **40 GbE Clock Architecture**

To support both clocking structures, the architecture has been modified by using the BUFG_GT functionality to dynamically change the divider as shown in Figure 4. These details are true for both the transmitter and the receiver side.

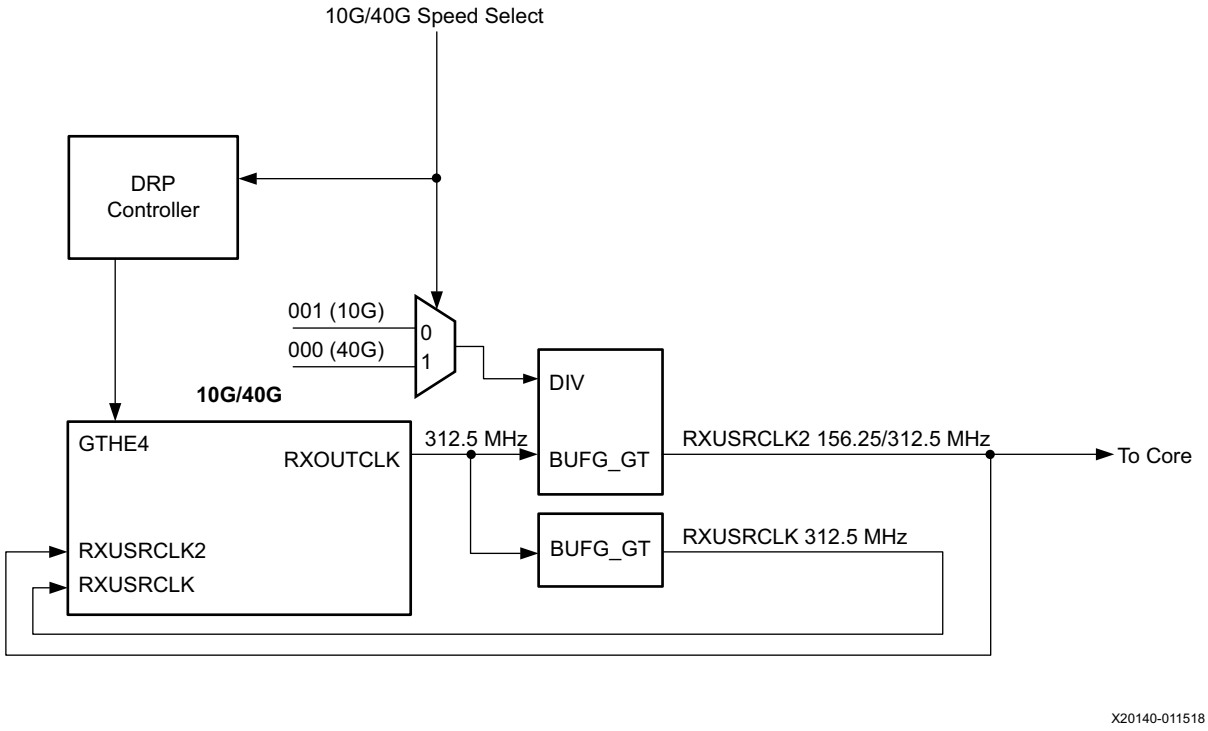

Figure 4: **New Clocking Architecture**

The two IP cores share the same Quad phased-lock loop (QPLL) in the same Quad. For this reason, the code has been modified to have a single common cell. The reset architecture is completely independent, so each IP has its original dedicated logic.

Datapath

The user datapath width of the GTHE channel for 10G Ethernet is configured as 64 bits, and the user data width for 40G Ethernet is configured as 32 bits x4 channels = 128 bits. The datapath has been modified to support both widths. See Figure 5 for datapath connection details.

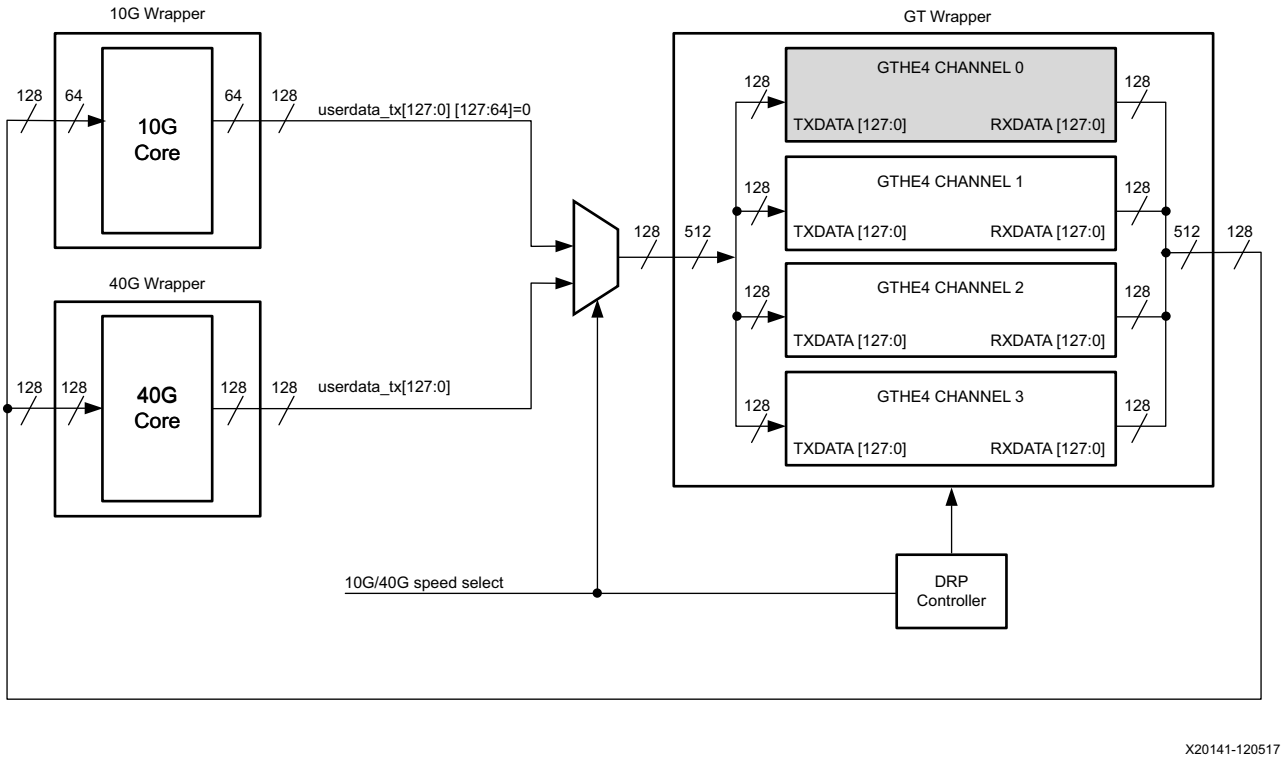

Figure 5: **Datapath**

The GTHE channel 0 is the transceiver shared between 10 GbE and 40 GbE. Due to the different data width, some attributes of this transceiver must be configured accordingly to the selected Ethernet core. The configuration is managed through a DRP controller. The DRP controller is the block that automatically reconfigures the transceiver every time the speed selector is asserted low (10G) or high (40G). The default configuration during start up is 40G.

Wrapper Interface

The reference design `top.v` can be instantiated directly in a customer design or it can be tested on the KCU105 and ZCU102 evaluation boards with the test bench top_test. The ports in the 10G and 40G cores are connected to the wrapper top_inst (`top.v`). These ports follow the selected configuration of the IP cores. Top_inst is instantiated in top_test connected to the test and debug logic for functional simulation and test in hardware (see Figure 6).

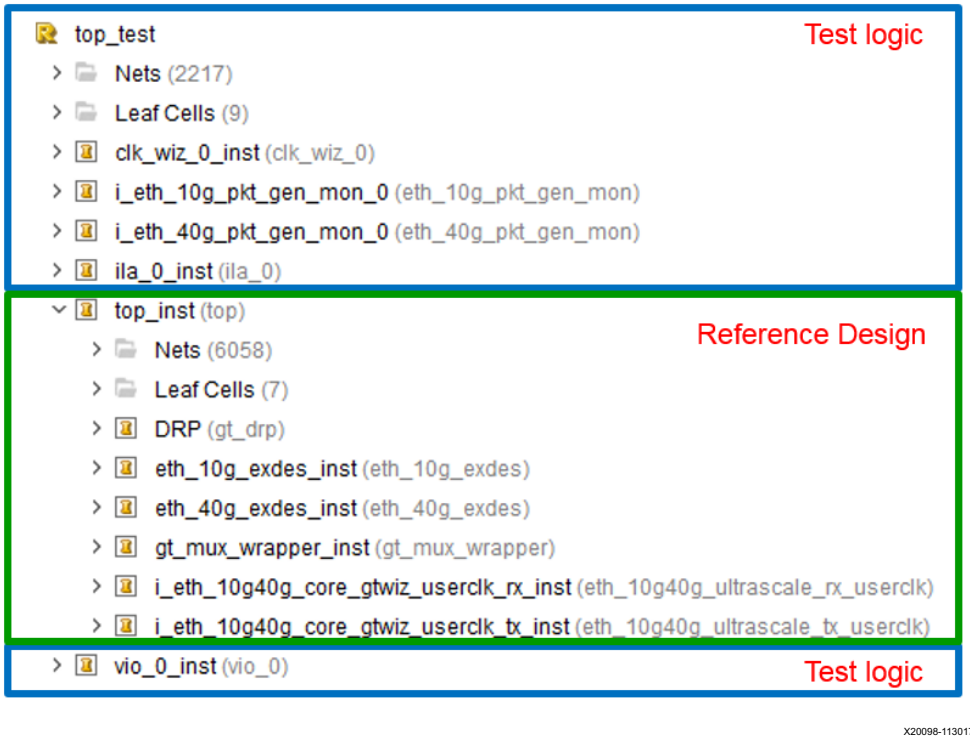

Figure 6: **Reference Design Structure**

The ports are available in the module `top.v` organized as two groups called // 10G PORTS and // 40G PORTS. See the *10G/25G High Speed Ethernet Subsystem Product Guide v2.1* (PG210) [Ref 1] or the *40G/50G High Speed Ethernet Subsystem Product Guide v2.1* (PG211) [Ref 2] for the description and usage of the ports in `top.v`.

General purpose I/Os in the top-level `top_test.v` are provided to control the reference design. The user input and user output ports in the top-level `top_test.v` are listed in Table 2.

Table 2: **Port List in `top_test.v`**

Name	Size	Direction	Description
sys_rst	1	Input	Global system reset
gt_refclk_p	1	Input	Differential input clk to transceiver, 156.25 MHz
gt_refclk_n	1	Input	Differential input clk to transceiver, 156.25 MHz
gt_rxp_in_0	1	Input	Differential serial transceiver receiver input for lane 0
gt_rxn_in_0	1	Input	Differential serial transceiver receiver input for lane 0
gt_txp_out_0	1	Output	Differential serial transceiver transmitter output for lane 0
gt_txn_out_0	1	Output	Differential serial transceiver transmitter output for lane 0
gt_rxp_in_1	1	Input	Differential serial transceiver receiver input for lane 1
gt_rxn_in_1	1	Input	Differential serial transceiver receiver input for lane 1
gt_txp_out_1	1	Output	Differential serial transceiver transmitter output for lane 1
gt_txn_out_1	1	Output	Differential serial transceiver transmitter output for lane 1
gt_rxp_in_2	1	Input	Differential serial transceiver receiver input for lane 2
gt_rxn_in_2	1	Input	Differential serial transceiver receiver input for lane 2
gt_txp_out_2	1	Output	Differential serial transceiver transmitter output for lane 2
gt_txn_out_2	1	Output	Differential serial transceiver transmitter output for lane 2
gt_rxp_in_3	1	Input	Differential serial transceiver receiver input for lane 3
gt_rxn_in_3	1	Input	Differential serial transceiver receiver input for lane 3
gt_txp_out_3	1	Output	Differential serial transceiver transmitter output for lane 3
gt_txn_out_3	1	Output	Differential serial transceiver transmitter output for lane 3
gt_10g40g_sel	1	Input	10G/40G speed select
clk_in_p	1	Input	300 MHz stable/free running input clk
clk_in_n	1	Input	300 MHz stable/free running input clk
restart_tx_rx	1	Input	This signal is used to restart the packet generation and reception for the data sanity test when the packet generator and the packet monitor are in idle state
rx_gt_locked_led_10G	1	Output	Indicates 10 GbE transceiver lock
rx_block_lock_led _10G	1	Output	Indicates 10 GbE core block lock
rx_gt_locked_led_40G	1	Output	Indicates 40 GbE transceiver lock

Table 2: **Port List in `top_test.v` *(Cont'd)***

Name	Size	Direction	Description
rx_block_lock_led _40G	1	Output	Indicates 40 GbE core block lock
completion_status	5	Output	This signal represents the test status/result: • 5'd0: Test did not run • 5'd1: 10GE/40GE core test successfully completed • 5'd2: No block lock on any lanes • 5'd3: Not all lanes achieved block lock • 5'd4: Some lanes lost block lock after achieving block lock • 5'd5: No lane sync on any lanes • 5'd6: Not all lanes achieved sync • 5'd7: Some lanes lost sync after achieving sync • 5'd8: No alignment status or rx_status was achieved • 5'd9: Loss of alignment status or rx_status after both were achieved • 5'd10: Transmitter timed out • 5'd11: No transmitter data was sent • 5'd12: Number of packets received did not equal the number of packets sent • 5'd13: Total number of bytes received did not equal the total number of bytes sent • 5'd14: A protocol error was detected • 5'd15: Bit errors were detected in the received packets • 5'd31: Test is stuck in reset

For information on the features and architectures of the 10 GbE IP and the 40 GbE IP, see the *10G/25G High Speed Ethernet Subsystem Product Guide v2.1* (PG210) [Ref 1] or the *40G/50G High Speed Ethernet Subsystem Product Guide v2.1* (PG211) [Ref 2].

DRP Controller

The DRP controller block uses the same code delivered with the *1G to 10G Ethernet Dynamic Switching Using Xilinx High Speed Serial I/O Solution Application Note* (XAPP1243) [Ref 3], but customized for this specific case.

The DRP controller is the block that automatically reconfigures the transceiver every time the speed selector is asserted Low (10G) or High (40G). The stable/free running clock is used as the clock for the DRP controller. This clock is also used for all of the logic in the design that needs to access the DRP port of the transceiver. At start-up, all ports are configured as 40G.

The DRP controller implements the finite state machine (FSM) to write attribute values in the corresponding transceiver registers. The FSM is synchronized by a stable clock and is triggered by the multiplexer select line (user input). The attribute values of the transceiver for both 10G and 40G protocols are hard coded and stored as ROM in the DRP controller. The output of the DRP controller is mapped to the transceiver DRP interface. The implemented FSM follows the

standard procedure of writing or reading the DRP registers of the UltraScale device GTH transceiver, as described in the *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 4]. The DRP controller FSM flowchart is shown in Figure 7.

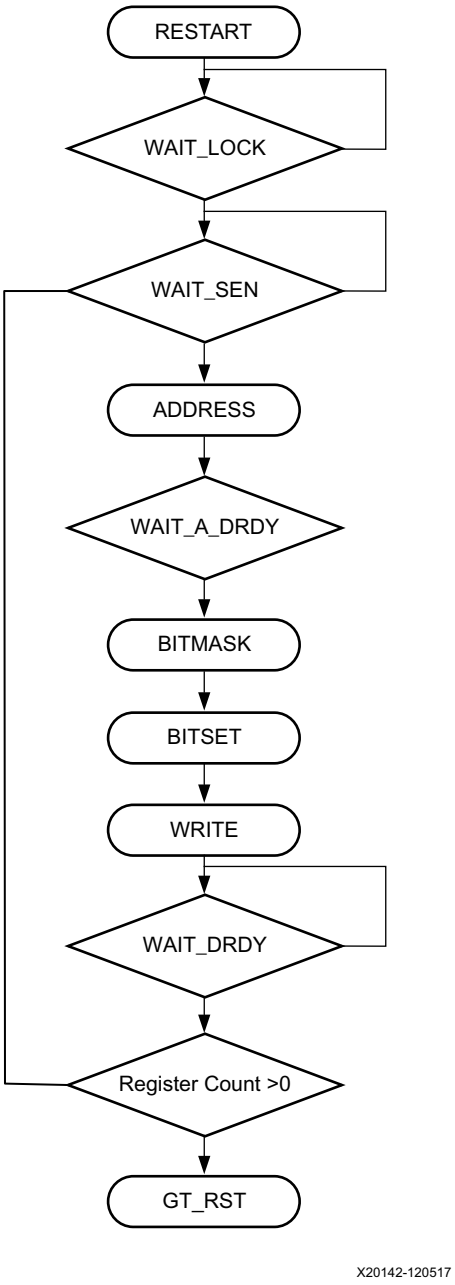

Figure 7: **Design Flow**

See Table 3 for the description of each state shown in Figure 7.

Table 3: **Finite State Machine Description**

State	Description
RESTART	The ROM starting address and the output values are initialized to zero.
WAIT_LOCK	The FSM polls for the channel phased-lock loop (CPLL) lock (for 1G) or the QPLL (for 10G). After the PLL is locked, it moves to the next state.
WAIT SEN	The FSM waits in this state until the multiplexer select line value (user input) is toggled to select the 1G rate option from the previous 10G selection and vice versa. Based on this trigger, the starting address to fetch the attribute values from the ROM is assigned.
ADDRESS	In this state, a read from the transceiver registers is enabled, and the attribute register address is set.
WAIT_A_DRDY	The logic implements a read to verify the write procedure. Consequently, the attribute values are initially read and then altered. This state polls for the ready signal from the transceiver to be asserted.
BITMASK	The portions of bits of the attribute register that are not to be altered are masked in this state.
BITSET	The attribute register bits are set in this state.
WRITE	The new value of the attribute is written to the corresponding register location.
WAIT_DRDY	This state polls for the ready signal from the transceiver to be asserted as an acknowledgment to a successful write.
REGISTER COUNT	In this state, the total number of the attribute registers to be changed is monitored. The FSM moves to the ADDRESS state until the register count becomes zero, indicating that all the registers are written.
GT_RST	The transceiver channel is reset to apply the new attribute values written. The FSM moves to the WAIT LOCK state and subsequently remains in the WAIT_SEN state until another SEN rising pulse is obtained.

Ethernet Core Configuration

Figure 8 through Figure 15 show the options used to generate the two 10G and 40G Ethernet cores.

10G/25G Ethernet Subsystem Configuration

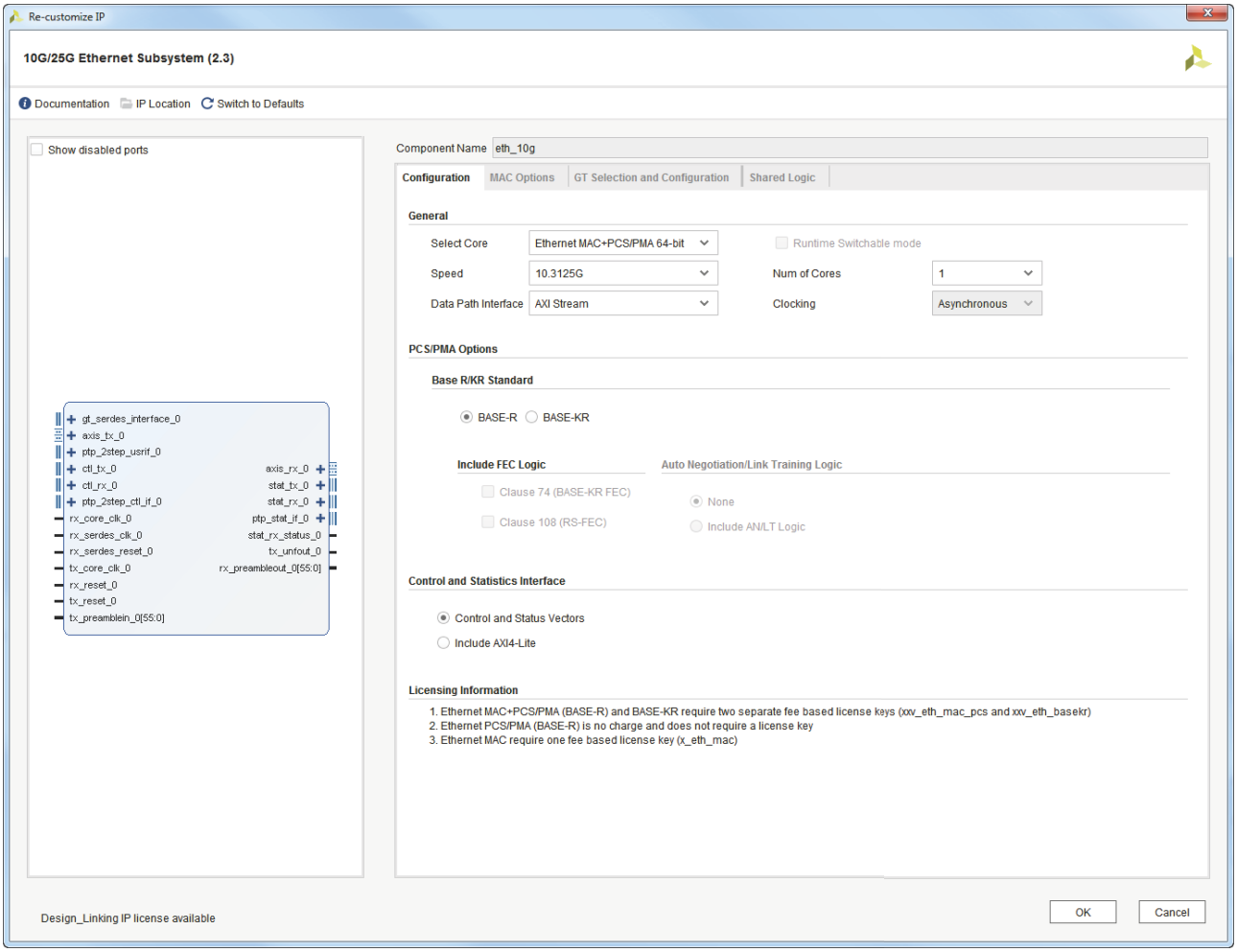

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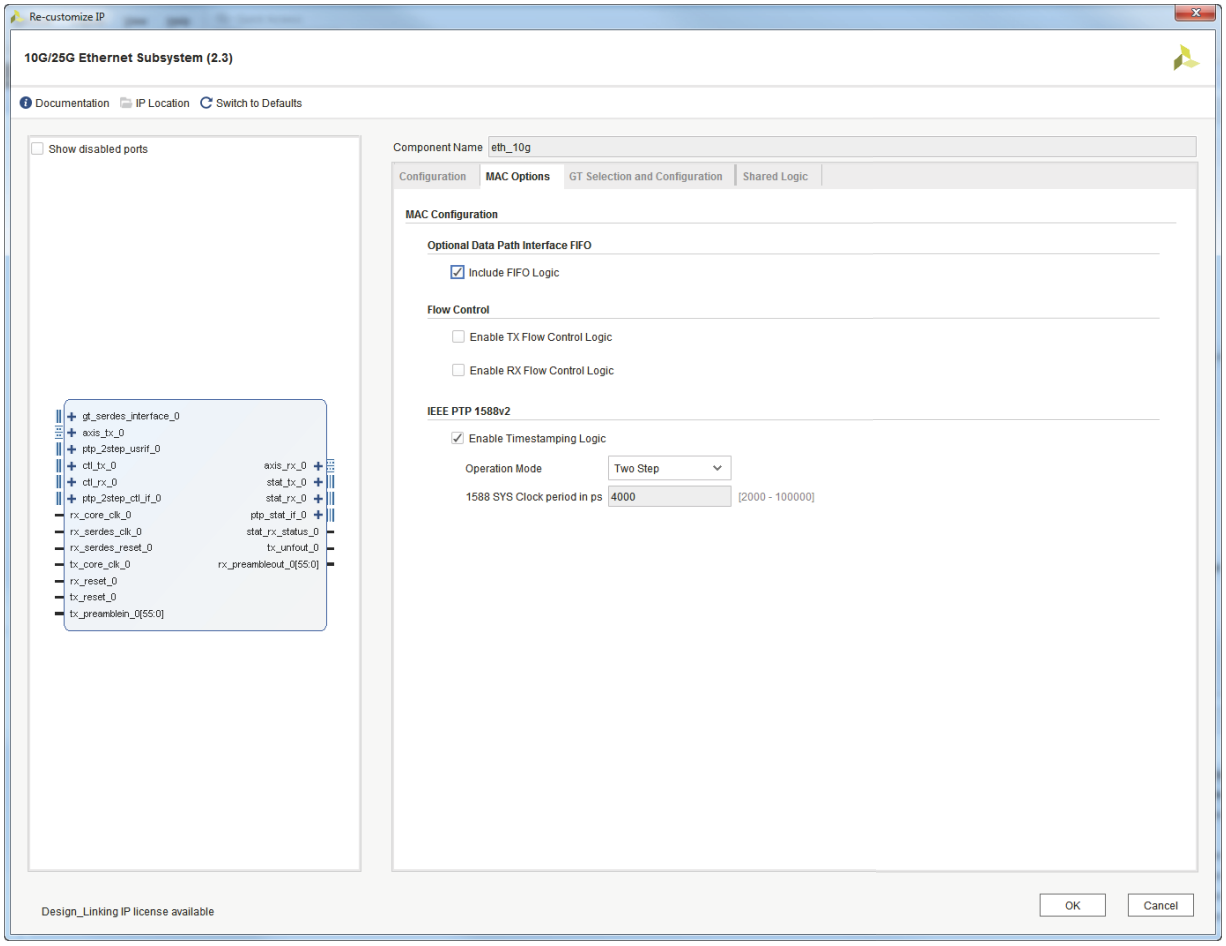
Figure 8: **10G/25G Ethernet Subsystem – Configuration**

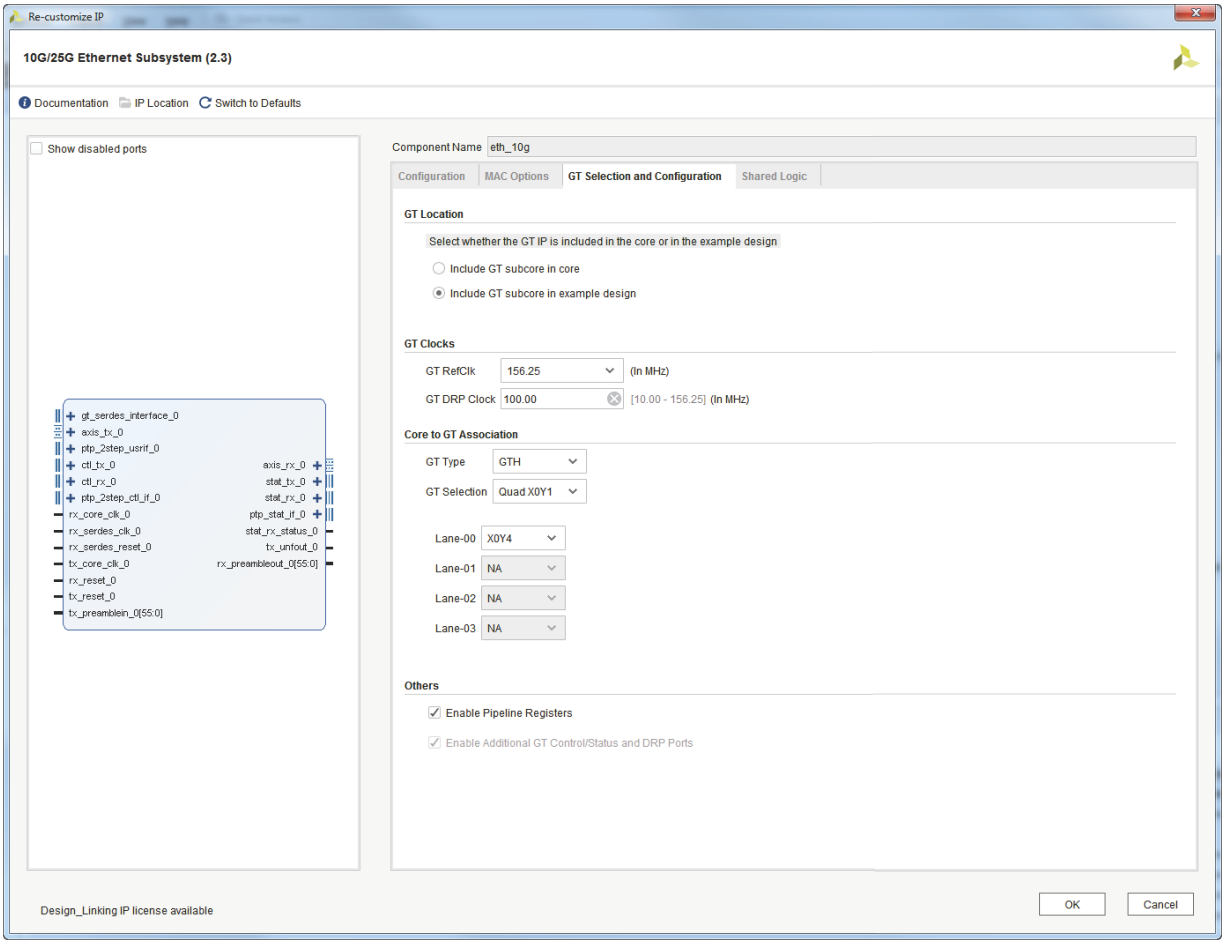
10G/25G Ethernet Subsystem MAC Options



X20105-113017

Figure 9: **10G/25G Ethernet Subsystem – MAC Options**

10G/25G Ethernet Subsystem Transceiver Selection and Configuration



X20110-113017

Figure 10: **10G/25G Ethernet Subsystem – Transceiver Selection and Configuration**

10G/25G Ethernet Subsystem Shared Logic

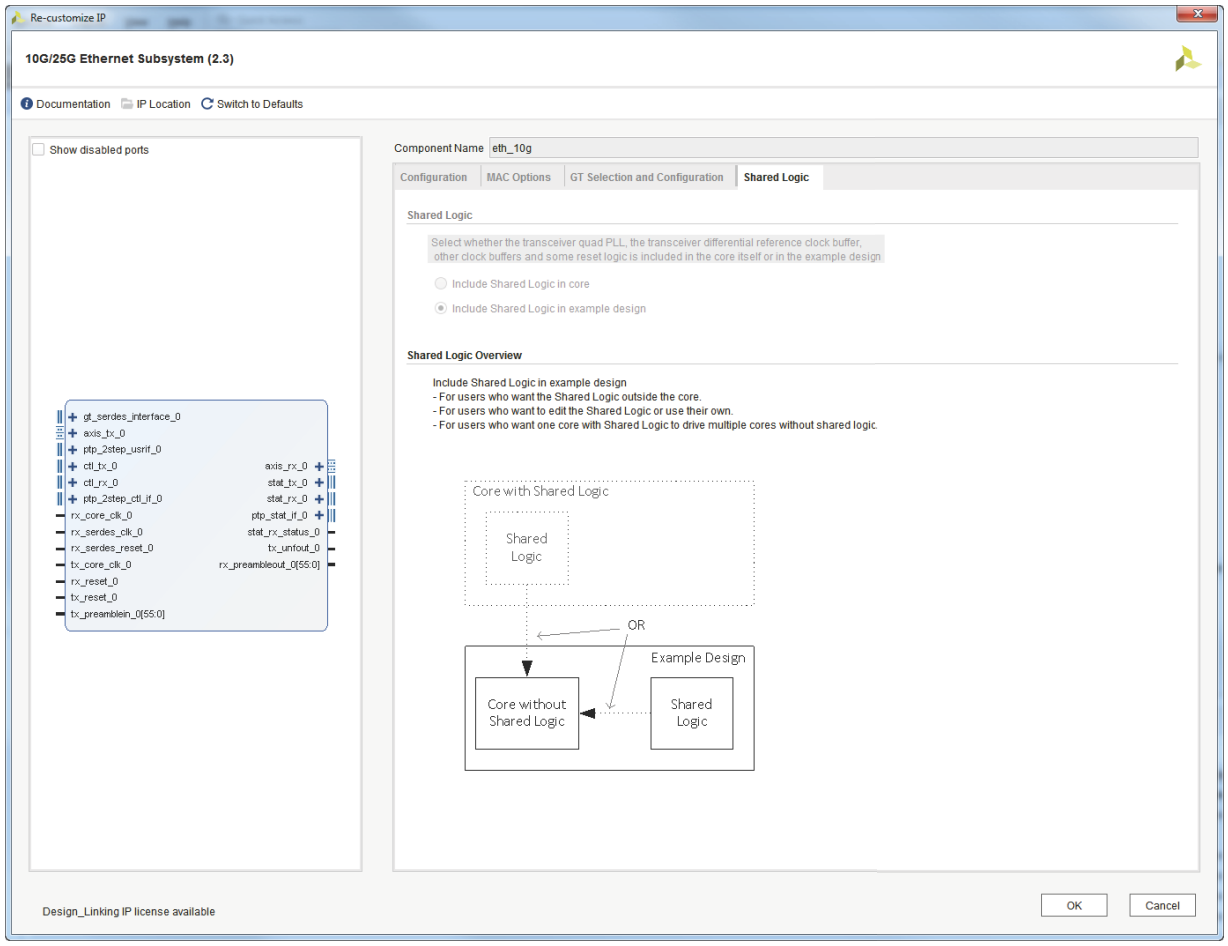


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Figure 11: **10G/25G Ethernet Subsystem – Shared Logic**

40G/50G Ethernet Subsystem Configuration

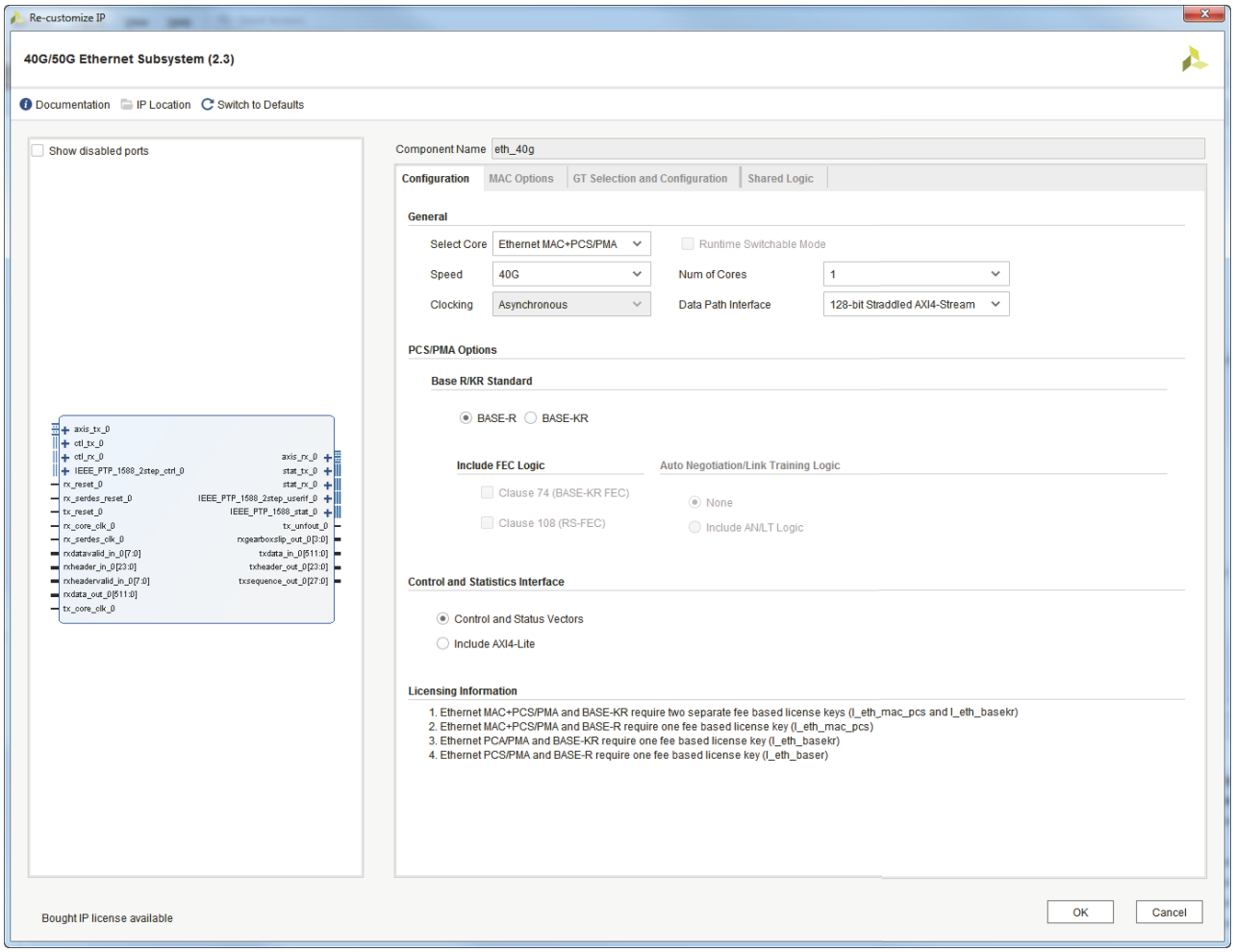

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Figure 12: **40G/50G Ethernet Subsystem – Configuration**

40G/50G Ethernet Subsystem MAC Options

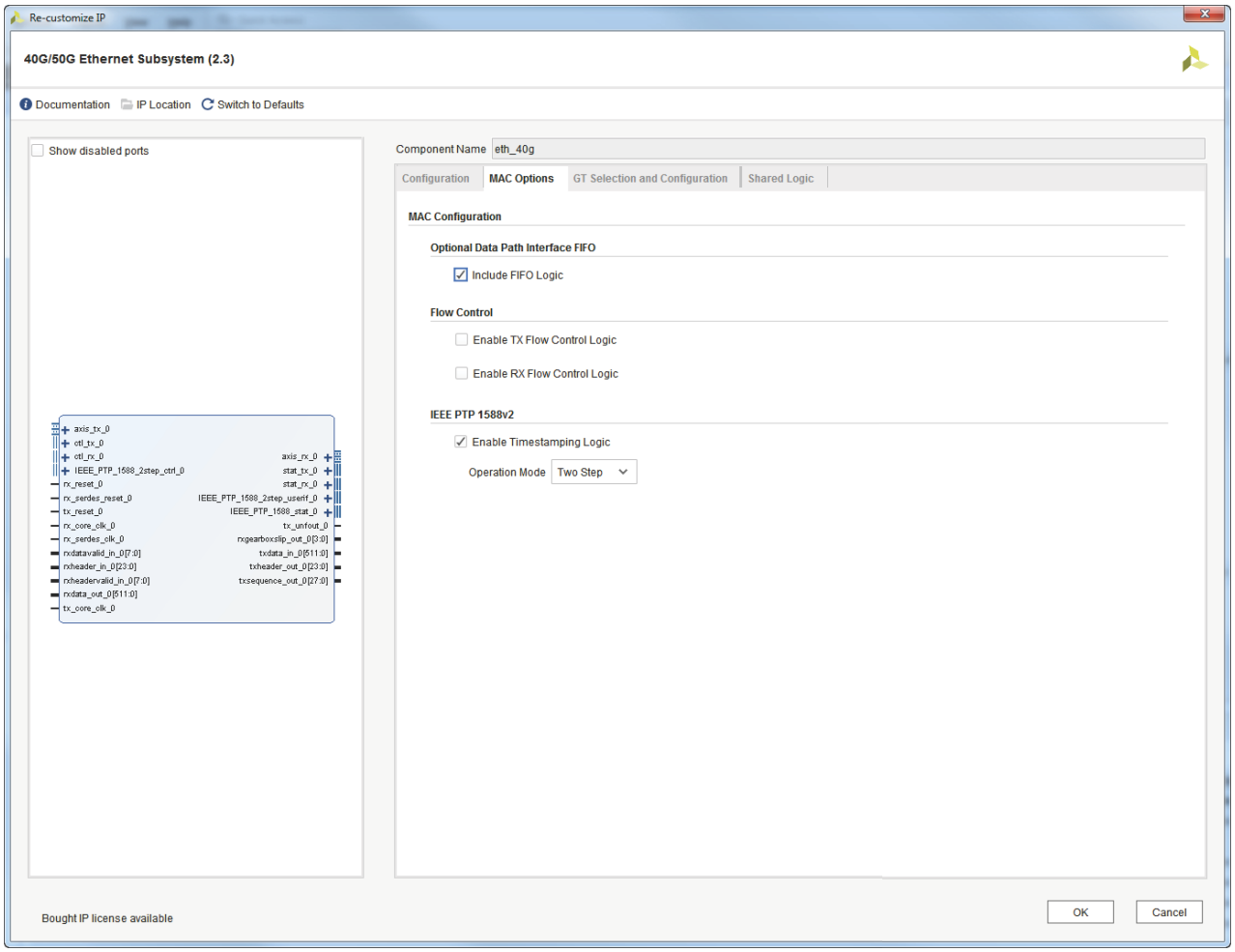

Figure 13: **40G/50G Ethernet Subsystem – MAC Options**

40G/50G Ethernet Subsystem Transceiver Selection and Configuration

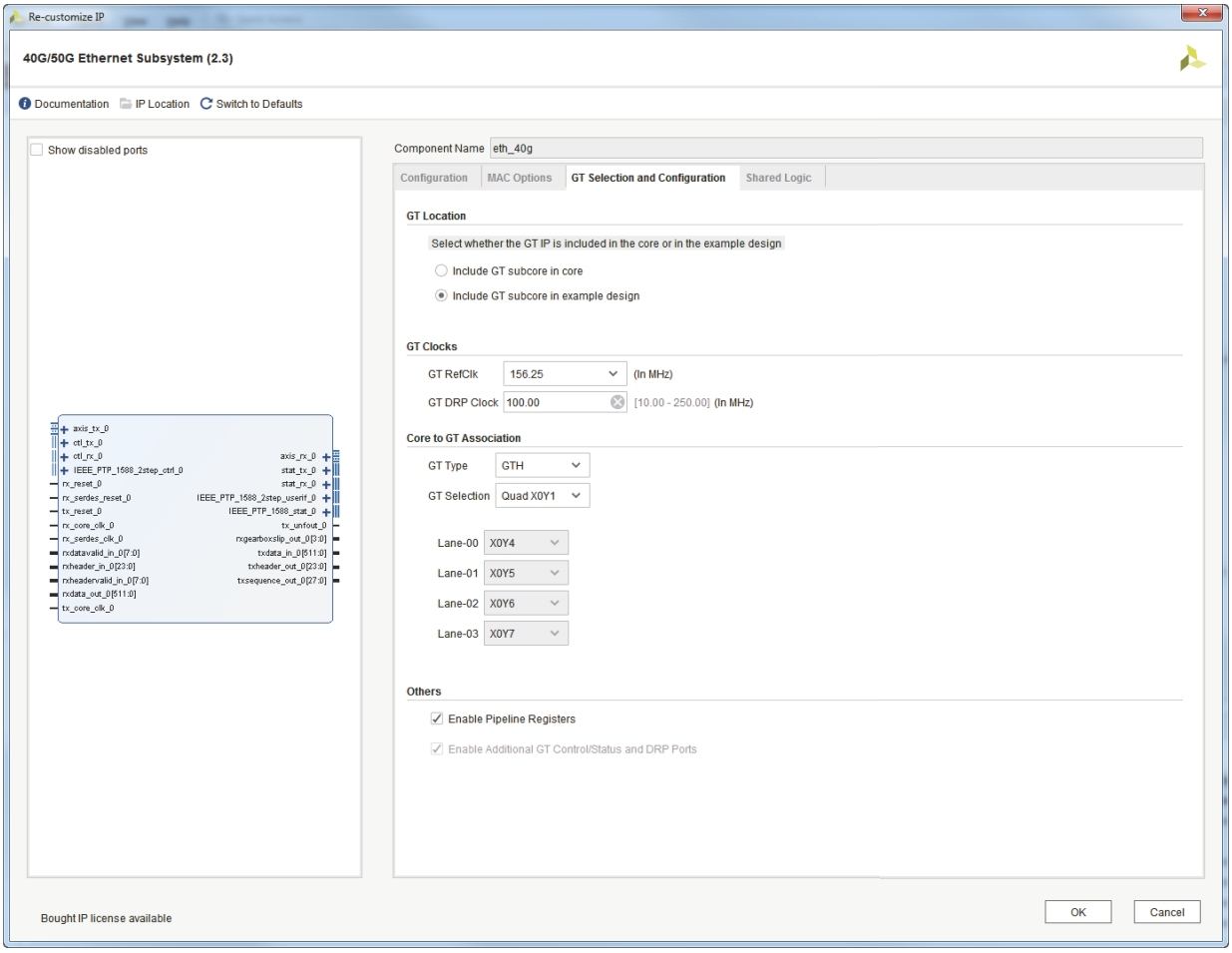

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Figure 14: **40G/50G Ethernet Subsystem – Transceiver Selection and Configuration**

40G/50G Ethernet Subsystem Shared Logic

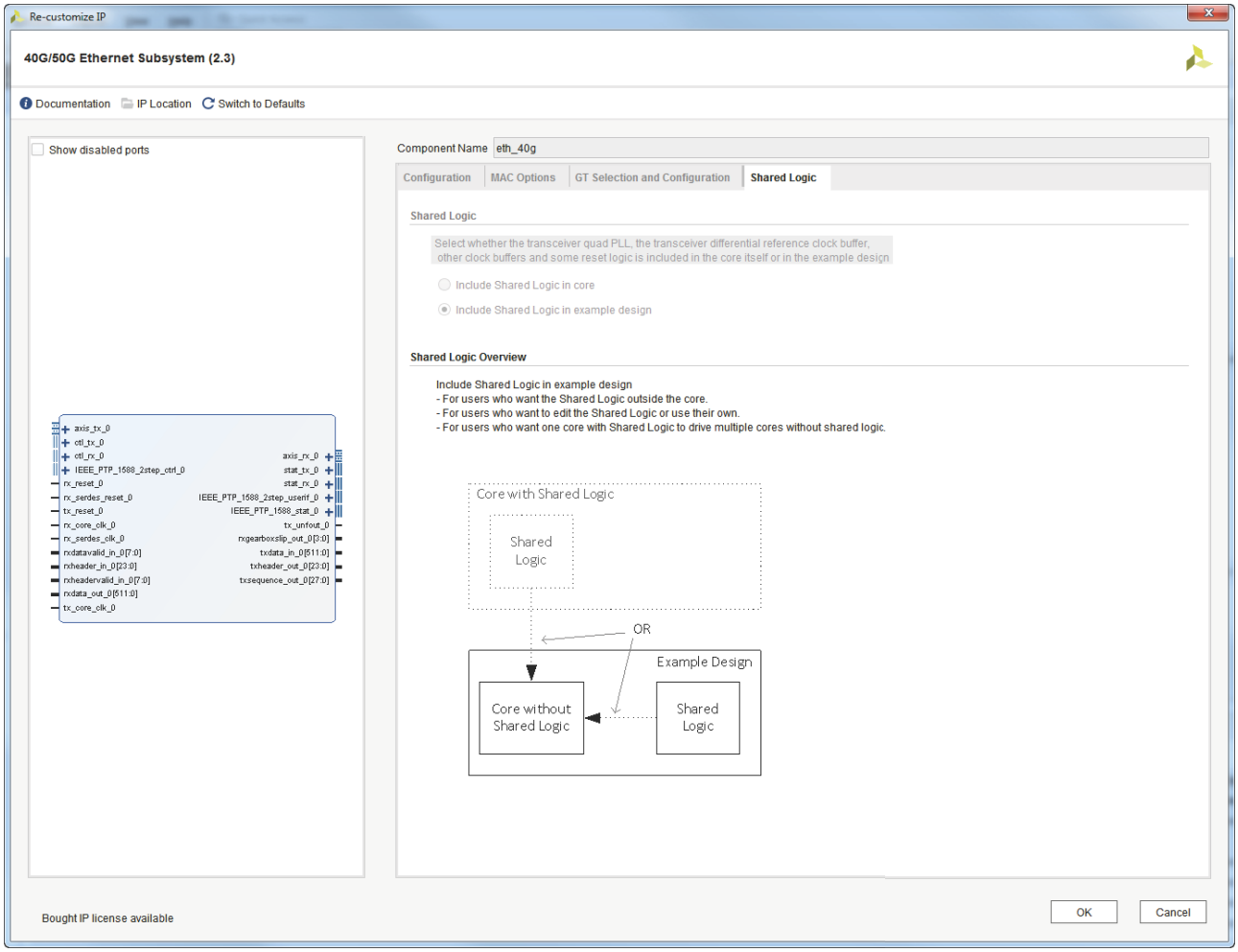

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Figure 15: **40G/50G Ethernet Subsystem – Shared Logic**

Testbench Simulation

The 10G and 40G cores, the switching logic, and the DRP configuration have been validated with a behavioral simulation. A test bench is provided and tested with the Vivado simulator. The test bench starts the simulation for the 40G. After the test is completed, it switches to the 10G test, then again to 40G, and then again to the 10G.

The full simulation log is listed here:

```
Vivado Simulator 2017.3
Time resolution is 1 fs
++++++++++++++++++++++++++++++++++++++++++++++++++++++
++++++++++++++       40G Ethernet       +++++++++++++++
++++++++++++++++++++++++++++++++++++++++++++++++++++++
INFO : SYS_RESET RELEASED TO 40G CORE
INFO : WAITING FOR THE GT LOCK..........
INFO : GT LOCKED
INFO : WAITING FOR RX_ALIGNED..........
INFO : RX ALIGNED
INFO : CORE Version is 2.3
INFO : Sanity Completed and Passed
INFO : CORE TEST SUCCESSFULLY COMPLETED and PASSED
INFO : Test Completed Successfully
++++++++++++++++++++++++++++++++++++++++++++++++++++++
++++++++++++++    40G -> 10G Switching   +++++++++++++++
++++++++++++++++++++++++++++++++++++++++++++++++++++++
INFO : SYS_RESET RELEASED TO 10G CORE
INFO : WAITING FOR THE GT LOCK..........
INFO : GT LOCKED
INFO : WAITING FOR RX_BLOCK_LOCK..........
INFO : CORE 10GE RX BLOCK LOCKED
INFO : WAITING FOR COMPLETION STATUS..........
INFO : COMPLETION_STATUS = 5'b00001
INFO : Sanity Completed and Passed
INFO : CORE TEST SUCCESSFULLY COMPLETED and PASSED
INFO : Test Completed Successfully
++++++++++++++++++++++++++++++++++++++++++++++++++++++
++++++++++++++    10G -> 40G Switching   +++++++++++++++
++++++++++++++++++++++++++++++++++++++++++++++++++++++
INFO : SYS_RESET RELEASED TO 40G CORE
INFO : WAITING FOR THE GT LOCK..........
INFO : GT LOCKED
INFO : WAITING FOR RX_ALIGNED..........
INFO : RX ALIGNED
INFO : CORE Version is 2.3
```

```
INFO : Sanity Completed and Passed
INFO : CORE TEST SUCCESSFULLY COMPLETED and PASSED
INFO : Test Completed Successfully
++++++++++++++++++++++++++++++++++++++++++++++++++++
++++++++++++++    40G -> 10G Switching   +++++++++++++++
++++++++++++++++++++++++++++++++++++++++++++++++++++
INFO : SYS_RESET RELEASED TO 10G CORE
INFO : WAITING FOR THE GT LOCK..........
INFO : GT LOCKED
INFO : WAITING FOR RX_BLOCK_LOCK..........
INFO : CORE 10GE RX BLOCK LOCKED
INFO : WAITING FOR COMPLETION STATUS..........
INFO : COMPLETION_STATUS = 5'b00001
INFO : Sanity Completed and Passed
INFO : CORE TEST SUCCESSFULLY COMPLETED and PASSED
INFO : Test Completed Successfully
Simulation Stopped
```

Figure 16 shows the waveform of the behavioral simulation.

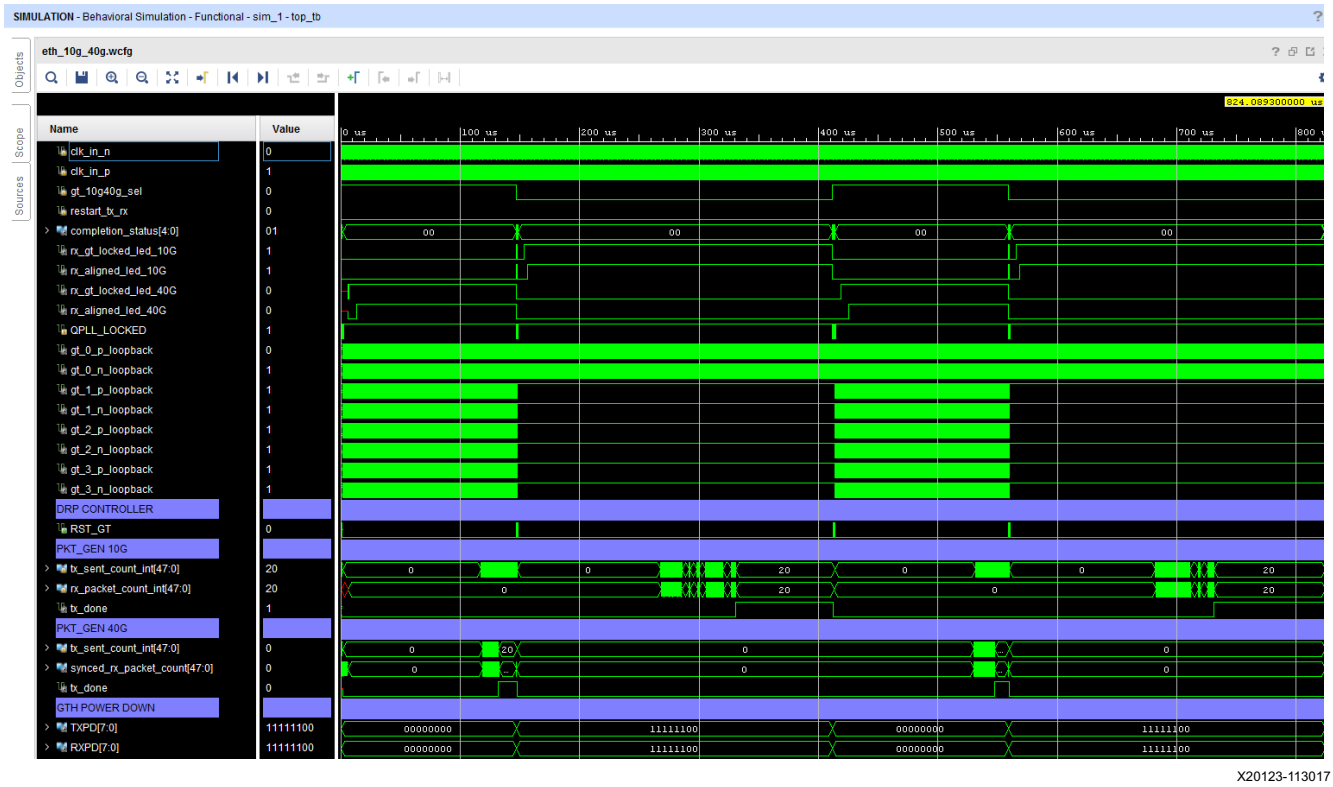

Figure 16: **Waveform Behavioral Simulation**

See Table 4 for a detailed description of all signals shown in Figure 16.

Table 4: **Waveform Signals Description**

Signal	Notes
gt_10g40g_sel	Multiplexer selector, 1 = 40G, 0 = 10G
restart_tx_rx	Restart packet generator test pattern
completion_status	Test results, 1 = test successfully completed
rx_gt_locked_led_10G	When gt_10g40g_sel = 0, transceiver lock when resetdone is asserted
rx_aligned_led_10G	When gt_10g40g_sel = 0, a value of 1 indicates the PCS lane is aligned, the receiver path is aligned and can receive packet data
rx_gt_locked_led_40G	When gt_10g40g_sel = 1, transceiver lock when resetdone is asserted
rx_aligned_led_40G	When gt_10g40g_sel = 1, a value of 1 indicates all PCS lanes are aligned and deskewed, the receiver path is aligned and can receive packet data
qpll_locked	The QPLL of the transceivers is receiving the right clock and is locked
gt_x_x_loopback	Transmitter and receiver ports external loopback
rst_gt	A value of 1 indicates the DRP controller has completed the reconfiguration of the transceivers generating a master reset for the design
tx_sent_count_int	10G/40G packet sent
rx_packet_count_int	10G packet received
synced_rx_packet_count	40G packet received
tx_done	10G/40G end packet sent
txpd	Transmitter power down port, `11` to power down a single transceiver, 40G = `00000000`, 10G = `11111100`
rxpd	Receiver power down port, `11` to power down a single transceiver, 40G = `00000000`, 10G = `11111100`

Reference Design Files

The reference design is for the AMD KCU105 and ZCU702 evaluation boards and the directory structure is the same for both. Figure 17 shows the directory structure for the Kintex™ UltraScale device (KCU105) design files.

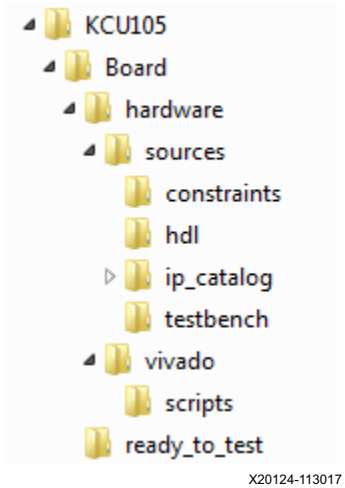

Figure 17: **Directory Structure**

The KCU105 folder contains the hardware design deliverables listed in Table 5.

Table 5: **Hardware Design Deliverables**

Folder Name	Description
Board	Contains all required scripts and a programming file for the board test
Sources/constraints	Contains the I/O and timing constraints file
Sources/hdl	Contains the source code deliverable files
Sources/ip_catalog	Contains the AMD IP cores required for the design
Sources/testbench	Contains the test bench files for simulation
Vivado/scripts	Contains the design creation script for both Windows and Linux operating systems in command line and in Vivado design suite IDE mode
Ready_to_test	Contains programming files to configure the KCU105 evaluation board

The `readme.txt` file provides the details on the folder structure, tool version, and revision.

The pinout defined in the `loc_timing.xdc` file delivered with the design uses the transceivers connected to the FMC1 connector. If needed, it is possible to modify the pinout to change the location of the transceiver ports.

Project Creation

The `kintex_ultrascale_10g_40g.tcl` script for the KCU105 evaluation board or the `zynq_ultrascalep_mpsoc_10g_40g.tcl` script for the ZCU102 evaluation board is used to create the Vivado tools project. The script can be sourced either in a shell configured for the Vivado tools or in the Tcl console available in the GUI (see Figure 18).

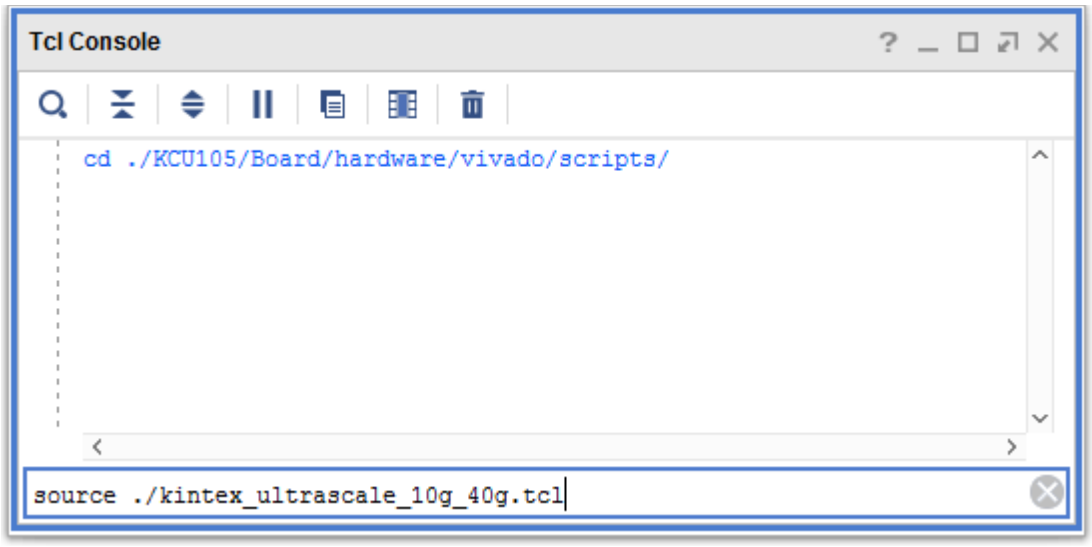

Figure 18: **Tcl Console**

For example, to create the project for the KCU105 evaluation board, from a shell move to the script directory and execute the command:

```
vivado -mode tcl -source kintex_ultrascale_10g_40g.tcl
```

In the GUI, move to the script directory and source `kintex_ultrascale_10g_40g.tcl`. The script creates the project by importing all of the design files needed for design implementation and simulation (see Figure 19).

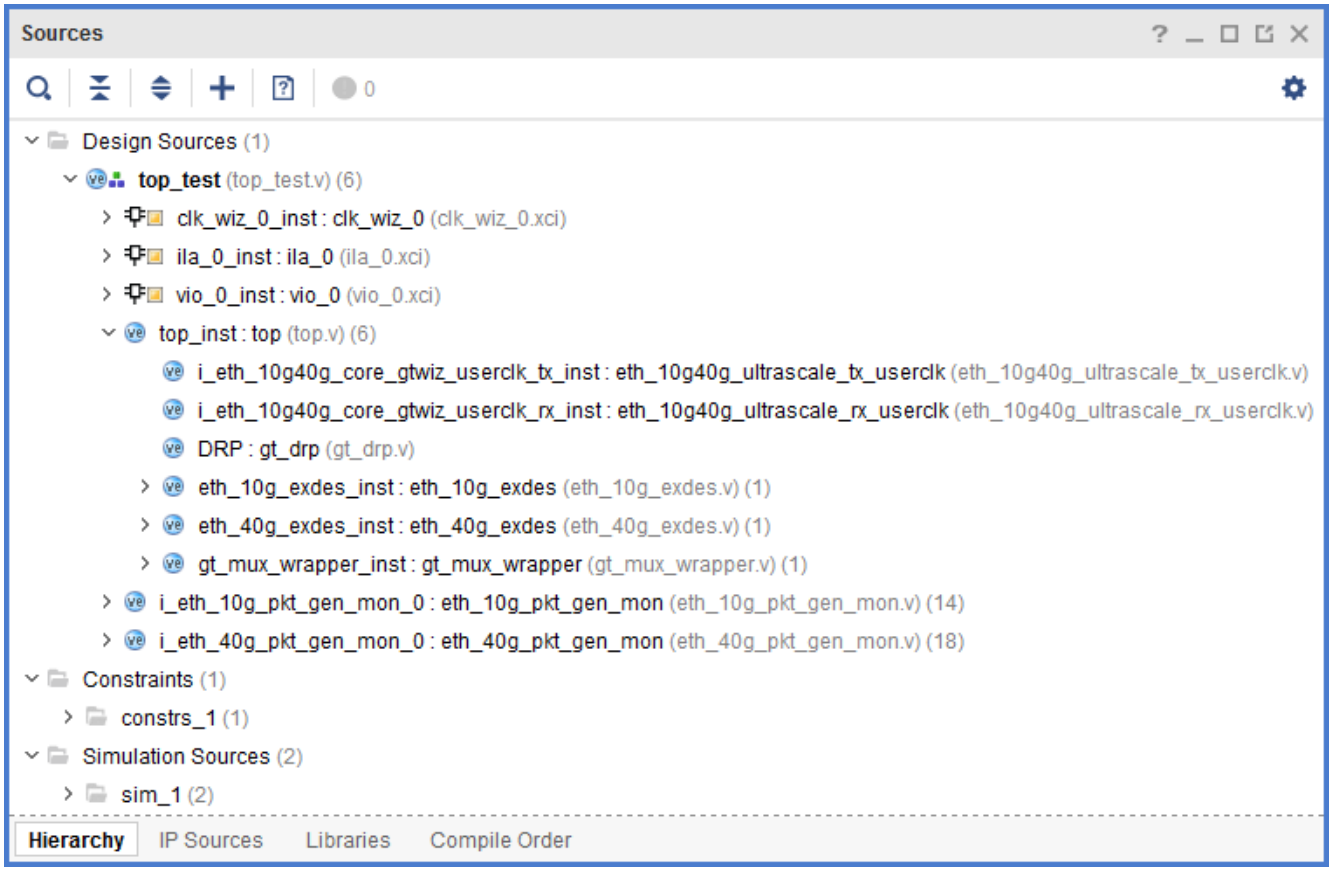

Figure 19: **Design Source Files**

Reference Design Maintenance

This section provides details on how to maintain the reference design for Vivado design suite updates or for new IP versions. The IP cores are generated as "include GT subcore in the example design," which means that all files related to the transceivers are not part of the core. All of the modified files for the reference design are in the transceiver side. When generating the IP, it is structured as two main blocks. For example, the 10G is eth_10g for the core and eth_10g_gt_0 for the transceiver. For each of the two main blocks, the Xilinx core instance (XCI) files are generated. The XCI files store the full IP configuration.

The value of the `IS_MANAGED` property for the `eth_10g_gt_0.xci` in the design is set to false, which means that all of the files that are part of the transceiver are not regenerated. If the IP needs to be updated due to a different option, open `eth_10g.xci`, change the option, close it, and generate the new files. The transceiver side is not overwritten because of the `IS MANAGED= false` property. Figure 20 shows the two XCI files of the 10G IP. The symbol denotes the IP is unmanaged.

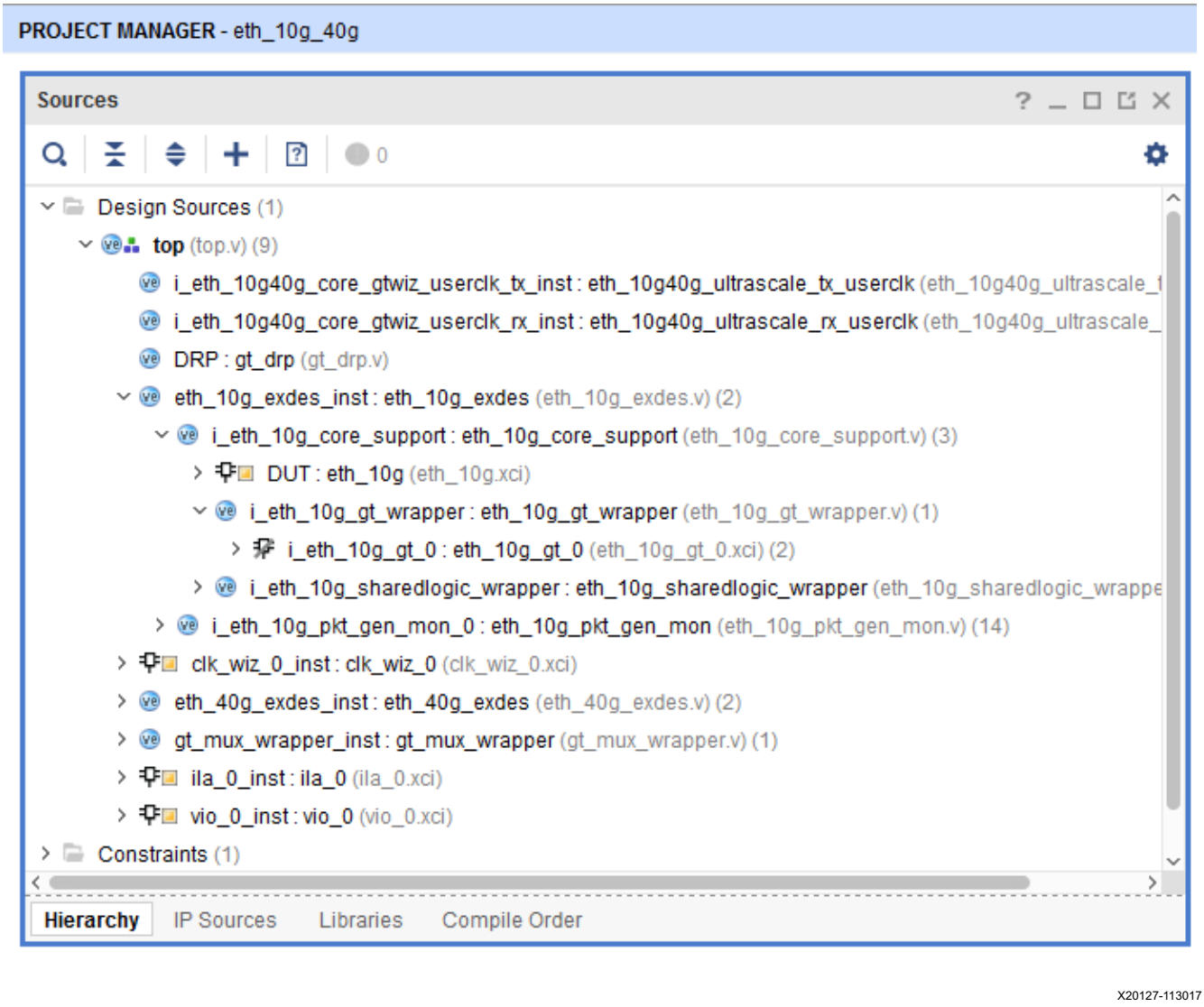

Figure 20: **Unmanaged IP Cores**

The behavior is the same if the design is ported to a new version of the Vivado design suite. Because the transceivers of the IP cores are unmanaged, it is possible to automatically update the IP cores without overwriting the modified part of the IP cores.

RECOMMENDED: *If the transceivers need to be updated, AMD recommends separately generating new transceivers and making sure they do not differ from the ones instantiated in the design. If they differ, the user should copy these modifications in the updated transceiver files.*

Hardware Test

The reference design has been validated in hardware using the KCU105 and ZCU102 evaluation boards. The Vivado logic analyzer is used to run the test. Virtual input/outputs (VIOs) are defined to force the state of some signals. For the test, the transceivers are set up in loopback PMA mode. Cables and optical modules are not required. Because the design uses the default clocks available on the board the oscillators do not need to be reconfigured. The reference clock for the transceivers is 156.25 MHz.

The frequency of the free-running clock needed for the DRP interface, DPR controller, and packet generator is 100 MHz. Because both boards only provide a 300 MHz free-running reference clock, a mixed-mode clock manager (MMCM) is instantiated in *top_test.v* to generate the 100 MHz from the 300 MHz. After the FPGA is configured, add all available signals in the VIO window using the "+" symbol (see Figure 21).

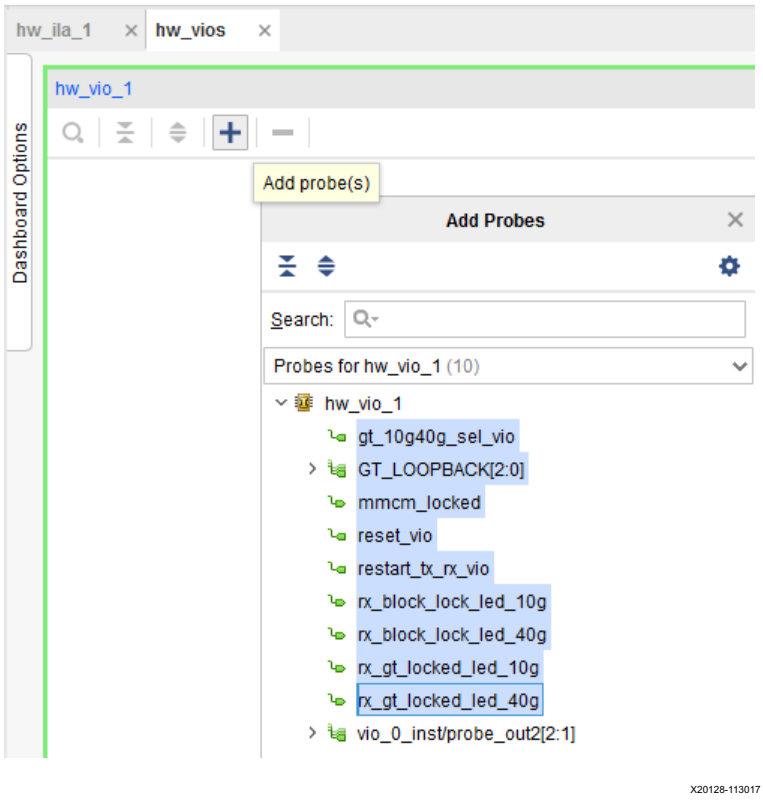

Figure 21: **Add Probes**

To run the test, use the VIO configuration in Table 6.

Table 6: **VIO Setup**

VIO	10G	40G
Outputs		
gt_10g40g_sel_vio	0	1
GT_LOOPBACK[2:0]	010	010
reset_vio	0	0
restart_tx_rx_vio	0	0
Inputs		
mmcm_locked	1	1
rx_gt_locked_led_10g	1	0
rx_block_lock_led_10g	1	0
rx_gt_locked_led_40g	0	1
rx_block_lock_led_40g	0	1

Figure 22 and Figure 23 show the VIO setup for 10G and 40G, respectively.

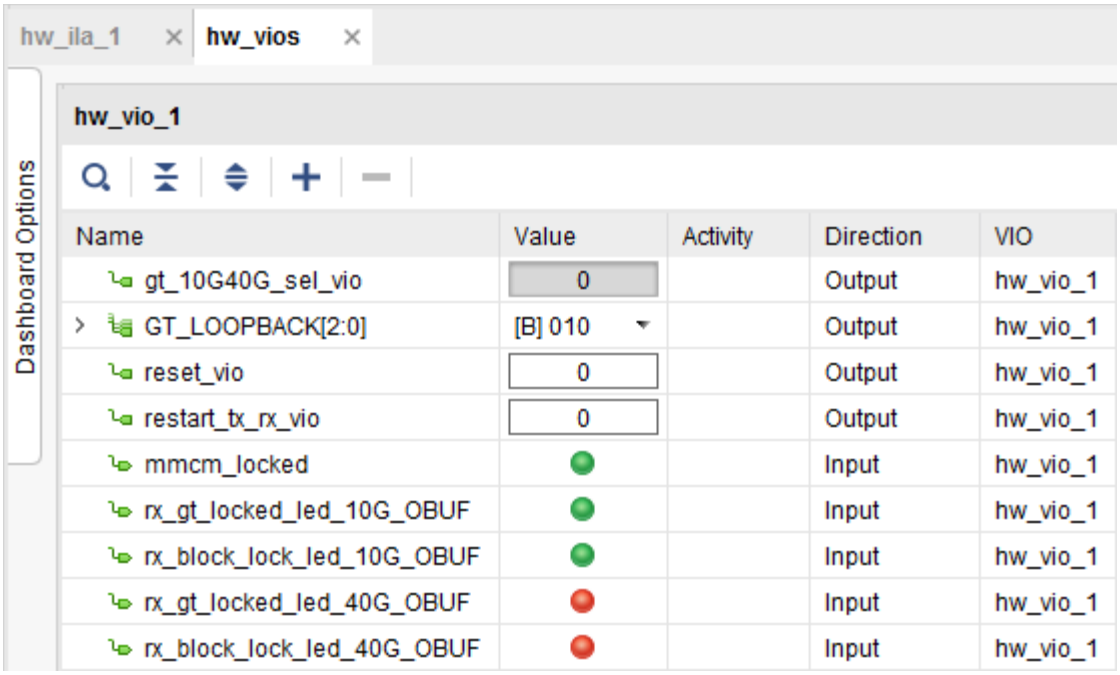

Figure 22: **VIO Setup for 10G**

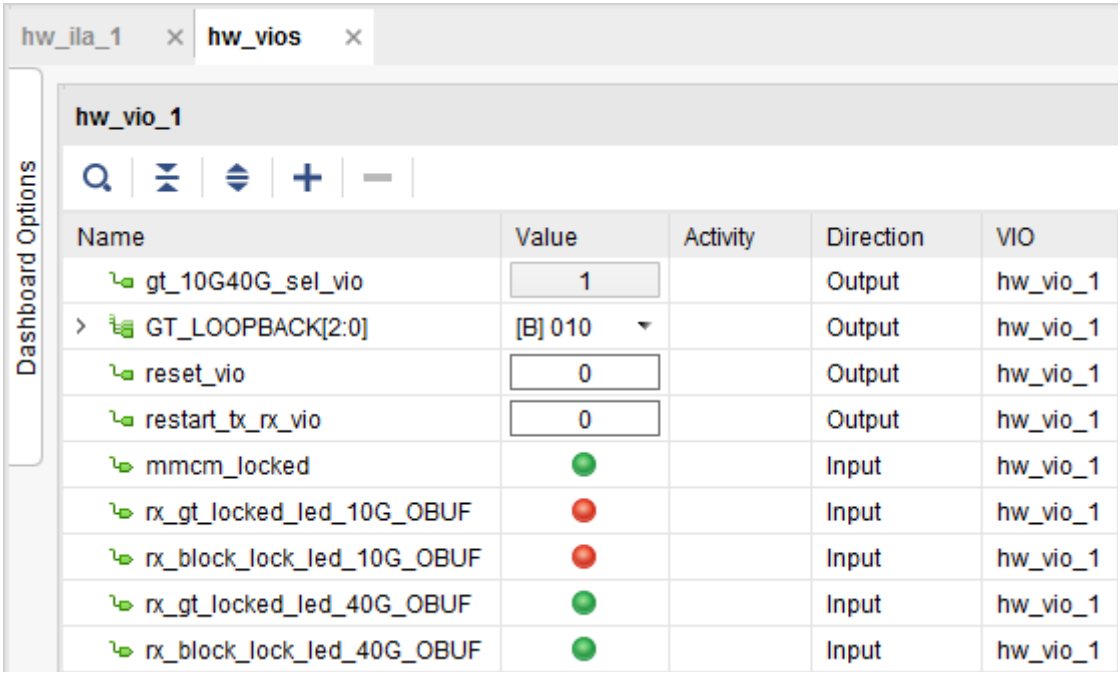

Figure 23: **VIO Setup for 40G**

The integrated logic analyzer (ILA) in Figure 24 shows the completion_status signals. A value of 1 means the test for the selected interface completed successfully.

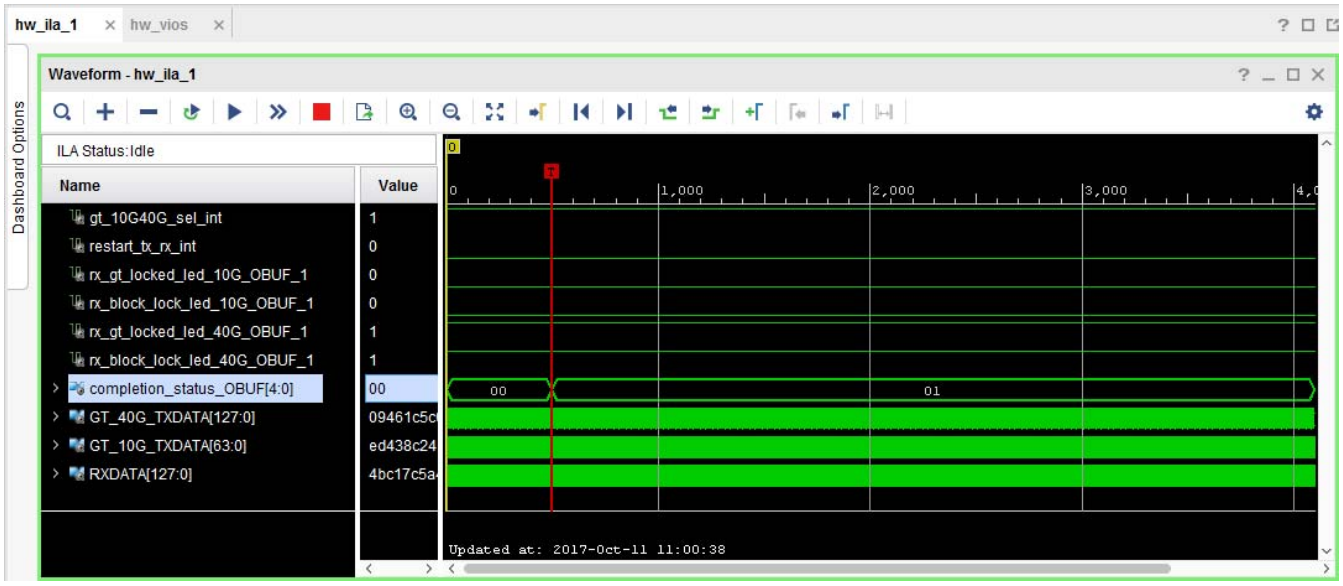

Figure 24: **ILA**

Table 7 lists the controls available on the evaluation boards.

Table 7: **Controls Available on the Board**

Ref	Control	Function	Notes
1	Pushbutton SW18	restart_tx_rx	
2	Pushbutton SW16	master reset	
3	LED DS38	rx_gt_locked_led_10g	
3	LED DS37	rx_block_lock_led_10G	
3	LED DS39	rx_gt_locked_led_40G	
3	LED DS40	rx_gt_locked_led_40G	
3	LED DS41:DS44	completion_status	When only DS44 is ON, status test= OK.
4	DIP Switch 8	gt_10g40g_sel	OFF= 10G, ON= 40G. When OFF, the port is controlled with the VIO.

Figure 25 and Figure 26 show the board controls for the KCU105 and ZCU102 evaluation boards, respectively.

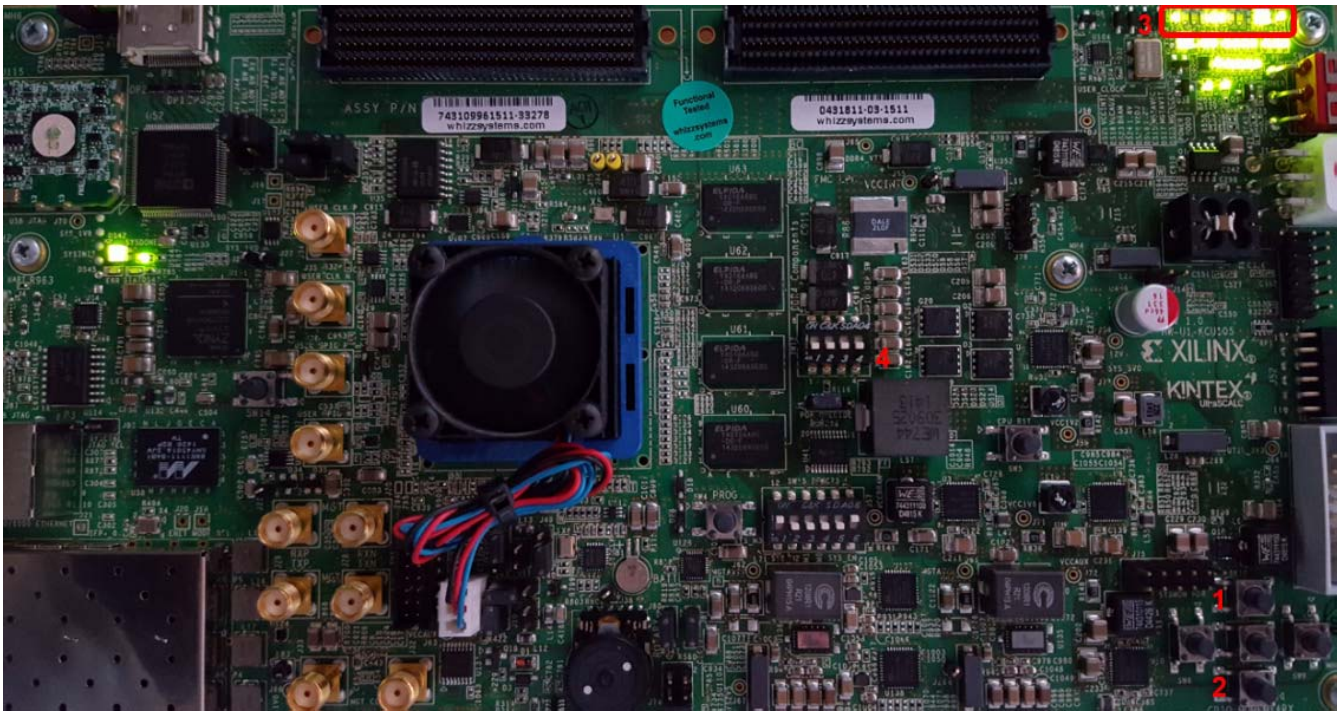

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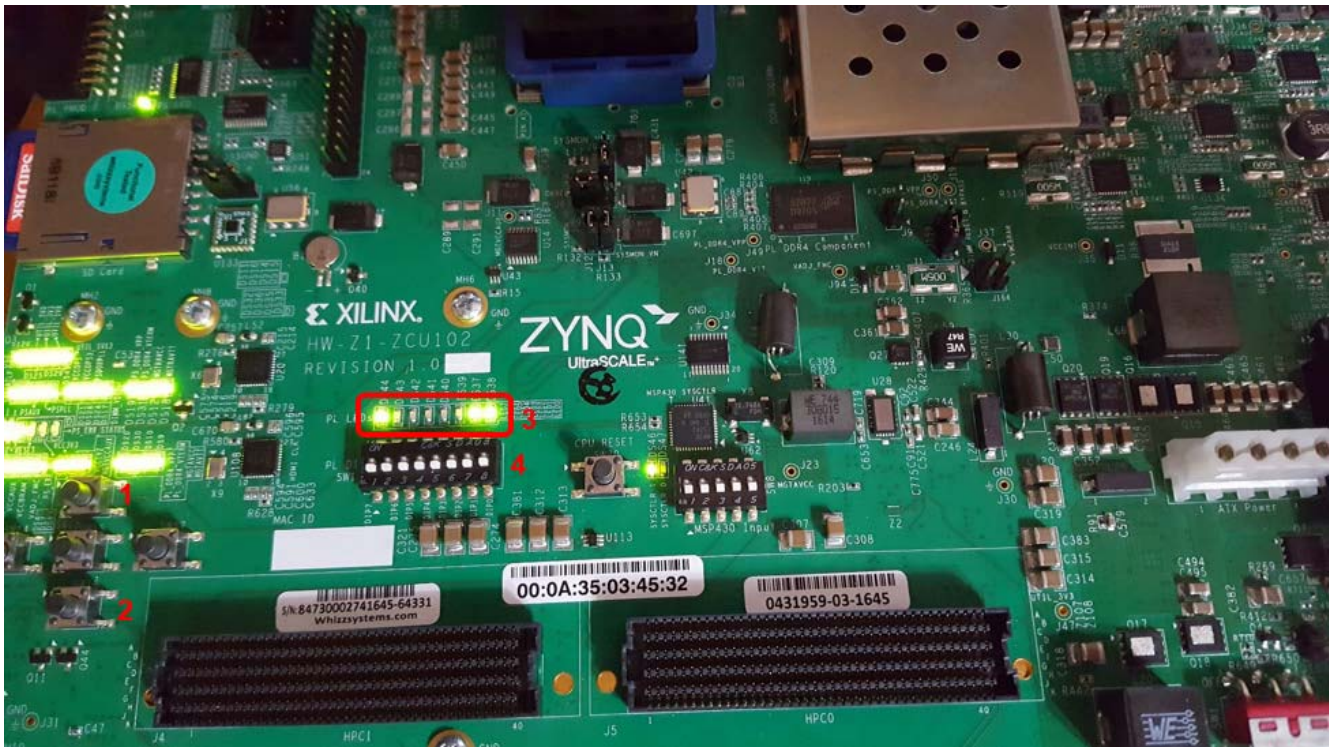
Figure 25: **KCU105 Board Controls**



X20133-113017

Figure 26: **ZCU102 Board Controls**

Conclusion

The reference design has been developed with these features:

- Interface:
  - 1x 40 GbE interface, 4 lanes at 10.3125 Gb/s
  - 1x 10 GbE interface, 1 lane at 10.3125 Gb/s
- The interface is real-time switchable:
  - Single bit file, single port operation
  - The reference design includes MACs for both interfaces
- Data connectivity to user application is through AXI interfaces
- IEEE PTP 1588v2 two step
- Power down of the unused transceivers when working in 10G mode

Finding Additional Documentation

Documentation Portal

The AMD Adaptive Computing Documentation Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Documentation Portal, go to https://docs.amd.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help > Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Note: For more information on DocNav, refer to the *Documentation Navigator User Guide* (UG968).

References

1. *10G/25G High Speed Ethernet Subsystem Product Guide v2.1* (PG210)
2. *40G/50G High Speed Ethernet Subsystem Product Guide v2.1* (PG211)
3. *1G to 10G Ethernet Dynamic Switching Using Xilinx High Speed Serial I/O Solution* (XAPP1243)
4. *UltraScale Architecture GTH Transceivers User Guide* (UG576)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/19/2024	1.0.1	Editorial updates only. No technical content updates.
02/02/2018	1.0	Initial Xilinx release.

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