



Diamond Jog BGA Breakout Geometries

WP538 (v1.0) September 14, 2022

Abstract

This document discusses BGA breakout techniques used on Xilinx® 1 mm pitch BGA devices high-speed interfaces with a data rate of 32 Gb and above. The context includes PCB layout decisions for BGA breakout and what compromises are needed to reduce crosstalk. Traditional designs used a diagonal BGA breakout because it creates the most usable routing area under a BGA device. However, with evermore faster interfaces with data rates at 32 Gb and above, we see a reduction in the usable routing area underneath due to the large keep-out areas required for signal fidelity. This white paper proposes a new BGA breakout style, the *Diamond Jog* that produces numerous advancements over the traditional *Diagonal Jog*, with limited drawbacks. To use the *Diamond Jog* breakout method:

- Convert *horizontal* solder ball alignment to *vertical* via alignment, freeing up routing channels
- Switch differential pair routing polarity by jogging to either the top or bottom via from either solder ball

This method avoids high-crosstalk scenarios by providing additional routing flexibility for FPGA breakouts.

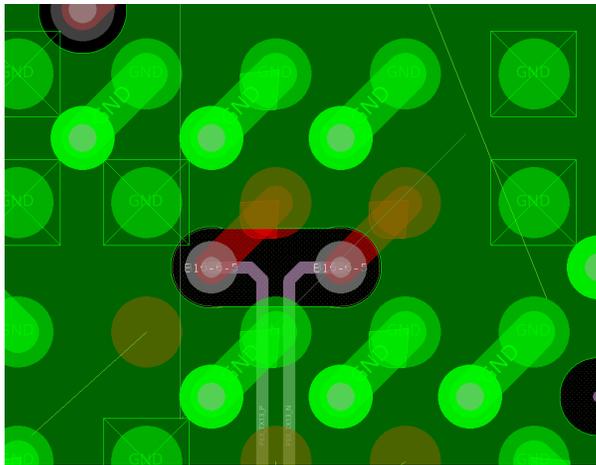
Xilinx is creating an environment where employees, customers, and partners feel welcome and included. To that end, we're removing non-inclusive language from our products and related collateral. We've launched an internal initiative to remove language that could exclude people or reinforce historical biases, including terms embedded in our software and IPs. You may still find examples of non-inclusive language in our older products as we work to make these changes and align with evolving industry standards. Follow this [link](#) for more information.

Breakout Types

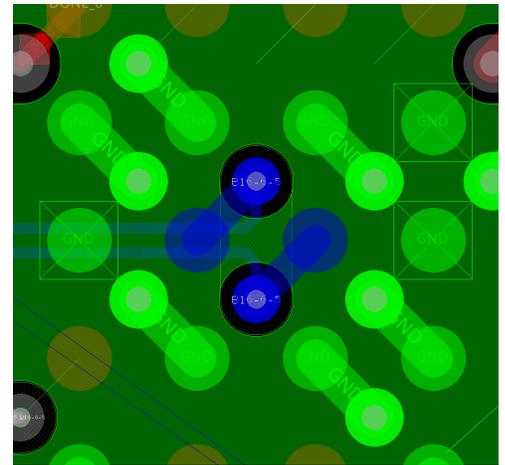
The following images show the standard diagonal jog and the diamond jog breakout types. The standard diagonal 45-degree jog is to a via with both jogs in the same direction. The diamond type breakout has a 45-degree jog to a via with jogs in the opposite direction.

Figure 1: Standard Diagonal and Diamond Jog Breakouts

Standard Diagonal Jog



Diamond Jog

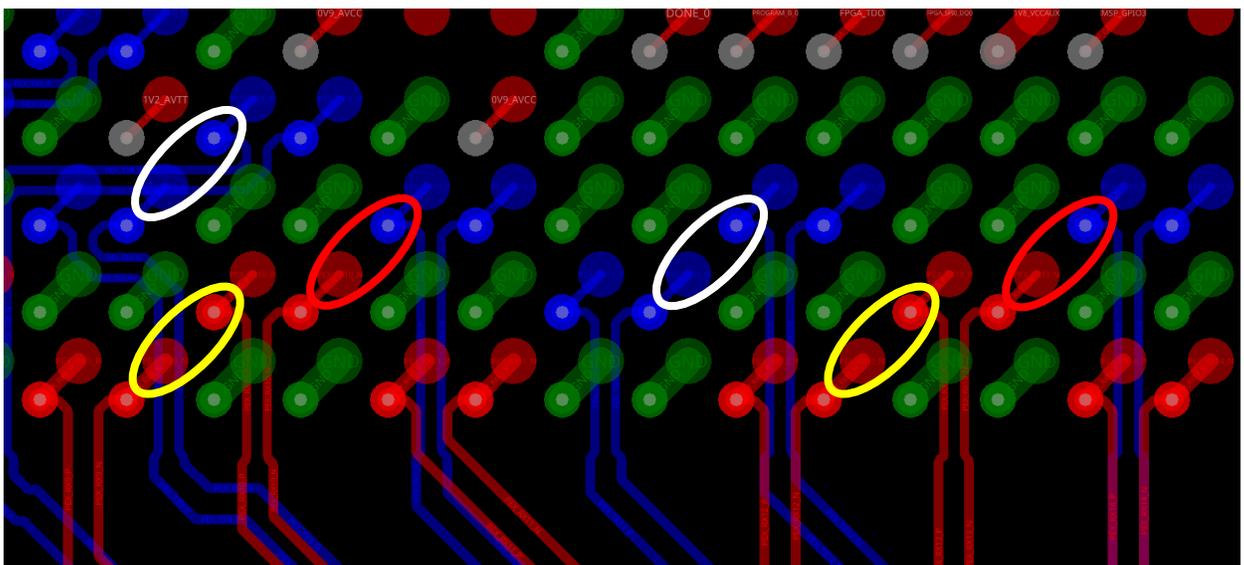


X25589-073021

PCIe Diagonal vs. Diamond Jog Breakout

The following images show a typical PCIe® BGA breakout. The TX is the red trace on layer 3, and the RX is the blue trace on layer 5.

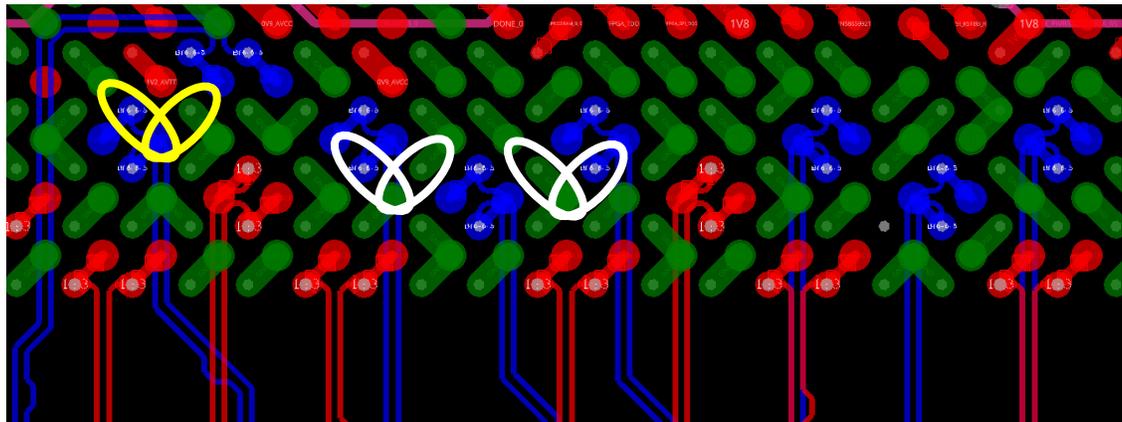
Figure 2: Standard Diagonal Jog Via Structure



X25675-100821

Note: The color highlight shows the proximity of the noise source and the noise recipient in the order of amplitude (red, yellow, or white), with red having the worst crosstalk.

Figure 3: Diamond Jog Via Structure



X25674-100821

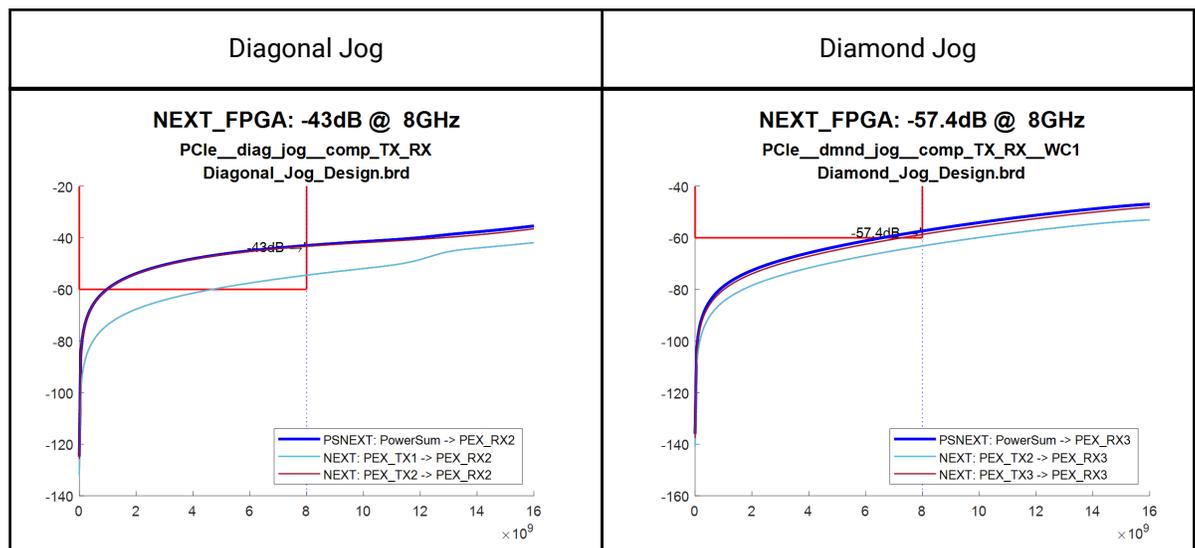
Note: The color highlight shows the reduction in proximity of the noise source and the noise recipient.

PCIe Crosstalk Simulation Results

The following images show the comparative results of diagonal jog vs. diamond jog simulations of near-end crosstalk (NEXT) and far-end crosstalk (FEXT). A decrease (improvement) in crosstalk is shown in all cases using the diamond job breakout.

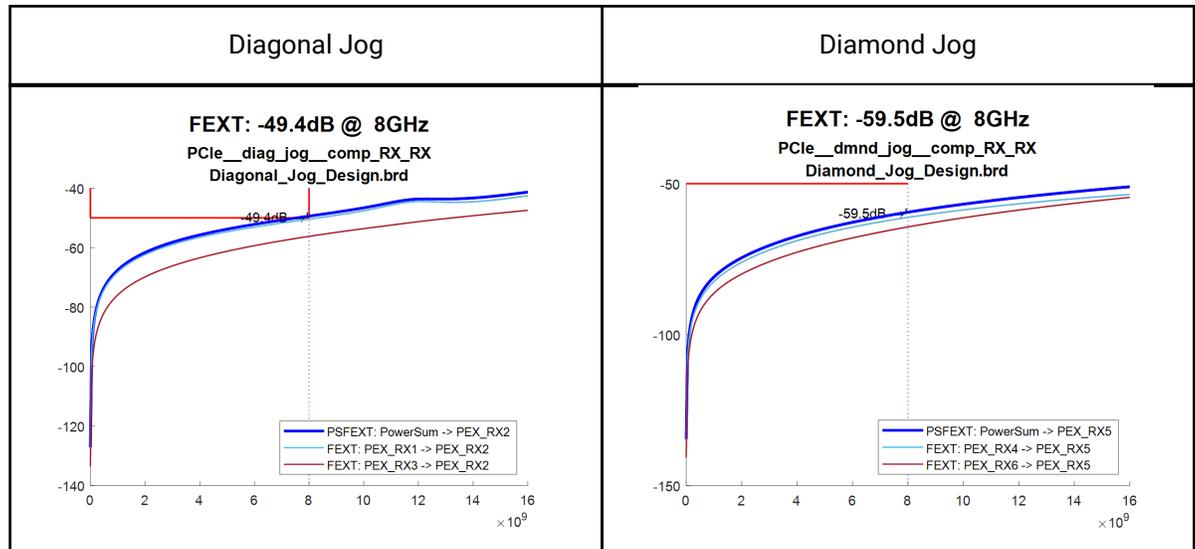
- TX-RX NEXT (Figure 4) shows the red highlights in Figure 2.
- RX-RX FEXT (Figure 5) shows the yellow highlights in Figure 2.
- TX-TX FEXT (Figure 6) shows the white highlights in Figure 2.

Figure 4: TX-RX NEXT Crosstalk



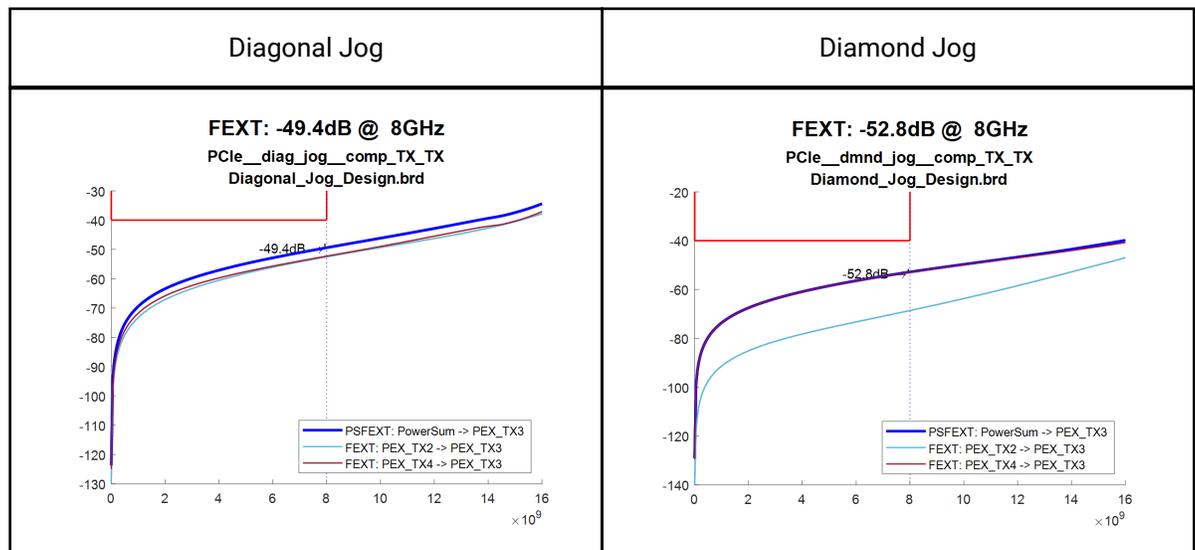
X25679-081922

Figure 5: RX-RX FEXT Crosstalk



X25680-081922

Figure 6: TX-TX FEXT Crosstalk



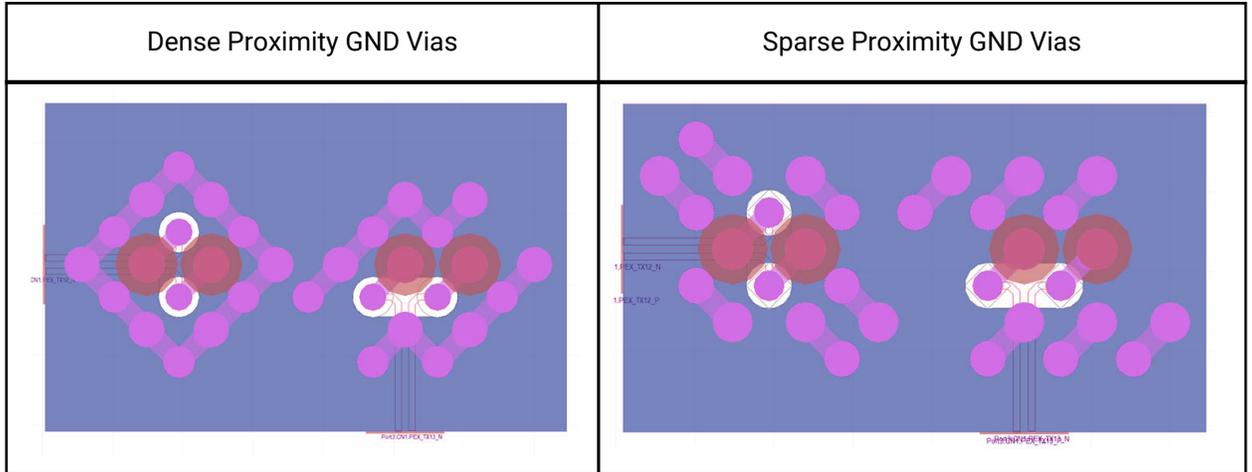
X25681-081922

High Signal Integrity Via Structures

This section shows a snapshot of detailed simulations comparing diagonal jog and diamond jog via structures.

The following figure shows a detailed example of a diagonal jog breakout vs a diamond jog breakout. Differences between the breakouts were compared in two GND via proximity environments, densely populated proximity GND vias and sparsely populated proximity GND vias. Ideally, you would use dense proximity GND vias. However, device pin out could dictate the use of sparse proximity GND vias.

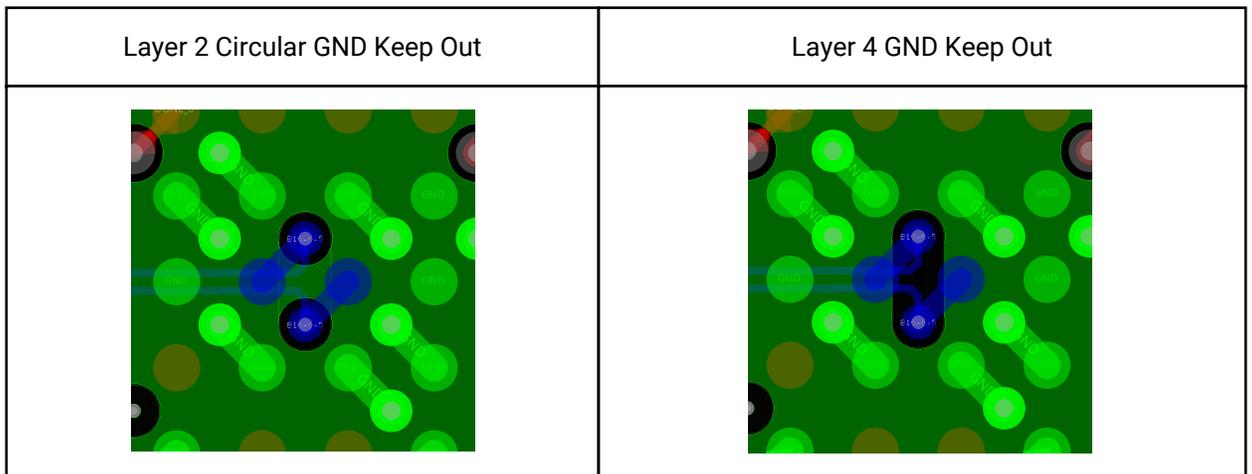
Figure 7: Comparison of Dense GND Via Structure vs. Sparse GND Via Structure



X25682-100821

Broadly, the simulation results show either an equivalent or a net gain in all metrics for the diamond jog breakout. Dense proximity GND vias are marginally better than the sparse proximity GND vias. Layer 2 GND keep outs must be circular to minimize trace-to-trace crosstalk between the signal traces on layer 1 and layer 3. In addition under this structure, the GND keep outs must be on the lower layers a shown in the following example.

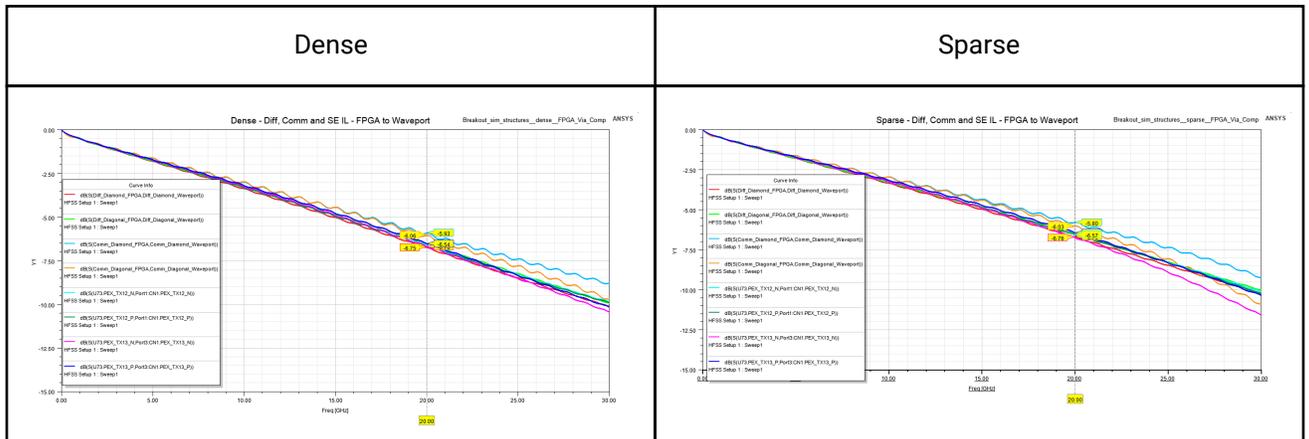
Figure 8: GND Keep Outs



X25683-100821

As shown in the following figure, in both GND via proximity environments (dense and sparse) the insertion losses for the diamond jog breakout and diagonal jog breakout were within a 1 dB range.

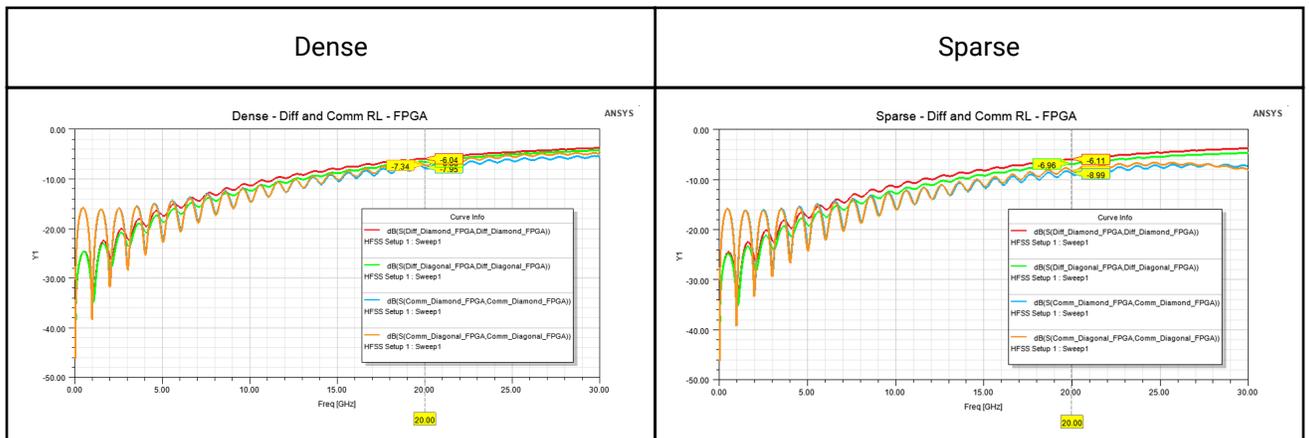
Figure 9: Differential, Common, and Single Ended Insertion Loss



X25684-100821

As shown in the following figure, in both GND via proximity environments (dense and sparse) the return losses for the diamond jog breakout and diagonal jog breakout were within a 1 dB range.

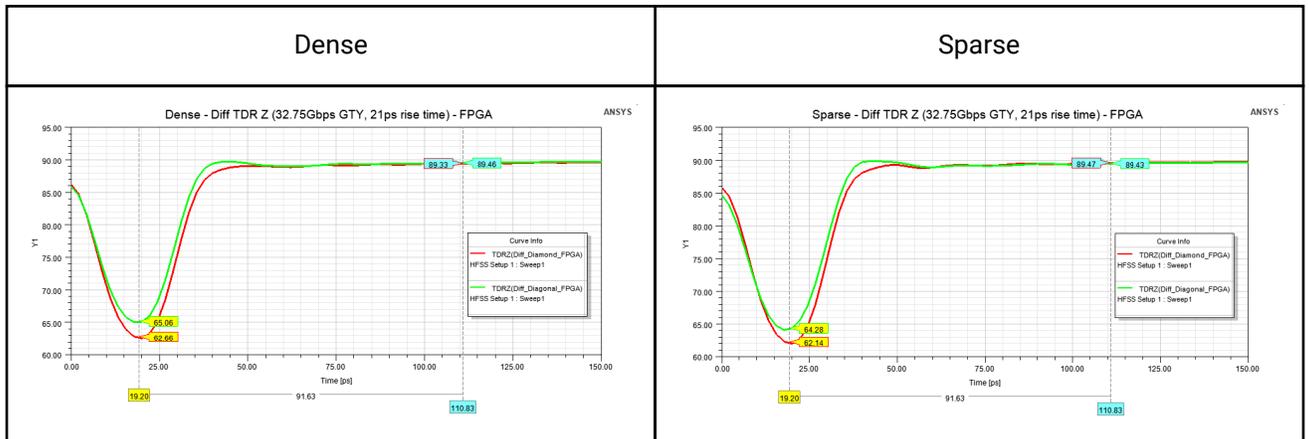
Figure 10: Differential and Common Return Loss



X25685-100821

As shown in the following figure, in both GND via proximity environments (dense and sparse) the differential time domain reflections (TDR) impedance for the diamond jog breakout and diagonal jog breakout were within a 3Ω range. A TDR measures the reflections along a conductor.

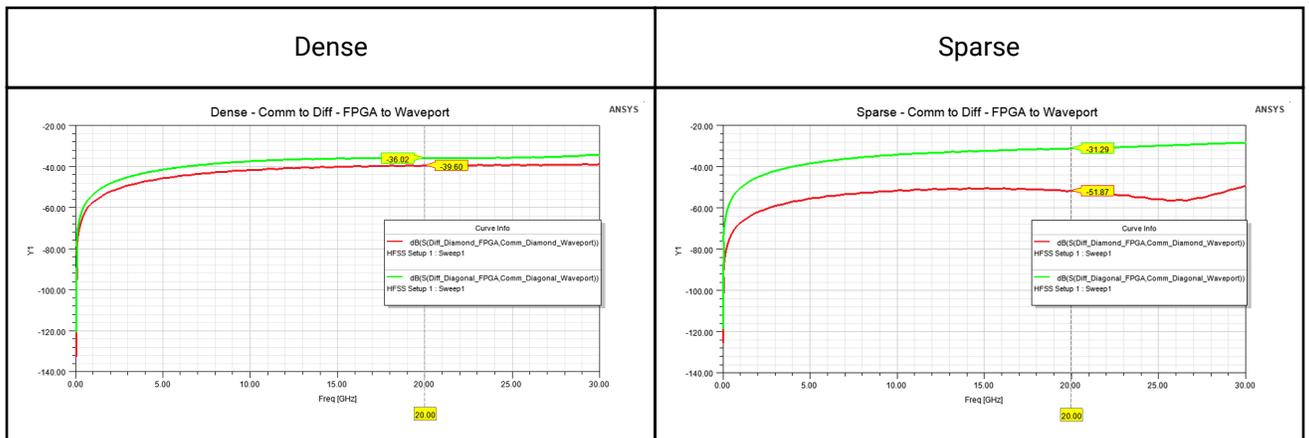
Figure 11: Differential TDR Impedance (Z) at 32.75 Gb/s GTY, 21 ps Rise Time



X25686-100821

As shown in the following figure, in both GND via proximity environments (dense and sparse) the diamond jog breakout is better than the diagonal jog breakout.

Figure 12: Common to Differential Mode Conversion

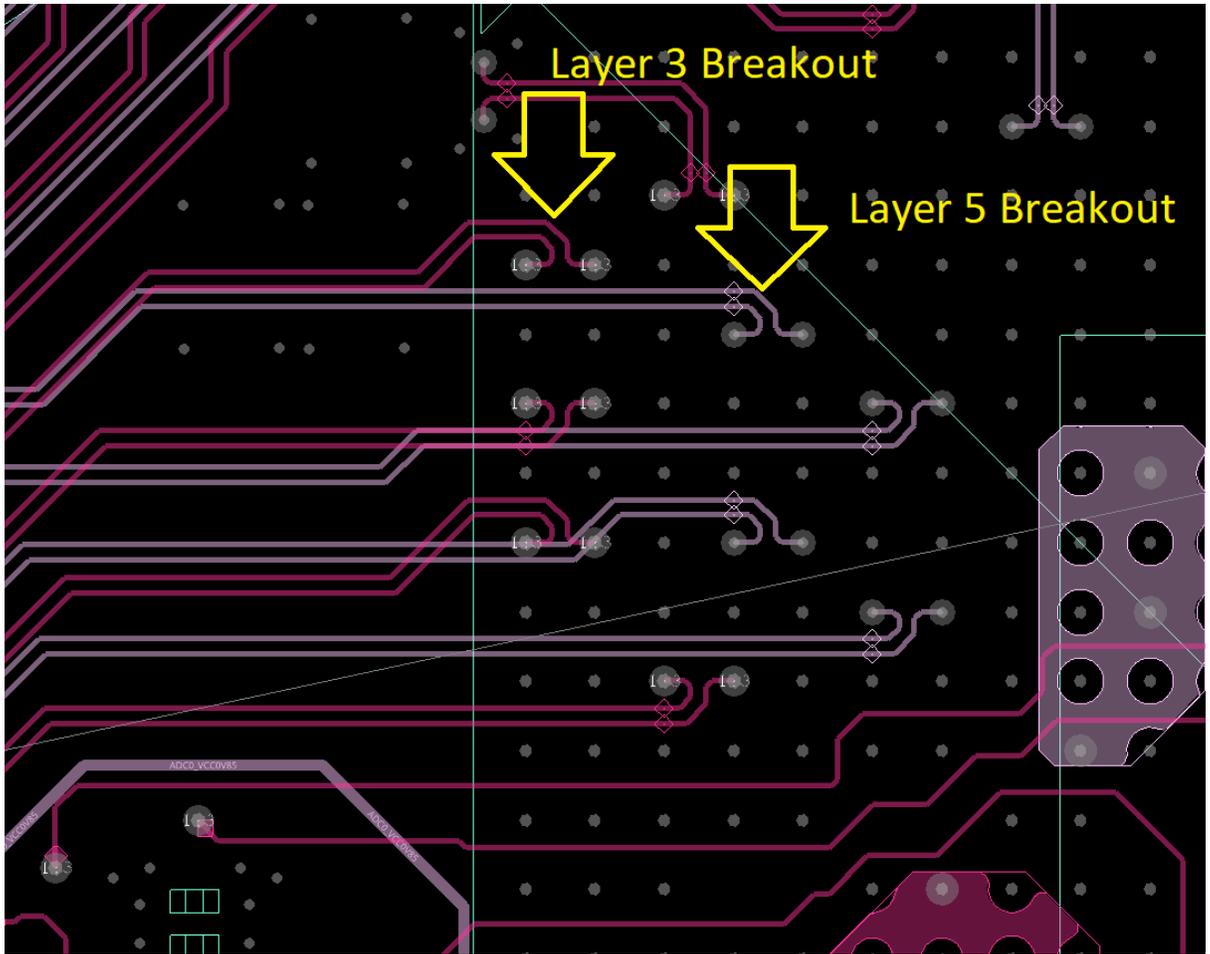


X25687-100821

GTY Transceiver Breakout Use Case

The following example shows a typical GTY transceiver breakout of a small form-factor pluggable (SFP) data bus on a Virtex® UltraScale+™ device (VU23P). In the image, the RX signals are routed on layer 3 (dark pink) and the TX signals are routed on layer 5 (light pink).

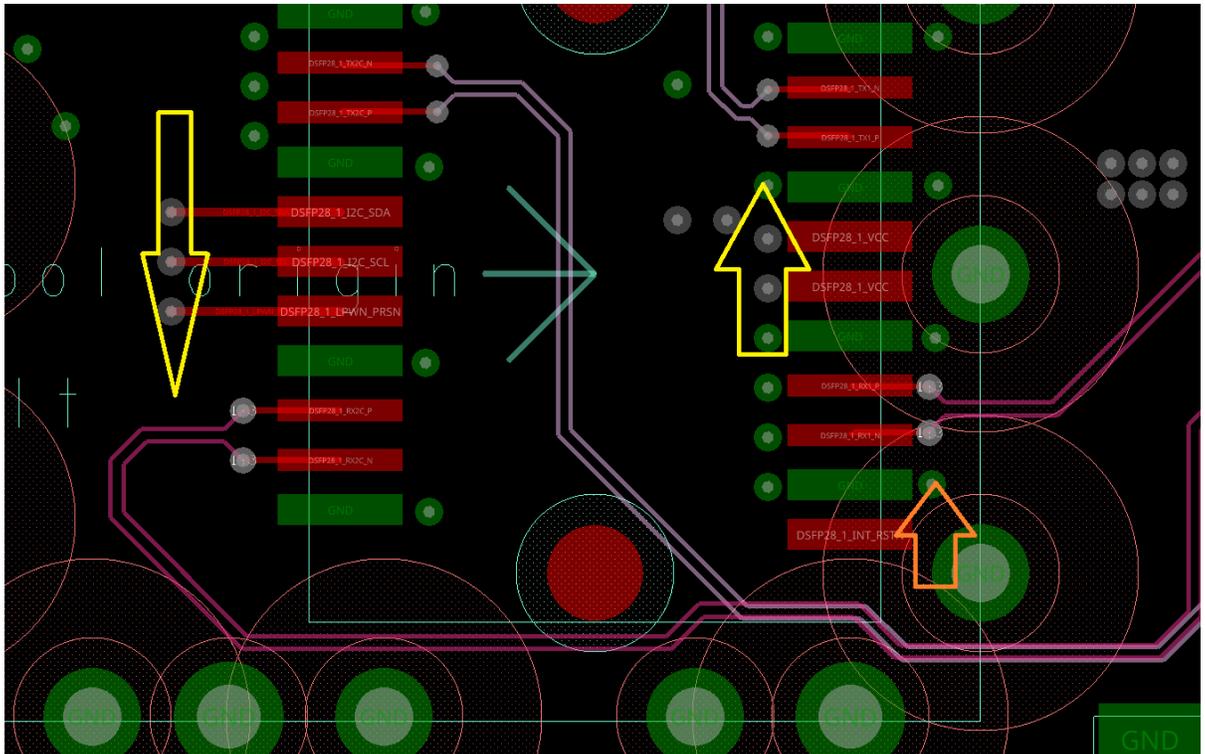
Figure 13: GTY Transceiver Breakout



X25846-100821

The following image shows the opposite end of the differential pair trace terminating at an SFP SMT connector. The ideal entry for a non-via in pad is marked by the orange arrow. The yellow arrows show a sub-optimal entry.

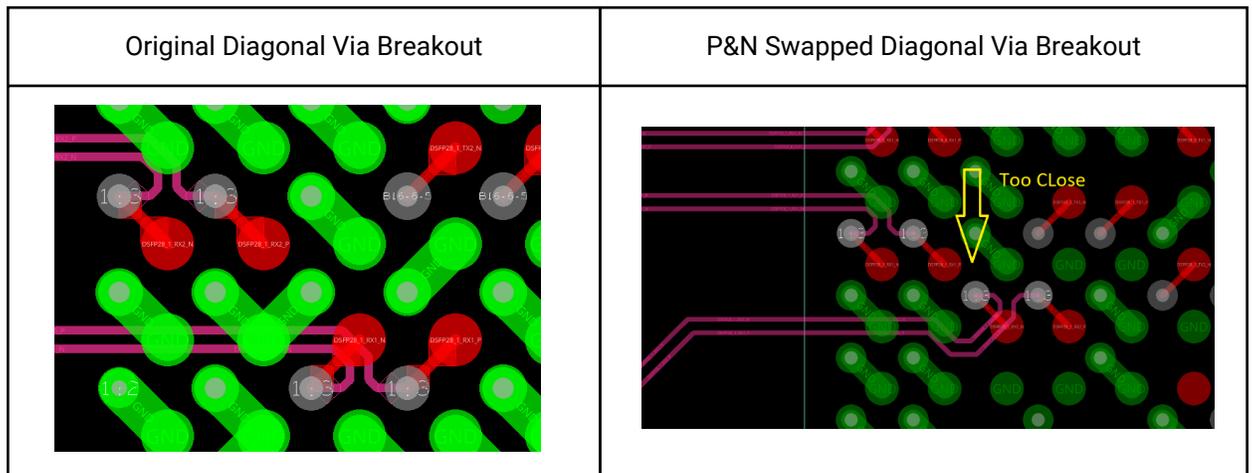
Figure 14: Differential Pair Trace Terminating at an SFP SMT Connector



X25847-100821

The SFP entry is compromised because there are routing loopbacks on entry, that effects the P-N skew and influences signal fidelity. By performing P&N swaps at the FPGA end, we can reduce the SFP entry to two loopbacks. However, it will make the proximity issue worse, and via to pad distances will be reduced to a critical distance because the jog via is moved closer to the adjacent GTY transceiver breakout pair. This is shown in the following image.

Figure 15: Comparing Standard with P&N Swapped Diagonal Via Breakouts



X25848-100821

The following image shows the proposed new breakout. It offers maximum distance pad to via, no cross routing at via structures, and reduces loopback occurrences to just one from four. By mixing via structure breakouts, we can maximize the distance between via and pad and remove all instances of trace proximity. The diamond breakout allows the P&N swap to remove loopback at the DSFP connector end. In this image:

- Diamond jog breakout is circled in orange
- Southeast diagonal jog breakout is circled in yellow

Figure 16: Proposed Breakouts to Reduce Loopback Occurrences



X25849-100821

Conclusion

With comparable or improved signal fidelity, the flexibility offered by the diamond jog breakout structure allows for significantly reduced crosstalk by having the option of moving signal vias further away from noise producing vias. The diamond jog's ability to perform PCB level P-N swaps enables the reduction of routing complexity, such as loopback or crossovers, as well as provides greater area utilization of the available PCB real estate. This structure can be used for BGA breakouts throughout a PCB design. This structure was analyzed and can be used at data rates up to 28 Gb/s.

References

These documents provide supplemental material useful with this guide:

1. *UltraScale Architecture PCB Design User Guide (UG583)*

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
9/14/2022 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm#tos>.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright

© Copyright 2022 Advanced Micro Devices, Inc. Xilinx, the Xilinx logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. PCI, PCIe, and PCI Express are trademarks of PCI-SIG and used under license. All other trademarks are the property of their respective owners.